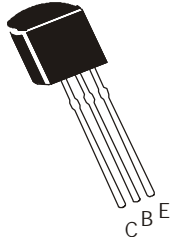


**PNP SILICON PLANAR EPITAXIAL TRANSISTORS**

**BC486, A, B, L**  
**BC488, A, B, L**  
**BC490, A, B, L**

**TO-92**  
**Plastic Package**



**High Current Transistors**

**ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub>=25°C)**

DESCRIPTION	SYMBOL	BC486	BC488	BC490	UNITS
Collector Emitter Voltage	V <sub>CEO</sub>	45	60	80	V
Collector Base Voltage	V <sub>CBO</sub>	45	60	80	V
Emitter Base Voltage	V <sub>EBO</sub>	4.0			V
Collector Current Continuous	I <sub>C</sub>	1.0			A
Power Dissipation at T <sub>a</sub> =25°C	P <sub>D</sub>	625			mW
Derate Above 25°C		5.0			mW/°C
Power Dissipation at T <sub>c</sub> =25°C	P <sub>D</sub>	1.5			W
Derate Above 25°C		12			mW/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to +150			°C

**THERMAL RESISTANCE**

Junction to Case	R <sub>th(j-c)</sub>	83.3	°C/W
Junction to Ambient in free air	R <sub>th(j-a)</sub>	200	°C/W

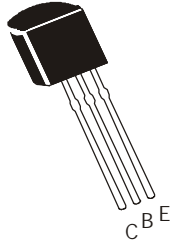
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=25°C unless specified otherwise)**

DESCRIPTION	SYMBOL	TEST CONDITION	BC486	BC488	BC490	UNITS
Collector Emitter Voltage	V <sub>CEO</sub>	I <sub>C</sub> =1mA, I <sub>B</sub> =0	>45	>60	>80	V
Collector Base Voltage	V <sub>CBO</sub>	I <sub>C</sub> =100µA, I <sub>E</sub> =0	>45	>60	>80	V
Emitter Base Voltage	V <sub>EBO</sub>	I <sub>E</sub> =10µA, I <sub>C</sub> =0	>4.0			V
Collector Cut Off Current	I <sub>CBO</sub>	V <sub>CB</sub> =30V, I <sub>E</sub> =0 V <sub>CB</sub> =40V, I <sub>E</sub> =0 V <sub>CB</sub> =60V, I <sub>E</sub> =0,	<b>BC486</b> <b>BC488</b> <b>BC490</b>	<100		nA
DC Current Gain	h <sub>FE</sub>	I <sub>C</sub> =10mA, V <sub>CE</sub> =2V I <sub>C</sub> =100mA, V <sub>CE</sub> =2V <b>BC486/488/490</b> <b>BC486L/488L/490L</b> <b>BC486A/488A/490A</b> <b>BC486B/488B/490B</b> *I <sub>C</sub> =1A, V <sub>CE</sub> =5V	>40		60 - 400 60 - 150 100 - 250 160 - 400	
Collector Emitter Saturation Voltage	V <sub>CE(sat)</sub>	I <sub>C</sub> =500mA, I <sub>B</sub> =50mA *I <sub>C</sub> =1A, I <sub>B</sub> =100mA	<0.50		TYP 0.50	V
Base Emitter Saturation Voltage	V <sub>BE(sat)</sub>	I <sub>C</sub> =500mA, I <sub>B</sub> =50mA *I <sub>C</sub> =1A, I <sub>B</sub> =100mA	<1.2		TYP 1.0	V

**\*Pulse test:- Pulse Width =300ms, Duty Cycle 2%**

BC486\_490 Rev\_1 210109E

## PNP SILICON PLANAR EPITAXIAL TRANSISTORS



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TO-92  
Plastic Package

### ELECTRICAL CHARACTERISTICS ( $T_a=25^\circ\text{C}$ unless specified otherwise)

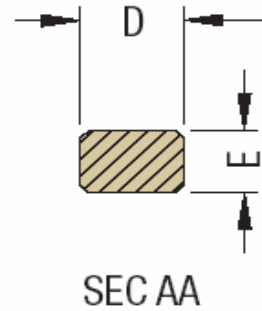
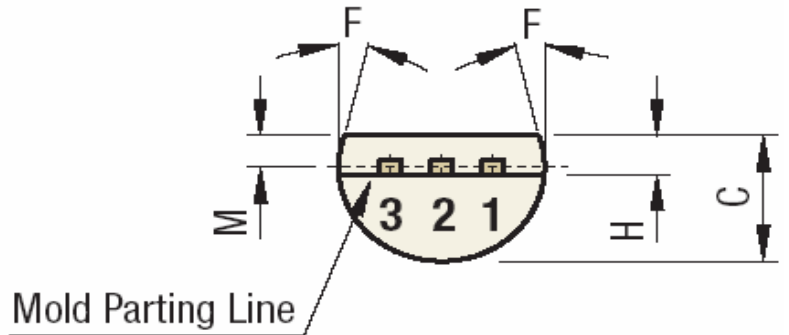
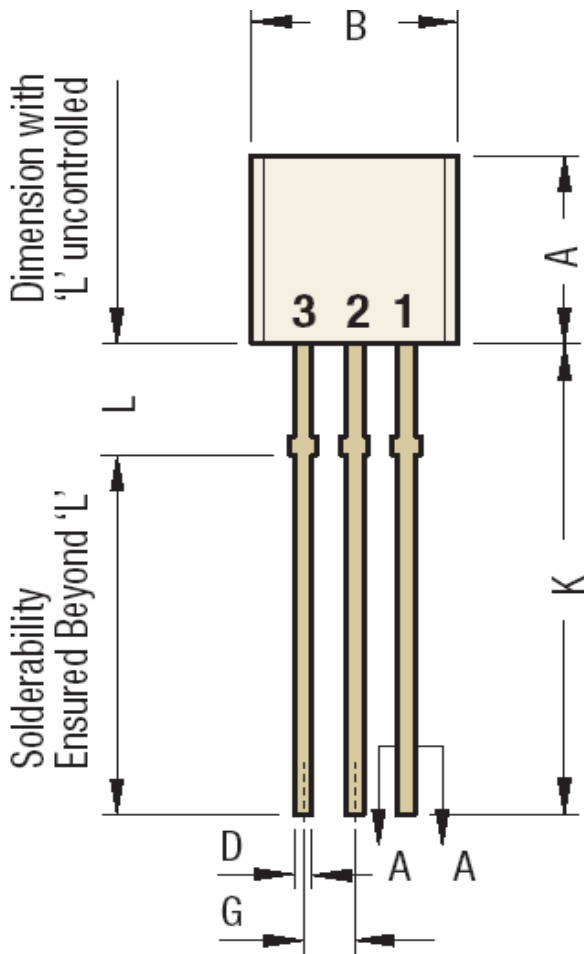
#### SMALL SIGNAL CHARACTERISTICS

DESCRIPTION	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Transistors Frequency	$f_T$	$I_C=50\text{mA}$ , $V_{CE}=2\text{V}$ , $f=100\text{MHz}$		150		MHz
Output Capacitance	$C_{ob}$	$V_{CB}=10\text{V}$ , $f=1\text{MHz}$		9.0		pF
Input Capacitance	$C_{ib}$	$V_{EB}=0.5\text{V}$ , $f=1\text{MHz}$		110		pF

BC486, A, B, L  
 BC488, A, B, L  
 BC490, A, B, L

TO-92  
 Plastic Package

TO-92 Leaded Plastic Package

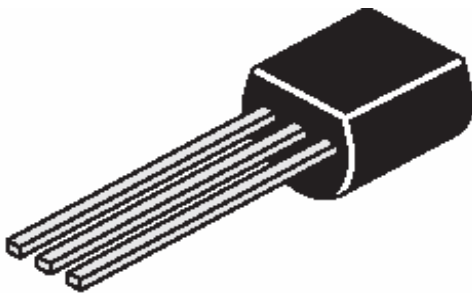


DIM	Min	Max
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.41	0.55
E	0.35	0.55
F	5°	

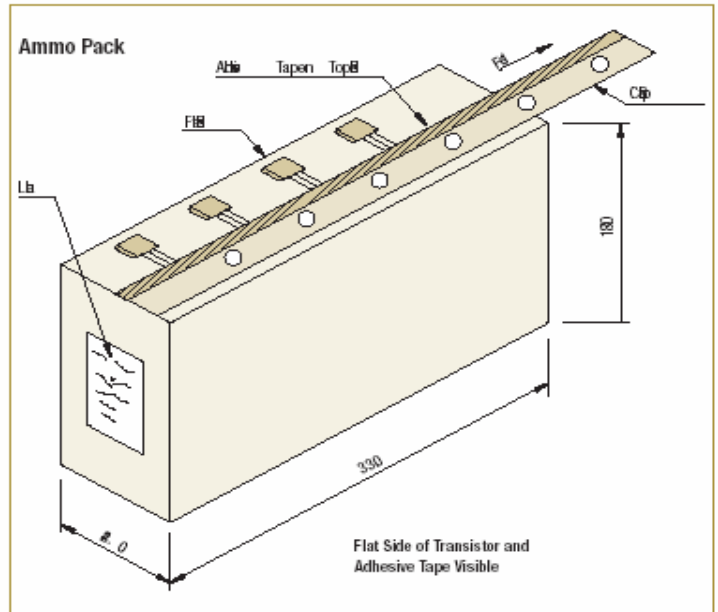
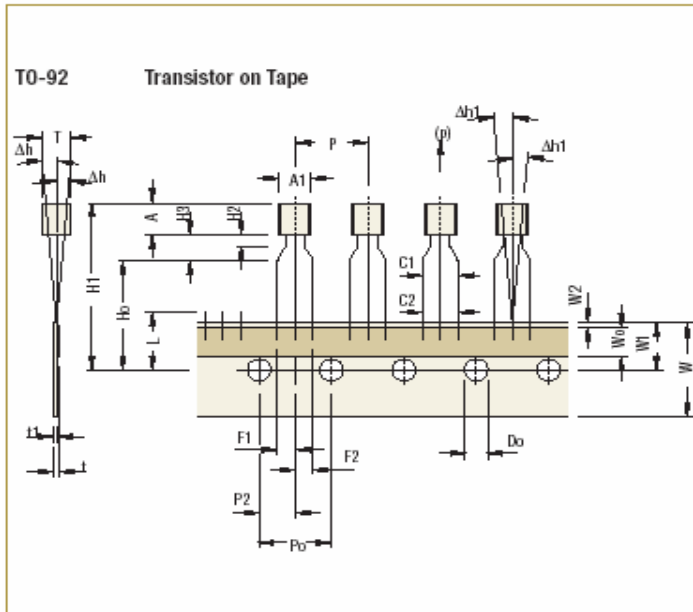
All Dimensions are in mm

DIM	Min	Max
G	1.14	1.40
H	1.20	1.80
K	12.5	
L	1.982	2.082
M	1.03	1.53

Pin 1 Emitter  
 Pin 2 Base  
 Pin 3 Collector



TO-92 Tape and Ammo Packaging



All Dimensions are in mm

Tape Specifications

Item description	Symbol	TO-92			
		Min	Nom	Max	Tol
Body width	A1	4.45		5.20	
Body height	A	4.32		5.33	
Body thickness	T	3.18		4.19	
Pitch of component <sup>Cr</sup>	P		12.7		±1.0
Feed hole pitch <sup>§1</sup>	Po		12.7		±0.3
Feed hole center to component centre <sup>§2</sup>	P2		6.35		±0.4
Comp. alignment, Side view <sup>§3</sup>	Dh		0	1.0	
Comp. alignment, Front view <sup>§3</sup>	Dh1		0	1.3	
Tape width <sup>Cr</sup>	W		18		±0.5
Hold down tape width <sup>Cr</sup>	W0		6		±0.2
Hole position	W1		9		+0.7 -0.5
Hold-down tape position	W2	0.0		0.7	
Lead wire clinch height	Ho		16		±0.5
Component height	H1			24.0	
Length of snapped leads	L			11.0	
Feed hole diameter <sup>Cr</sup>	Do		4		±0.2
Total tape thickness <sup>§4</sup>	t			1.2	
Lead-to-lead distance <sup>Cr</sup>	F1, F2	2.4		2.7	
Stand off	H2	0.45		1.45	
Clinch height	H3			3.0	
Lead parallelism <sup>Cr</sup>	C1-C2			0.22	
Pull-out force	(p)	6N			

All Dimensions are in mm

Taping Specification

- Maximum alignment deviation between leads not to be greater than 0.20 mm.
- Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
- Hold down tape not to exceed beyond the edge(s) carrier tape and there shall be no exposure of adhesive.
- No more than 3 consecutive missing components is permitted.
- A tape trailer, having at least three feed holes is required after the last component.
- Splices shall not interfere with the sprocket feed holes.

§1 Cumulative pitch error 1.0 mm/20 pitch.

§2 To be measured at bottom of clinch.

§3 At top of body.

§4 t1 = 0.3 – 0.6 mm

Cr Critical Dimension.

**TO-92  
 Plastic Package**

**Packaging Information**

T & A: Tape and Ammo Pack; T & R: Tape and Red; Bulk: Loose in Poly bags; Tube: Tube and Ammo Pack; k: 1.000

Package/Case Type	Packaging Type	Std. Packing	Inner Carton			Outer Carton		
		Qty	Qty	Size L x W x H (cm)	Gross Weight (Kg)	Qty	Size L x W x H (cm)	Gross Weight (Kg)
TO-92	Bulk	1,000	5K	19x19x8	1.10	80K	43x40x35	20.0
	T&A	2,000	2K	32x4.5x20	0.70	40K	43x40x35	15.20

**Component Disposal Instructions**

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

**Customer Notes**

**Disclaimer**

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s). CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.



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