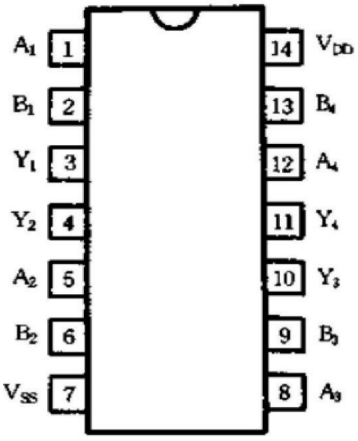
Four 2-input OR gate CD4001

summary

CD4001 is composed of four 2-input CMOS or NOT gate circuits, and this device is mainly used as a general-purpose 2-input or NOT gate.



Recommended working conditions:

Power supply voltage…….....V～15V

Input Voltage…..... 0V～VDD

Operating temperature range

0℃～70℃

Limit value:

supply voltage…...－0.5V～18V

INPUT VOLTAGE……－0.5V~VDD+0.5V

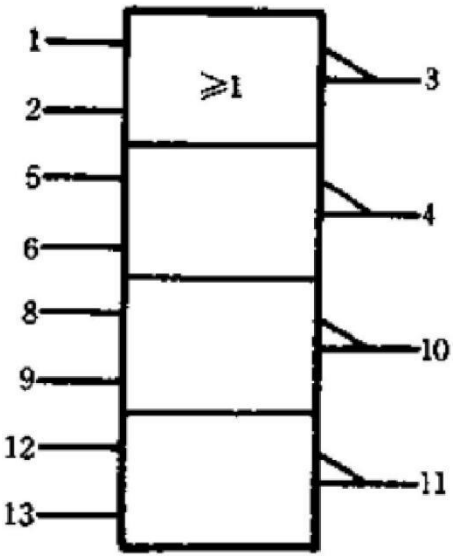
welding temperature（10S）T_L.....265℃

storage temperatureT_S..... －65℃～150℃

Lead out symbol：

1A～4A	Data input terminal
1B～4B	Data input terminal
VDD	Positive power supply
Vss	grounds
1Y～4Y	Data input terminal

逻辑符号



logical expression： $Y = \overline{A \quad B}$

static characteristic:

parameter	Test conditions			value	UNIT
	Vo/V	Vi/V	VDD/V	25℃	
V_{OL} Low output Level voltage (maximum)	-	5/0 10/0 15/0	5.0 10.0 15.0	0.05	V
V_{OH} Output high Level voltage (minimum)	-	5/0 10/0 15/0	5.0 10.0 15.0	4.95 9.95 14.95	V
V_{IL} Input low Level voltage (maximum)	4.5 9.0 13.5	-	5.0 10.0 15.0	1.5 3.0 4.0	V
VIH input high Level voltage (minimum)	0.1 1.0 1.5	-	5.0 10.0 15.0	3.5 7.0 11.0	V
Output high level Current IOH (minimum)	2.5 4.6 9.5 13.5	5/0 5/0 10/0 15/0	5.0 5.0 10.0 15.0	-1.6 -0.51 -1.3 -3.4	mA
Output low level Current IOL (minimum)	0.4 0.5 1.5	5/0 10/0 15/0	5.0 10.0 15.0	0.61 1.3 3.4	mA
I_I Input Current	-	15/0	15.0	±0.1	uA
I_{DD} Power supply current (maximum)	-	5/0 10/0 15/0	5.0 10.0 15.0	0.25 0.5 1.0	uA

Dynamics:

parameter	Test conditions	VDD/V	value		unit
			min	max	
t_{PLH} Output transmission delay time from low level to high level	CL＝50pF RL＝200kΩ tr＝20ns tf＝20ns	5.0 10.0 15.0	--	250 120 90	ns
t_{PHL} Output transmission delay time from high level to low level		5.0 10.0 15.0	--	250 120 90	
tTLH Output transfer from low level to high level conversion time		5.0 10.0 15.0	--	200 100 80	
t_{THL} Output conversion time from high level to low level		5.0 10.0 15.0	--	200 100 80	
CI Input capacitance (Any input terminal)		--	--	7.5	Pf

logic diagram: