Three 2 choose 1 bidirectional analog switch

summary

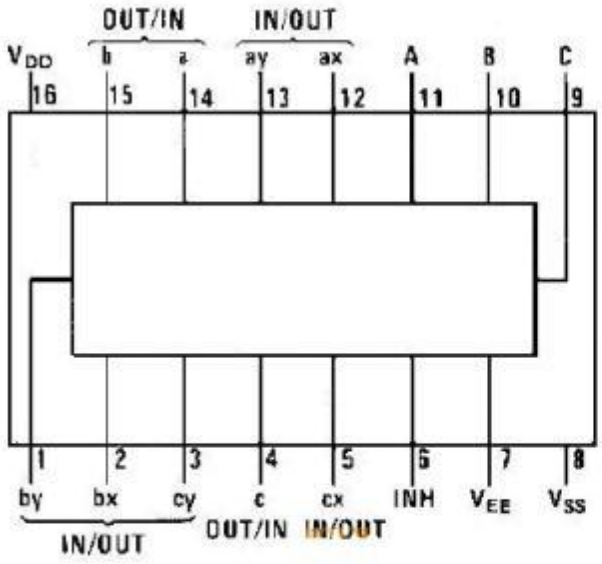
CD 405X series analog switches are designed using digital signals to control multiple modulated / select analog switches with low conduction resistance and very low cut-off leakage current.Digital signals with amplitude value of 4.5 V to 18V can control analog signals with peak value of 18 V.For example, select VDD= + 5V, Vss=0V, VEE = -13.5V, then the digital signal of 0~5V can control-13.5~4.5V analog signal, these switching circuits have very low static power consumption in the entire VDD-VSS and VDD-VEE power range.

CD 4053 is a three sets of two choose 1 two-way analog switch, equivalent to three sets of single knife double throw switches.It has three sets of independent binary digital control inputs A, B, C and INH suppression input, and the binary digital control signal can put any one of the two analog channels into the conduction state.I NH input "1" normally puts all channels of 3 groups 2 select 1 analog switch into off state, and input "0" normally puts all channels of 3 groups 2 select 1 analog switch into on state.

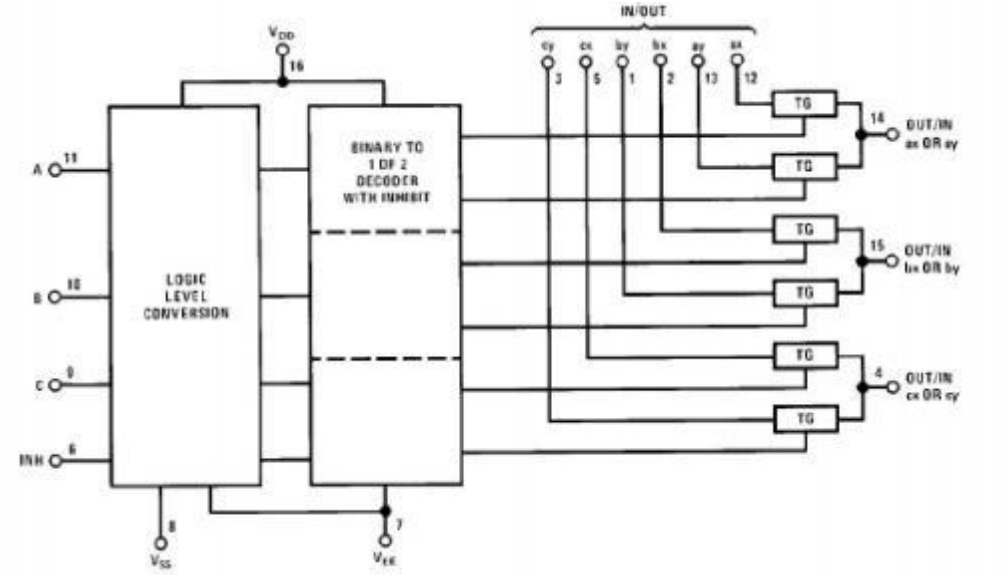
main features

Due to the very wide digital control and transmission of analog signal voltage range: digital 4.5V ~18V, analog 18V;
Due to low on-on resistance: 80 Ω (VDD-VEE =15V, signal greater than 15Vpp);
Due to the very low static voltage power consumption;
Due to high-off resistance;
Switch the analog signal at 18Vpp due to the logic level conversion of the digital address signal from 4.5 V to 18 V;
Because of the built-in binary address decoder.

Foot description (top view)



CD 4053 logic diagram:



truth table:

Input, status		Output, situation
INH	A, or, B, or, C	
0	0	A. ax or bx or cx
0	1	A y or by or cy
1	×	No ne

absolute rating:

number	Described, described		extreme	Single, position
VDD	The DC current, the source voltage		-0.5~+18	V
VI N	Input, voltage		-0.5~VDD +0.5	V
Tstg	Package the operating temperature range		0—70	℃
Ptot	Work, consumption	DI P	700	m W
		S OP	500	m W
T L	welding temperature		260	℃

Recommended working conditions:

Fu, number	Described, described	extreme	Single, position
VDD	The DC current, the source voltage	+5~+15	V
VI N	Input, voltage	0~VDD	V

DC parameters:

symbol	project	condition		+25℃ least value	+25℃ representative value	+25℃ crest value	unit
I DD		VDD=5V				5	uA
		VDD=10V				10	
		VDD=15V				20	
Signal input VIS and output VOS							
R ON	On-on resistance (peak VEE VIS VDD)	R L = 10 KΩ (either channel)	VDD =2.5V VEE = -2.5V or VDD =5V VEE=0V		270	1050	Ω
			VDD=5V VEE = -5V or VDD=10V VEE=0V		120	400	
			VDD =7.5V VEE = -7.5V or VDD=15V VEE=0V		80	240	
△RON	Oon resistance gain between any two channels	R L = 10 KΩ (either channel)	VDD =2.5V VEE = -2.5V or VDD =5V VEE=0V		10		Ω
			VDD=5V VEE = -5V or VDD=10V VEE=0V		10		

			VDD =7.5V VEE = -7.5V or VDD=15V VEE=0V		5		
	Off-state channel leakage current, any channel is in the off-state	VDD =7.5V, VEE=-7.5V O/I=± 7.5V , I /O =0V			±0.01	±50	n A
	Off-state channel leakage current, and all channels are in the off-state	INH =7.5V			±0.02	±200	n A
Control the inputs A, B, C, and INH							
VI L	Low level input Electricity, pressure	VEE=VSS RL =1KΩ All pass, the road is pass form	VDD=5V			1.5	V
			VDD=10V			3.0	
			VDD=15V			4.0	
VI H	high-level input Electricity, pressure	VDD=5V		3.5			V
		VDD=10V		7			
		VDD=15V		11			
I IN	Input, current	VDD=15V VEE=0V	VIN=0V		-10-5	-0.1	uA
			VIN=15V		10-5	0.1	

AC current parameters:

symbol	Item, eye	condition	VD D	least value	representative value	crest value	unit
t PZH t PZL	Transmission delay time from forbidden to signal output (open channel)	VEE =VSS =0V RL =1KΩ CL =50pF	5V		600	1200	n s
			10V		225	450	
			15V		160	320	
t PHZ t PLZ	Transmission delay time from forbidden to signal output	VEE =VSS =0V RL =1KΩ CL =50pF	5V		210	420	n s
			10V		100	200	
			15V		75	150	

	(closed channel)						
C in	Input, capacitance	Control, input			5	7.5	p F
		Signal, input			10	15	
Cout	Output capacitance (total input / output) VEE=VSS=0V		10V		8		p F
C IOS	Bypass, capacitance				0.2		p F

C PO	Power supply dissipation capacitance				70		p F
Signal input VIS and output VOS							
	Sine-wave distortion degree	RL =10KΩ fIS=1KHz VIS =5Vp-p VEE=VSI=0V	10V		0.04		%
	Sine-wave wave frequency response	RL =1KΩ VEE =0V VIS=5Vp-p 20log 10VOS /VIS=-40dB	10V		40		MHz
	Cross-state crosstalk frequency	RL =1KΩ VEE =0V VIS=5Vp-p 20log 10VOS /VIS=-40dB	10V		10		MHz
	Signal crosstalk frequency	RL =1KΩ VEE =0V VIS=5Vp-p 20log 10VOS /VIS=-40dB	10V		3		MHz
t PHL t PLH	Transmission delay of the signal input to the output	VEE =VSS =0V CL =50pF	5V		25	55	n s
			10V		15	35	
			15V		10	25	
Control the inputs A, B, C, and INH							
	Control the input to the signal response	VEE =VSS =0V RL=10KΩ Enter at the end of all channels Square-wave amplitude of 10V	10V		65		m V
t PHL t PLH	propagation delay time From the address to the signal output channel For either on or off	VEE =VSS =0V CL =50pF	5V		500	1000	n s
			10V		160	350	
			15V		120	240	

oscillogram: