Fourteen bit binary serial counter

summary :

CD4060 includes an oscillator and a set of fourteen bit binary serial counters. The structure of the oscillator can be an RC or crystal oscillator circuit. Reset is at high level, the counter is cleared and the oscillator is invalid. All counter bits are the master slave trigger. The falling edge counter of CP1 (and CP0) is counted in binary, and the Schmidt trigger is used on the clock pulse line to unlimited clock rise and fall time.

feature:

Up to 18 power supplies (limit)

Public reset RESET

Input up to 12MHz at 15V

Capable of fully static operation

Buffered inputs and outputs

Schmidt triggered input pulse

Standardized, symmetrical output characteristics

Three levels of 5V, 10V, and 15V

Oscillator characteristics:

RC or crystal oscillator configuration

At 15V, the RC oscillator can reach a frequency of 690kHz for application:

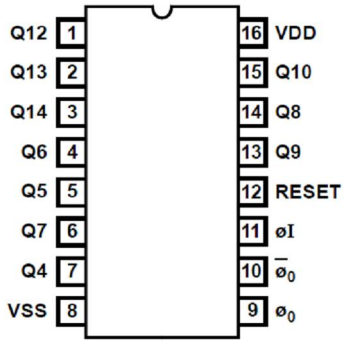
Control Count

Timer

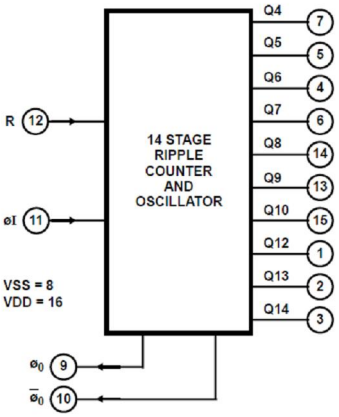
Frequency divider

Delay circuit

Pin arrangement diagram:



Functional Block Diagram:



limit value: (Ta=25° C)

Parameter	symbol	value	UNIT
supply voltage	Vdd	-0.5 to +18	V
Working current	Idd	±10	mA
INPUT VOLTAGE	V_{POL}	-0.5 to VDD +0.5	V
operation temperature	Topr	0 to +70	° C
Storage temperature	Tstg	-65 to +150	° C

Electrical parameter characteristics: (If there are no other regulations: Ta = 25°C;)

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		TEMPERATURE (° C)	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 18V, VIN = VDD or GND		+25	-	10	uA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 18V	+25	-300	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 18V	+25	-	300	nA
Output Voltage	VOL15	VDD = 15V, No Load		+25	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		+25	14.95	-	V
Output Current (Sink) (Excluding pins 9 & 10)	IOL5	VDD = 5V, VOUT = 0.4V		+25	0.53	-	mA
	IOL10	VDD = 10V, VOUT = 0.5V		+25	1.4	-	mA
	IOL15	VDD = 15V, VOUT = 1.5V		+25	3.5	-	mA
Output Current (Source) (Excluding pins 9 & 10)	IOH5A	VDD = 5V, VOUT = 4.6V		+25	-	-0.53	mA
	IOH5B	VDD = 5V, VOUT = 2.5V		+25	-	-1.8	mA
	IOH10	VDD = 10V, VOUT = 9.5V		+25	-	-1.4	mA
	IOH15	VDD = 15V, VOUT = 13.5V		+25	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10uA		+25	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10uA		+25	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		+25	VOH > VDD/2	VOL < VDD/2	V
		VDD = 18V, VIN = VDD or GND					
		VDD = 3V, VIN = VDD or GND					
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		+25	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		+25	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		+25	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		+25	11	-	V

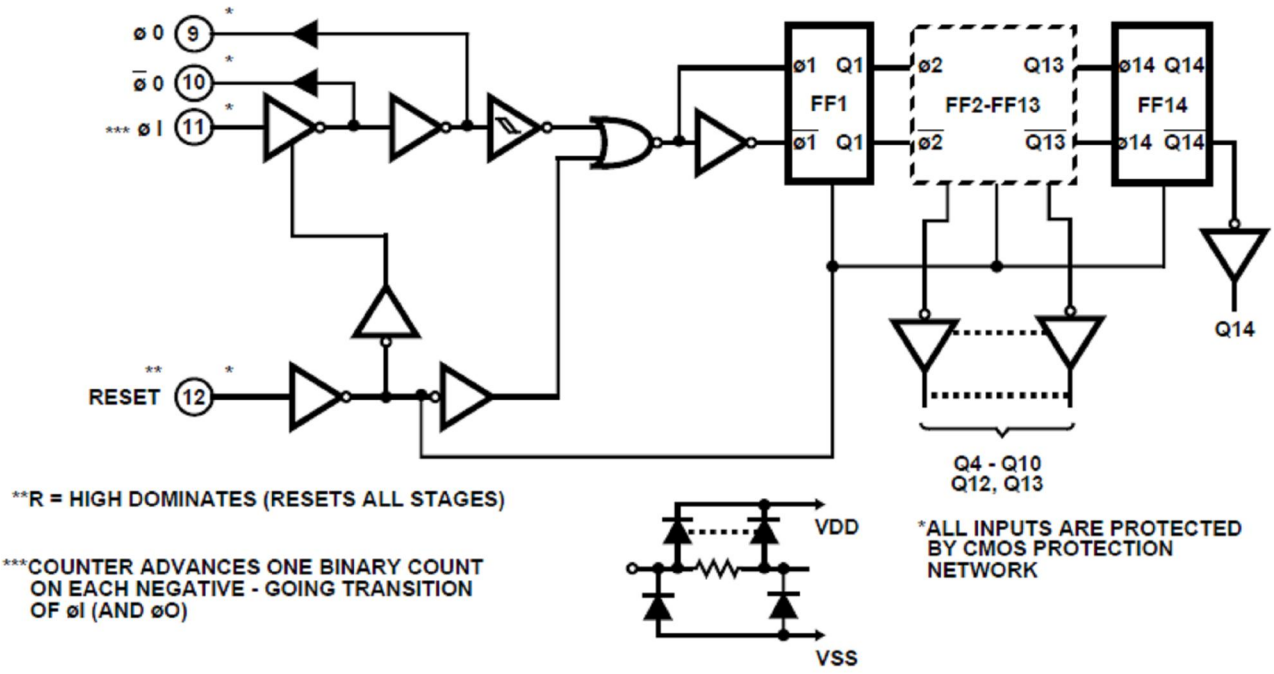
Notes: 1. All voltages referenced to device GND, 100% testing being implemented.

2. Go/No Go test with limits applied to inputs.

3. For accuracy, voltage is measured differentially to VDD. Limitis 0.050V max.

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE (° C)	LIMITS		UNITS
				MIN	MAX	
Drive Current at Pin 9 Oscillator Design	IOL	VDD = 5V, VO = .4V	+25	0.16	-	mA
		VDD = 10V, VO = .5V	+25	0.42	-	mA
		VDD = 15V, VO = 1.5V	+25	-1.0	-	mA
Drive Current at Pin 9 Oscillator Design	IOH	VDD = 5V	+25	-	-.16	mA
		VDD = 10V	+25	-	-.42	mA
		VDD = 15V	+25	-	1.0	mA
Propagation Delay Input Pulse øI to Q4	TPHL1 TPLH1	VDD = 10V	+25	-	300	ns
		VDD = 15V	+25	-	200	ns
Propagation Delay QN to QN + 1	TPHL2 TPLH2	VDD = 10V	+25	-	100	ns
		VDD = 15V	+25	-	80	ns
Propagation Delay RESET	TPHL3	VDD = 10V	+25	-	160	ns
		VDD = 15V	+25	-	100	ns
Transition Time	TTHL TTLH	VDD = 10V	+25	-	100	ns
		VDD = 15V	+25	-	80	ns
Maximum Input Pulse Frequency	FØI	VDD = 10V	+25	8	-	MHz
		VDD = 15V	+25	12	-	MHz
Minimum RESET Pulse Width	TW	VDD = 5V	+25	-	120	ns
		VDD = 10V	+25	-	60	ns
		VDD = 15V	+25	-	40	ns
Minimum Input Pulse Width F = 100kHz	TW	VDD = 5V	+25	-	100	ns
		VDD = 10V	+25	-	40	ns
		VDD = 15V	+25	-	30	ns
RC Operation RX Max	RX	VDD = 5V, CX = 10 F	+25	-	20	MΩ
		VDD = 10V, CX = 50 F	+25	-	20	MΩ
		VDD = 15V, CX = 10 F	+25	-	10	MΩ
RC Operation CX Max	CX	VDD = 5V, RX = 500kΩ	+25	-	1000	F
		VDD = 10V, RX = 300kΩ	+25	-	50	F
		VDD = 15V, RX = 300kΩ	+25	-	50	F
Maximum Oscillator Frequency (Note 4)	RX = 5kΩ CX = 15pF	VDD = 10V	+25	530	810	ns
		VDD = 15V	+25	690	940	ns
RC Operation Variation of Frequency (Unit-to-Unit)	CX = 200pF RS = 560K RX = 50k	VDD = 5V	+25	18	25	kHz
		VDD = 10V	+25	20	26	kHz
		VDD = 15V	+25	21.1	27	kHz
Variation of Frequency with Voltage Change	CX = 200pF RS = 560K	5V to 10V	+25	-	2	kHz
		10V to 15V	+25	-	1	kHz
Input Capacitance	CIN	Any Input	+25	-	7.5	pF

Internal Block Diagram:



characteristic curve:

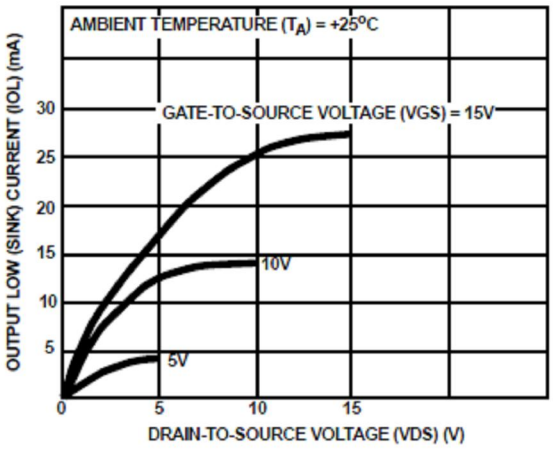


FIGURE 1. TYPICAL N-CHANNEL OUTPUT LOW SINK CURRENT CHARACTERISTICS

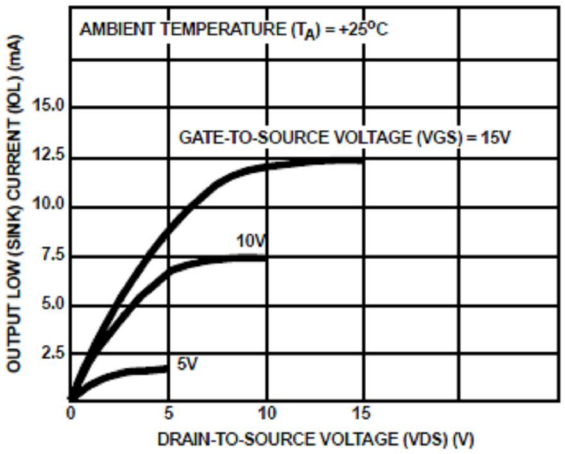


FIGURE 2. MINIMUM N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

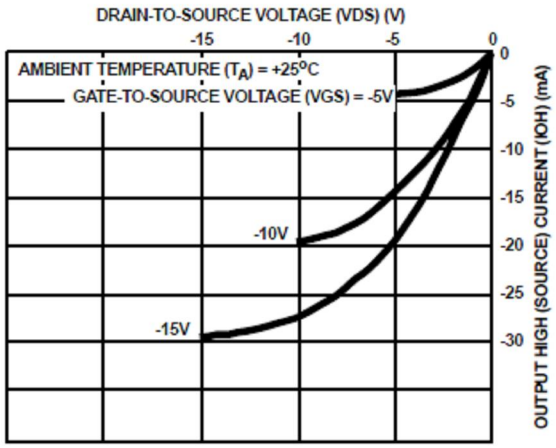


FIGURE 3. TYPICAL P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

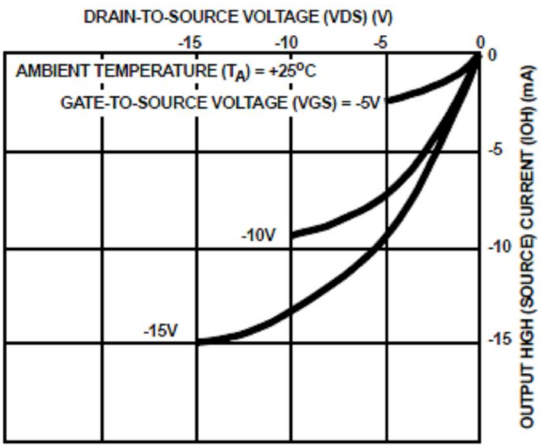


FIGURE 4. MINIMUM P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

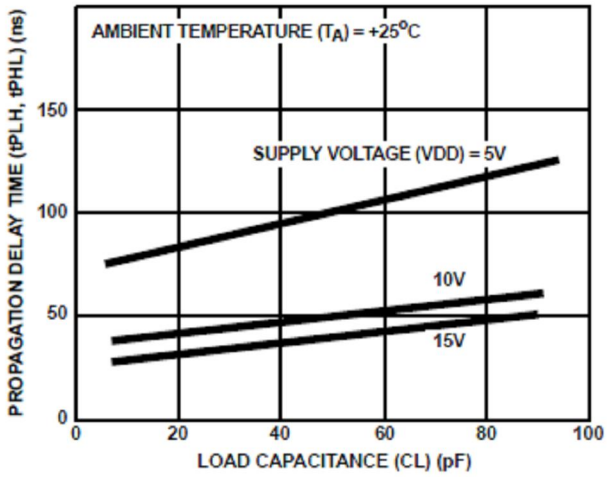


FIGURE 5. TYPICAL PROPAGATION DELAY TIME (QN TO QN+1) AS A FUNCTION OF LOAD CAPACITANCE

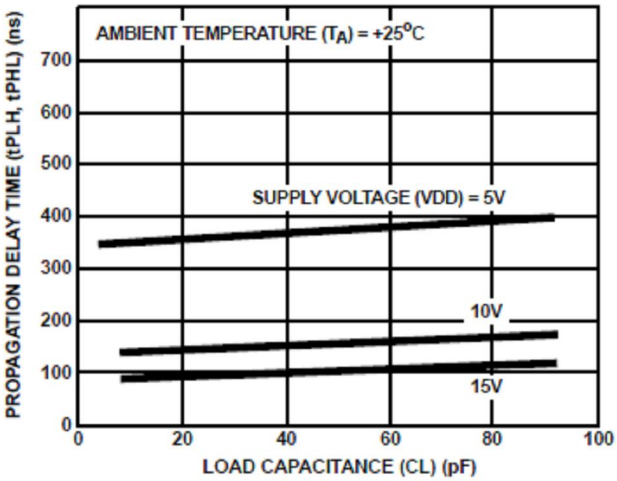


FIGURE 6. TYPICAL PROPAGATION DELAY TIME (Ø1 TO Q4 OUTPUT) AS A FUNCTION OF LOAD CAPACITANCE

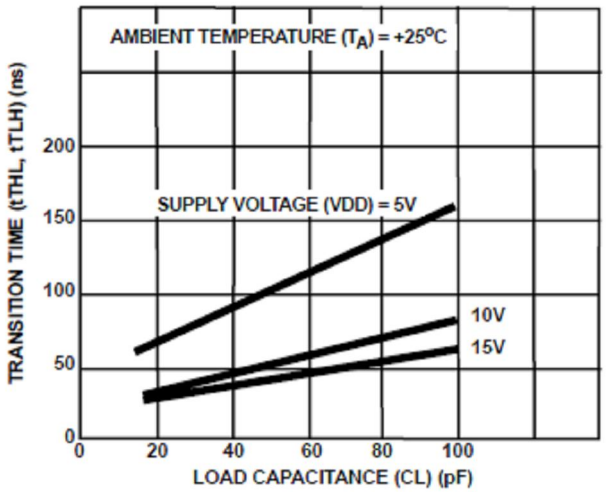


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

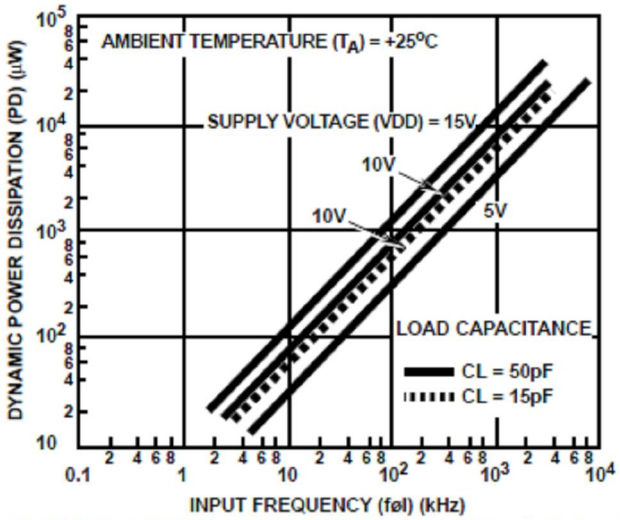


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Test Circuit:

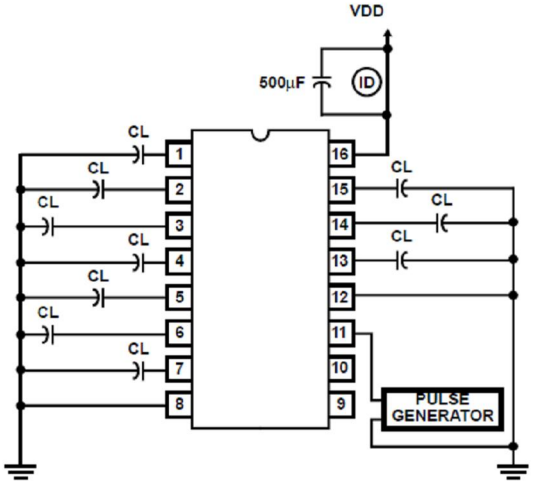


FIGURE 9. DYNAMIC POWER DISSIPATION TEST CIRCUIT

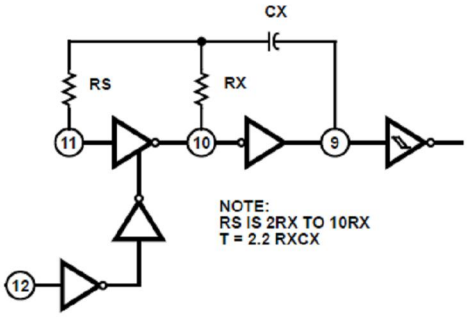
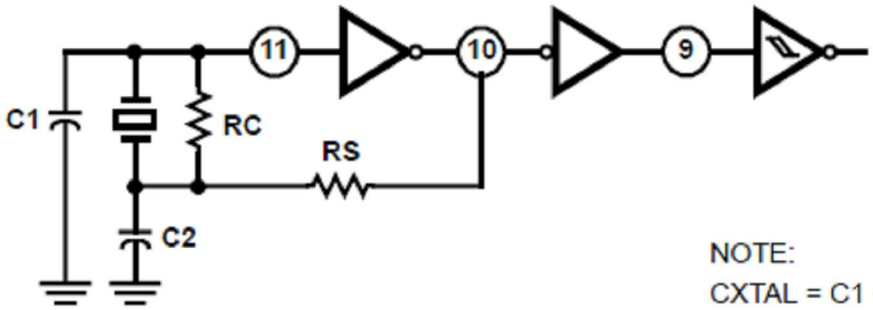


FIGURE 10. TYPICAL RC CIRCUIT



NOTE:
CXTAL = C1 + C2 + CSTRAY
RC = Broader frequency response
RS = Current limiting

FIGURE 11. TYPICAL CRYSTAL CIRCUIT