

Datasheet

APM32F103xC

Arm[®] Cortex[®]-M3 based 32-bit MCU

Version: V1.2

1. Product characteristics

■ Core

- 32-bit Arm® Cortex®-M3 core
- Up to 96MHz working frequency

■ On-chip memory

- Flash: 256KB
- SRAM: 64KB
- SDRAM: 2MB (only applicable to sealed products)

■ Clock

- HSECLK: 4~16MHz external crystal/ceramic oscillator supported
- LSECLK: 32.768KHz crystal/ceramic oscillator supported
- HSICLK: 8MHz RC oscillator calibrated by factory
- LSICLK: 40KHz RC oscillator supported
- PLL: Phase locked loop, 2~16 times of frequency supported

■ Reset and power management

- V_{DD} range: 2.0~3.6V
- V_{DDA} range: 2.0~3.6V
- V_{BAT} range of backup domain power supply: 1.8V~3.6V
- Power-on/power-down reset (POR/PDR) supported
- Programmable power supply voltage detector supported

■ Low-power mode

- Sleep, shutdown and standby modes supported

■ DMA

- Two DMA; DMA1 supports 7 channels and DMA2 supports 5 channels

■ Debugging interface

- JTAG
- SWD

■ I/O

- Up to 80 I/Os
- All I/Os can be mapped to external interrupt vector
- Up to 60 FT input I/Os

■ Communication peripherals

- 2 I2C interfaces (1Mbit/s), all of which support SMBus/PMBus

- 3 USART, 2 UART, support ISO7816, LIN and IrDA functions

- 3 SPI (18Mbps) interfaces, two of which support I2S interface multiplexing

- 2 CAN, USB D and CAN can work independently at the same time

- 1 USB D

■ Analog peripherals

- 3 12-bit ADCs, support up to 16 external channels

- 2 12-bit DACs

■ Timer

- 2 16-bit advanced timers TMR1/8 that can provide 7-channel PWM output, support dead zone generation and braking input functions

- 4 16-bit general-purpose timers TMR2/3/4/5, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions

- 2 16-bit basic timers TMR6/7

- 2 watchdog timers: one independent watchdog IWDG and one window watchdog WWDG

- 1 24-bit autodecrement SysTick Timer

■ RTC

- Support calendar and clock functions

■ 84Bytes backup register

■ CRC computing unit

■ 96-bit unique device ID

Catalog

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2. Product information

See the following table for APM32F103xC product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32F103xC Series Chips

| Product | | APM32F103 | | | |
|------------------------------------|-------------------|--|--------|---------|---------|
| Model | | CCTx | RCTx | VCTx | VCTxS |
| Package | | LQFP48 | LQFP64 | LQFP100 | LQFP100 |
| Core and maximum working frequency | | Arm® 32-bit Cortex®-M3@96MHz | | | |
| Operating voltage | | 2.0~3.6V | | | |
| Flash(KB) | | 256 | | | |
| SRAM(KB) | | 64 | | | |
| SDRAM(MB) | | 0 | | | 2 |
| GPIOs | | 37 | 51 | 80 | 55 |
| EMMC | | 0 | | 1 | 0 |
| Communication interface | USART/UART | 3 | 3/2 | | 3 |
| | SPI/I2S | 3/2 | | | |
| | I2C | 2 | | | 1 |
| | USB D | 1 | | | |
| | CAN | 2 | | | |
| | SDIO | 0 | 1 | | 0 |
| Timer | 16-bit advanced | 1 | 2 | | |
| | 16-bit general | 4 | | | |
| | 16-bit basic | 2 | | | |
| | System tick timer | 1 | | | |
| | Watchdog | 2 | | | |
| Real-time clock | | 1 | | | |
| 12-bit ADC | Unit | 2 | 3 | | |
| | External channel | 10 | 16 | | |
| | Internal channel | 2 | | | |
| 12-bit DAC | Unit | 2 | | | |
| | Channel | 2 | | | |
| Operating temperature | | Ambient temperature: -40°C to 85°C/-40°C to 105°C Junction temperature: -40°C to 105°C/-40°C to 125°C | | | |

Note:

- (1) When x is 6, ambient temperature is: from -40°C to 85°C, and the junction temperature is from -40°C to 105°C.
- (2) When x is 7, ambient temperature is: from -40°C to 105°C, and the junction temperature is from -40°C to 125°C.

3. Pin information

3.1. Pin distribution

Figure 1 Distribution Diagram of APM32F103xCTxS (Sealed SDRAM) Series LQFP100 Pins

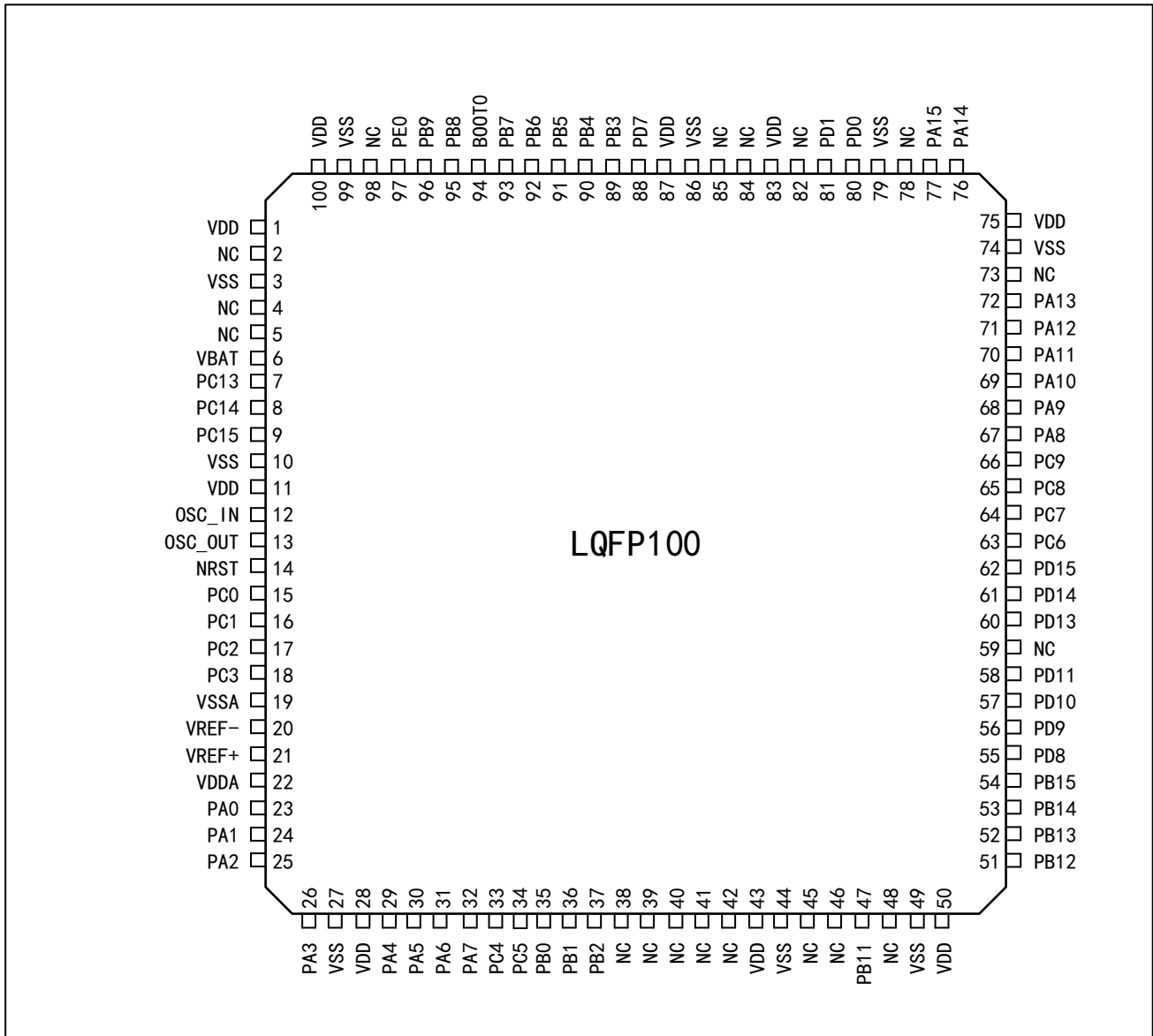


Figure 2 Distribution Diagram of APM32F103xCTx Series LQFP100 Pins

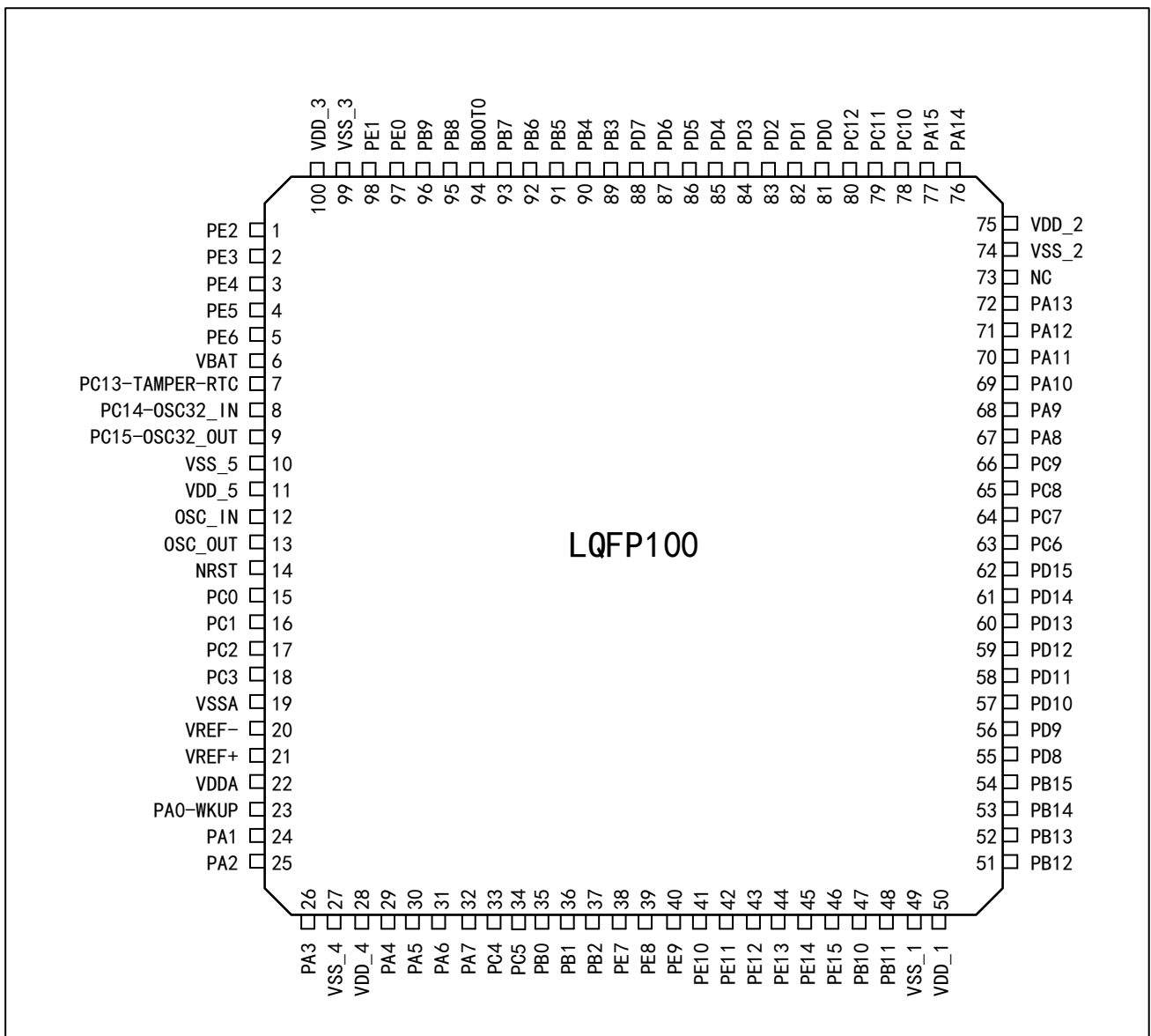


Figure 3 Distribution Diagram of APM32F103xCTx Series LQFP64 Pins

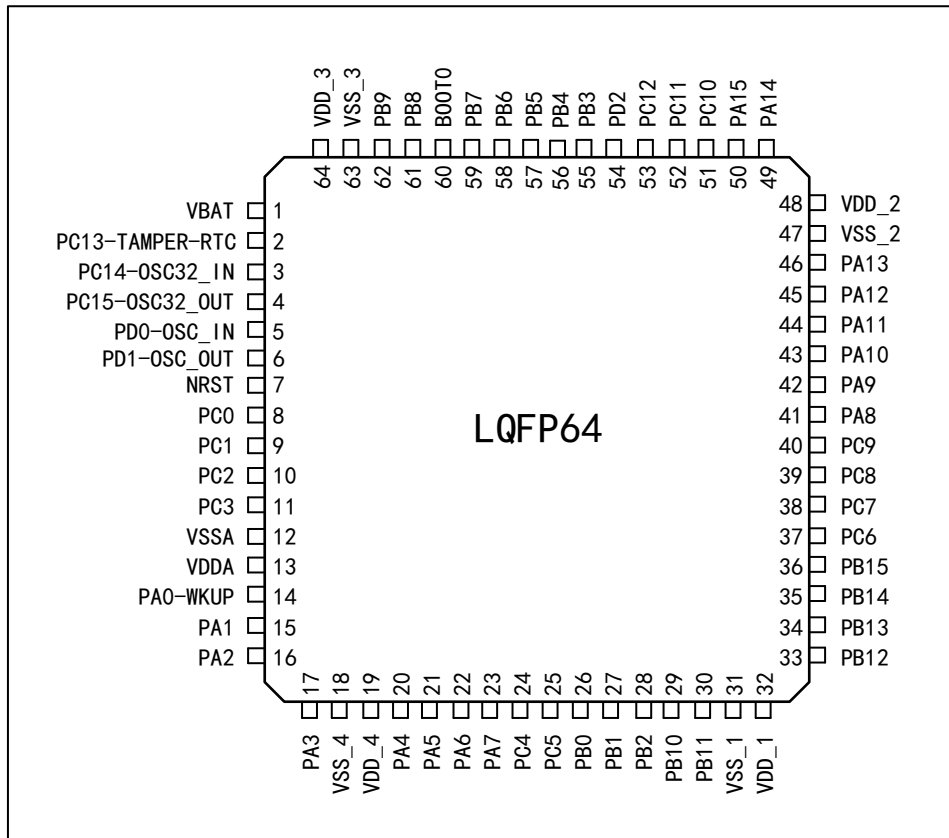
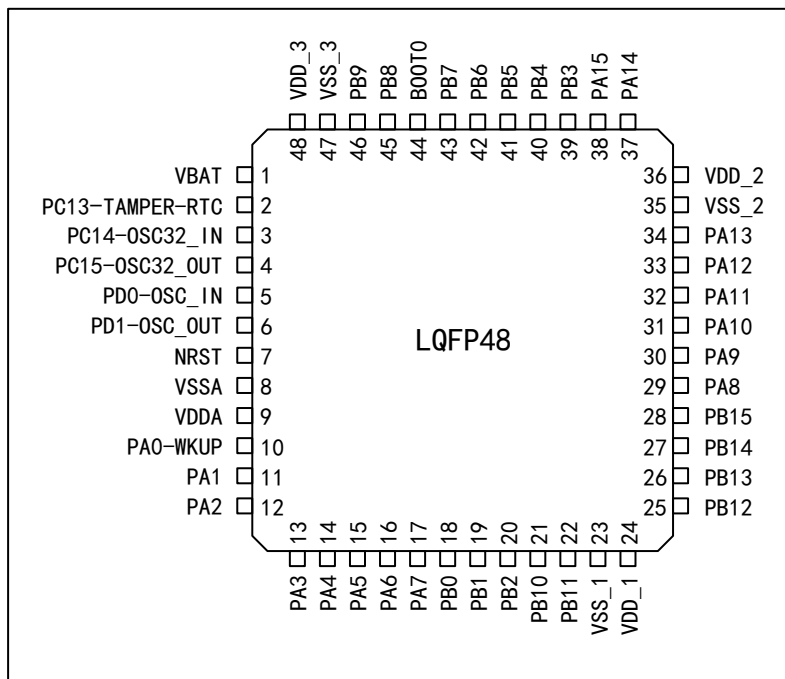


Figure 4 Distribution Diagram of APM32F103xCTx Series LQFP48 Pins



3.2. Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

| Name | | Abbreviation | Definition |
|---------------|-------------------------------|--|--|
| Pin name | | Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name | |
| Pin type | | P | Power pin |
| | | I | Only input pin |
| | | I/O | I/O pin |
| I/O structure | | 5T | FT I/O |
| | | STDA | I/O with 3.3 V tolerance, directly connected to ADC |
| | | STD | I/O with 3.3 V tolerance |
| | | B | Dedicated Boot0 pin |
| | | RST | Bidirectional reset pin with built-in pull-up resistor |
| Note | | Unless otherwise specified in the notes, all I/O is set as floating input during and after reset | |
| Pin function | Default multiplexing function | Function directly selected/enabled through peripheral register | |
| | Remap | Select this function through AFIO remapping register | |

Table 3 Description of APM32F103xCTxS (Sealed SDRAM) by Pin Number

| Name | Type | Structure | Default multiplexing function | Remap | LQFP100 |
|------------------|------|-----------|-------------------------------|-------|---------|
| V _{DD} | P | - | - | - | 1 |
| NC | - | - | - | - | 2 |
| V _{SS} | P | - | - | - | 3 |
| NC | - | - | - | - | 4 |
| NC | - | - | - | - | 5 |
| V _{BAT} | P | - | - | - | 6 |
| PC13 (PC13) | I/O | STD | TAMPER-RTC | - | 7 |
| PC14 (PC14) | I/O | STD | OSC32_IN | - | 8 |
| PC15 (PC15) | I/O | STD | OSC32_OUT | - | 9 |
| V _{SS} | P | - | - | - | 10 |

| Name | Type | Structure | Default multiplexing function | Remap | LQFP100 |
|-------------------|------|-----------|---|-------|---------|
| V _{DD} | P | - | - | - | 11 |
| OSC_IN | I | STD | - | - | 12 |
| OSC_OUT | O | STD | - | - | 13 |
| NRST | I/O | RST | - | - | 14 |
| PC0 | I/O | STDA | ADC123_IN10 | - | 15 |
| PC1 | I/O | STDA | ADC123_IN11 | - | 16 |
| PC2 | I/O | STDA | ADC123_IN12 | - | 17 |
| PC3 | I/O | STDA | ADC123_IN13 | - | 18 |
| V _{SSA} | P | - | - | - | 19 |
| V _{REF-} | P | - | - | - | 20 |
| V _{REF+} | P | - | - | - | 21 |
| V _{DDA} | P | - | - | - | 22 |
| PA0 (PA0) | I/O | STDA | WKUP, USART2_CTS, ADC123_IN0, TMR2_CH1_ETR, TMR5_CH1, TMR8_ETR | - | 23 |
| PA1 | I/O | STDA | USART2_RTS, ADC123_IN1, TMR5_CH2, TMR2_CH2 | - | 24 |
| PA2 | I/O | STDA | USART2_TX, TMR5_CH3, ADC123_IN2, TMR2_CH3 | - | 25 |
| PA3 | I/O | STDA | USART2_RX, TMR5_CH4, ADC123_IN3, TMR2_CH4 | - | 26 |
| V _{SS} | P | - | - | - | 27 |
| V _{DD} | P | - | - | - | 28 |
| PA4 | I/O | STDA | SPI1_NSS, USART2_CK, DAC_OUT1, ADC12_IN4 | - | 29 |

| Name | Type | Structure | Default multiplexing function | Remap | LQFP100 |
|--------------------|------|-----------|--|-----------|---------|
| PA5 | I/O | STDA | SPI1_SCK, DAC_OUT2, ADC12_IN5 | - | 30 |
| PA6 | I/O | STDA | SPI1_MISO, TMR8_BKIN, ADC12_IN6 TMR3_CH1 | TMR1_BKIN | 31 |
| PA7 | I/O | STDA | SPI1_MOSI, TMR8_CH1N, ADC12_IN7, TMR3_CH2 | TMR1_CH1N | 32 |
| PC4 | I/O | STDA | ADC12_IN14 | - | 33 |
| PC5 | I/O | STDA | ADC12_IN15 | - | 34 |
| PB0 | I/O | STDA | ADC12_IN8, TMR3_CH3, TMR8_CH2N | TMR1_CH2N | 35 |
| PB1 | I/O | STDA | ADC12_IN9, TMR3_CH4, TMR8_CH3N | TMR1_CH3N | 36 |
| PB2 (PB2,BOOT1) | I/O | 5T | PB2,BOOT1 | - | 37 |
| NC | - | - | - | - | 38 |
| NC | - | - | - | - | 39 |
| NC | - | - | - | - | 40 |
| NC | - | - | - | - | 41 |
| NC | - | - | - | - | 42 |
| V _{DD} | P | - | - | - | 43 |
| V _{SS} | P | - | - | - | 44 |
| NC | - | - | - | - | 45 |
| NC | - | - | - | - | 46 |
| PB11 (CKE) | I/O | 5T | USART3_TX | TMR2_CH4 | 47 |
| NC | - | - | - | - | 48 |
| V _{SS} | P | - | - | - | 49 |
| V _{DD} | P | - | - | - | 50 |
| PB12 | I/O | 5T | SPI2_NSS, | - | 51 |

| Name | Type | Structure | Default multiplexing function | Remap | LQFP100 |
|------|------|-----------|---|------------|---------|
| | | | I2S2_WS, USART3_CK, TMR1_BKIN, CAN2_RX | | |
| PB13 | I/O | 5T | SPI2_SCK, I2S2_CK, USART3_CTS, TMR1_CH1N, CAN2_TX | - | 52 |
| PB14 | I/O | 5T | SPI2_MISO, TMR1_CH2N, USART3_RTS | - | 53 |
| PB15 | I/O | 5T | SPI2_MOSI, I2S2_SD, TMR1_CH3N | - | 54 |
| PD8 | I/O | 5T | - | USART3_TX | 55 |
| PD9 | I/O | 5T | - | USART3_RX | 56 |
| PD10 | I/O | 5T | - | USART3_CK | 57 |
| PD11 | I/O | 5T | - | USART3_CTS | 58 |
| NC | - | - | - | - | 59 |
| PD13 | I/O | 5T | - | TMR4_CH2 | 60 |
| PD14 | I/O | 5T | - | TMR4_CH3 | 61 |
| PD15 | I/O | 5T | - | TMR4_CH4 | 62 |
| PC6 | I/O | 5T | I2S2_MCK, TMR8_CH1 | TMR3_CH1 | 63 |
| PC7 | I/O | 5T | I2S3_MCK, TMR8_CH2 | TMR3_CH2 | 64 |
| PC8 | I/O | 5T | TMR8_CH3 | TMR3_CH3 | 65 |
| PC9 | I/O | 5T | TMR8_CH4 | TMR3_CH4 | 66 |
| PA8 | I/O | 5T | USART1_CK, TMR1_CH1, MCO | - | 67 |
| PA9 | I/O | 5T | USART1_TX, TMR1_CH2 | - | 68 |
| PA10 | I/O | 5T | USART1_RX, TMR1_CH3 | - | 69 |
| PA11 | I/O | 5T | USART1_CTS, USBDDM, | - | 70 |

| Name | Type | Structure | Default multiplexing function | Remap | LQFP100 |
|----------------------|------|-----------|--|--|---------|
| | | | USB2DM, CAN1_RX, TMR1_CH4 | | |
| PA12 | I/O | 5T | USART1_RTS, USBDDP USB2DP, CAN1_TX, TMR1_ETR | - | 71 |
| PA13 (JTMS,SWDIO) | I/O | 5T | - | - | 72 |
| NC | - | - | - | - | 73 |
| V _{SS} | P | - | - | - | 74 |
| V _{DD} | P | - | - | - | 75 |
| PA14 (JTCK,SWCLK) | I/O | 5T | - | - | 76 |
| PA15 (JTDI) | I/O | 5T | SPI3_NSS, I2S3_WS | TMR2_CH1_ETR, PA15, SPI1_NSS | 77 |
| NC | - | - | - | - | 78 |
| V _{SS} | I/O | 5T | - | - | 79 |
| PD0 | I/O | 5T | - | CAN1_TX | 80 |
| PD1 | I/O | 5T | - | CAN1_RX | 81 |
| NC | - | - | - | - | 82 |
| VDD | I/O | 5T | - | - | 83 |
| NC | - | - | - | - | 84 |
| NC | - | - | - | - | 85 |
| V _{SS} | I/O | 5T | - | - | 86 |
| V _{DD} | I/O | 5T | - | - | 87 |
| PD7 | I/O | 5T | - | USART2_CK | 88 |
| PB3 (JTDO) | I/O | 5T | SPI3_SCK, I2S3_CK | PB3, TRACESWO, TMR2_CH2, SPI1_SCK | 89 |
| PB4 (NJTRST) | I/O | 5T | SPI3_MISO | PB4, TMR3_CH1, SPI1_MISO | 90 |

| Name | Type | Structure | Default multiplexing function | Remap | LQFP100 |
|-----------------|------|-----------|--------------------------------------|------------------------------------|---------|
| PB5 | I/O | STD | SPI3_MOSI, I2C1_SMBAL, I2S3_SD | TMR3_CH2, SPI1_MOSI, CAN2_RX | 91 |
| PB6 | I/O | 5T | I2C1_SCL, I2C3_SCL, TMR4_CH1 | USART1_TX, CAN2_TX | 92 |
| PB7 | I/O | 5T | I2C1_SDA, I2C3_SDA, TMR4_CH2 | USART1_RX | 93 |
| BOOT0 | I | B | - | - | 94 |
| PB8 | I/O | 5T | TMR4_CH3 | I2C1_SCL, I2C3_SCL, CAN1_RX | 95 |
| PB9 | I/O | 5T | TMR4_CH4 | I2C1_SDA, I2C3_SDA, CAN1_TX | 96 |
| PE0 | I/O | 5T | TMR4_ETR | - | 97 |
| NC | - | - | - | - | 98 |
| V _{SS} | P | - | - | - | 99 |
| V _{DD} | P | - | - | - | 100 |

Table 4 Description of APM32F103xCTx by Pin Number

| Name (Function after reset) | Type | Structure | Default multiplexing function | Remap | LQFP48 | LQFP64 | LQFP100 |
|--------------------------------|------|-----------|-------------------------------|-------|--------|--------|---------|
| PE2 | I/O | 5T | TRACECK, SMC_A23 | - | - | - | 1 |
| PE3 | I/O | 5T | TRACED0, SMC_A19 | - | - | - | 2 |
| PE4 | I/O | 5T | TRACED1, SMC_A20 | - | - | - | 3 |
| PE5 | I/O | 5T | TRACED2, SMC_A21 | - | - | - | 4 |
| PE6 | I/O | 5T | TRACED3, SMC_A22 | - | - | - | 5 |
| V _{BAT} | P | - | - | - | 1 | 1 | 6 |
| PC13-TAMPER-RTC (PC13) | I/O | STD | TAMPER_RTC | - | 2 | 2 | 7 |
| PC14-OSC32_IN | I/O | STD | OSC32_IN | - | 3 | 3 | 8 |

| Name (Function after reset) | Type | Structure | Default multiplexing function | Remap | LQFP48 | LQFP64 | LQFP100 |
|--------------------------------|------|-----------|---|-------|--------|--------|---------|
| (PC14) | | | | | | | |
| PC15-OSC32_OUT (PC15) | I/O | STD | OSC32_OUT | - | 4 | 4 | 9 |
| V _{SS_5} | P | - | - | - | - | - | 10 |
| V _{DD_5} | P | - | - | - | - | - | 11 |
| OSC_IN | I | STD | - | PD0 | 5 | 5 | 12 |
| OSC_OUT | O | STD | - | PD1 | 6 | 6 | 13 |
| NRST | I/O | RST | - | - | 7 | 7 | 14 |
| PC0 | I/O | STDA | ADC123_IN10, DMC_WE | - | - | 8 | 15 |
| PC1 | I/O | STDA | ADC123_IN11, DMC_RAS | - | - | 9 | 16 |
| PC2 | I/O | STDA | ADC123_IN12, DMC_CS | - | - | 10 | 17 |
| PC3 | I/O | STDA | ADC123_IN13, DMC_CKE | - | - | 11 | 18 |
| V _{SSA} | P | - | - | - | 8 | 12 | 19 |
| V _{REF-} | P | - | - | - | - | - | 20 |
| V _{REF+} | P | - | - | - | - | - | 21 |
| V _{DDA} | P | - | - | - | 9 | 13 | 22 |
| PA0-WKUP (PA0) | I/O | STDA | WKUP, USART2_CTS, ADC123_IN0, TMR2_CH1_ETR, TMR5_CH1, TMR8_ETR | - | 10 | 14 | 23 |
| PA1 | I/O | STDA | USART2_RTS, ADC123_IN1, TMR5_CH2, TMR2_CH2 | - | 11 | 15 | 24 |
| PA2 | I/O | STDA | USART2_TX, TMR5_CH3, ADC123_IN2, TMR2_CH3 | - | 12 | 16 | 25 |
| PA3 | I/O | STDA | USART2_RX, TMR5_CH4, ADC123_IN3, TMR2_CH4 | - | 13 | 17 | 26 |

| Name (Function after reset) | Type | Structure | Default multiplexing function | Remap | LQFP48 | LQFP64 | LQFP100 |
|--------------------------------|------|-----------|--|-----------|--------|--------|---------|
| V _{SS_4} | P | - | - | - | - | 18 | 27 |
| V _{DD_4} | P | - | - | - | - | 19 | 28 |
| PA4 | I/O | STDA | SPI1_NSS, USART2_CK, DAC_OUT1, ADC12_IN4 | - | 14 | 20 | 29 |
| PA5 | I/O | STDA | SPI1_SCK, DAC_OUT2, ADC12_IN5 | - | 15 | 21 | 30 |
| PA6 | I/O | STDA | SPI1_MISO, TMR8_BKIN, ADC12_IN6 TMR3_CH1 | TMR1_BKIN | 16 | 22 | 31 |
| PA7 | I/O | STDA | SPI1_MOSI, TMR8_CH1N, ADC12_IN7, TMR3_CH2 | TMR1_CH1N | 17 | 23 | 32 |
| PC4 | I/O | STDA | ADC12_IN14 | - | - | 24 | 33 |
| PC5 | I/O | STDA | ADC12_IN15 | - | - | 25 | 34 |
| PB0 | I/O | STDA | ADC12_IN8, TMR3_CH3, TMR8_CH2N | TMR1_CH2N | 18 | 26 | 35 |
| PB1 | I/O | STDA | ADC12_IN9, TMR3_CH4, TMR8_CH3N | TMR1_CH3N | 19 | 27 | 36 |
| PB2 (PB2,BOOT1) | I/O | 5T | - | - | 20 | 28 | 37 |
| PE7 | I/O | 5T | SMC_D4, DMC_D4 | TMR1_ETR | - | - | 38 |
| PE8 | I/O | 5T | SMC_D5, DMC_D5 | TMR1_CH1N | - | - | 39 |
| PE9 | I/O | 5T | SMC_D6, DMC_D6 | TMR1_CH1 | - | - | 40 |
| PE10 | I/O | 5T | SMC_D7, DMC_D7 | TMR1_CH2N | - | - | 41 |
| PE11 | I/O | 5T | SMC_D8, DMC_D8 | TMR1_CH2 | - | - | 42 |
| PE12 | I/O | 5T | SMC_D9, DMC_D9 | TMR1_CH3N | - | - | 43 |

| Name (Function after reset) | Type | Structure | Default multiplexing function | Remap | LQFP48 | LQFP64 | LQFP100 |
|--------------------------------|------|-----------|---|------------|--------|--------|---------|
| PE13 | I/O | 5T | SMC_D10, DMC_D10 | TMR1_CH3 | - | - | 44 |
| PE14 | I/O | 5T | SMC_D11, DMC_D11 | TMR1_CH4 | - | - | 45 |
| PE15 | I/O | 5T | SMC_D12, DMC_D12 | TMR1_BKIN | - | - | 46 |
| PB10 | I/O | 5T | I2C2_SCL, I2C4_SCL, USART3_TX | TMR2_CH3 | 21 | 29 | 47 |
| PB11 | I/O | 5T | I2C2_SDA, I2C4_SDA, USART3_RX | TMR2_CH4 | 22 | 30 | 48 |
| V _{SS_1} | P | - | - | - | 23 | 31 | 49 |
| V _{DD_1} | P | - | - | - | 24 | 32 | 50 |
| PB12 | I/O | 5T | SPI2_NSS, I2S2_WS, I2C2_SMBAL, USART3_CK, TMR1_BKIN, CAN2_RX | - | 25 | 33 | 51 |
| PB13 | I/O | 5T | SPI2_SCK, I2S2_CK, USART3_CTS, TMR1_CH1N, CAN2_TX | - | 26 | 34 | 52 |
| PB14 | I/O | 5T | SPI2_MISO, TMR1_CH2N, USART3_RTS | - | 27 | 35 | 53 |
| PB15 | I/O | 5T | SPI2_MOSI, I2S2_SD, TMR1_CH3N | - | 28 | 36 | 54 |
| PD8 | I/O | 5T | SMC_D13, DMC_D13 | USART3_TX | - | - | 55 |
| PD9 | I/O | 5T | SMC_D14, DMC_D14 | USART3_RX | - | - | 56 |
| PD10 | I/O | 5T | SMC_D15, DMC_D15 | USART3_CK | - | - | 57 |
| PD11 | I/O | 5T | SMC_A16, DMC_BA0 | USART3_CTS | - | - | 58 |
| PD12 | I/O | 5T | SMC_A17, | TMR4_CH1, | - | - | 59 |

| Name (Function after reset) | Type | Structure | Default multiplexing function | Remap | LQFP48 | LQFP64 | LQFP100 |
|--------------------------------|------|-----------|--|------------|--------|--------|---------|
| | | | DMC_BA1 | USART3_RTS | | | |
| PD13 | I/O | 5T | SMC_A18 | TMR4_CH2 | - | - | 60 |
| PD14 | I/O | 5T | SMC_D0, DMC_D0 | TMR4_CH3 | - | - | 61 |
| PD15 | I/O | 5T | SMC_D1, DMC_D2 | TMR4_CH4 | - | - | 62 |
| PC6 | I/O | 5T | I2S2_MCK, TMR8_CH1, SDIO_D6 | TMR3_CH1 | - | 37 | 63 |
| PC7 | I/O | 5T | I2S3_MCK, TMR8_CH2, SDIO_D7 | TMR3_CH2 | - | 38 | 64 |
| PC8 | I/O | 5T | TMR8_CH3, SDIO_D0 | TMR3_CH3 | - | 39 | 65 |
| PC9 | I/O | 5T | TMR8_CH4, SDIO_D1 | TMR3_CH4 | - | 40 | 66 |
| PA8 | I/O | 5T | USART1_CK, TMR1_CH1, MCO | - | 29 | 41 | 67 |
| PA9 | I/O | 5T | USART1_TX, TMR1_CH2 | - | 30 | 42 | 68 |
| PA10 | I/O | 5T | USART1_RX, TMR1_CH3 | - | 31 | 43 | 69 |
| PA11 | I/O | 5T | USART1_CTS, USBDDM, USBD2DM, CAN1_RX, TMR1_CH4 | - | 32 | 44 | 70 |
| PA12 | I/O | 5T | USART1_RTS, USBDDP USBD2DP, CAN1_TX, TMR1_ETR | - | 33 | 45 | 71 |
| PA13 (JTMS,SWDIO) | I/O | 5T | - | PA13 | 34 | 46 | 72 |
| NC | - | - | Not connected | - | - | - | 73 |
| V _{SS_2} | P | - | - | - | 35 | 47 | 74 |
| V _{DD_2} | P | - | - | - | 36 | 48 | 75 |
| PA14 | I/O | 5T | - | PA14 | 37 | 49 | 76 |

| Name (Function after reset) | Type | Structure | Default multiplexing function | Remap | LQFP48 | LQFP64 | LQFP100 |
|--------------------------------|------|-----------|--------------------------------------|--|--------|--------|---------|
| (JTCK,SWCLK) | | | | | | | |
| PA15 (JTDI) | I/O | 5T | SPI3_NSS, I2S3_WS | TMR2_CH1_ETR, PA15, SPI1_NSS | 38 | 50 | 77 |
| PC10 | I/O | 5T | UART4_TX, SDIO_D2 | USART3_TX | - | 51 | 78 |
| PC11 | I/O | 5T | UART4_RX, SDIO_D3 | USART3_RX | - | 52 | 79 |
| PC12 | I/O | 5T | UART5_TX, SDIO_CK | USART3_CK | - | 53 | 80 |
| PD0 (OSC_IN) | I/O | 5T | SMC_D2, DMC_D2 | CAN_RX | - | - | 81 |
| PD1 (OSC_OUT) | I/O | 5T | SMC_D3, DMC_D3 | CAN_TX | - | - | 82 |
| PD2 | I/O | 5T | TMR3_ETR, UART5_RX, SDIO_CMD | - | - | 54 | 83 |
| PD3 | I/O | 5T | SMC_CLK | USART2_CTS | - | - | 84 |
| PD4 | I/O | 5T | SMC_NOE | USART2_RTS | - | - | 85 |
| PD5 | I/O | 5T | SMC_NWE | USART2_TX | - | - | 86 |
| PD6 | I/O | 5T | SMC_NWAIT | USART2_RX | - | - | 87 |
| PD7 | I/O | 5T | SMC_NE1, SMC_NCE2 | USART2_CK | - | - | 88 |
| PB3 (JTDO) | I/O | 5T | SPI3_SCK, I2S3_CK | PB3, TRACESWO, TMR2_CH2, SPI1_SCK | 39 | 55 | 89 |
| PB4 (NJTRST) | I/O | 5T | SPI3_MISO | PB4, TMR3_CH1, SPI1_MISO | 40 | 56 | 90 |
| PB5 | I/O | STD | I2C1_SMBAL, SPI3_MOSI, I2S3_SD | TMR3_CH2, SPI1_MOSI, CAN2_RX | 41 | 57 | 91 |
| PB6 | I/O | 5T | I2C1_SCL, I2C3_SCL, TMR4_CH1 | USART1_TX, CAN2_TX | 42 | 58 | 92 |
| PB7 | I/O | 5T | I2C1_SDA, I2C3_SDA, SMC_NADV, | USART1_RX | 43 | 59 | 93 |

| Name (Function after reset) | Type | Structure | Default multiplexing function | Remap | LQFP48 | LQFP64 | LQFP100 |
|--------------------------------|------|-----------|-------------------------------------|-----------------------------------|--------|--------|---------|
| | | | TMR4_CH2 | | | | |
| BOOT0 | I | B | - | - | 44 | 60 | 94 |
| PB8 | I/O | 5T | TMR4_CH3, SDIO_D4 | I2C1_SCL, I2C3_SCL, CAN1_RX | 45 | 61 | 95 |
| PB9 | I/O | 5T | TMR4_CH4, SDIO_D5 | I2C1_SDA, I2C3_SDA, CAN1_TX | 46 | 62 | 96 |
| PE0 | I/O | 5T | TMR4_ETR, SMC_NBL0, DMC_LDQM | - | - | - | 97 |
| PE1 | I/O | 5T | SMC_NBL1, DMC_UDQM | - | - | - | 98 |
| V _{SS_3} | P | - | - | - | 47 | 63 | 99 |
| V _{DD_3} | P | - | - | - | 48 | 64 | 100 |

Note:

(1) PC13, PC14 and PC15 are powered through the power switch. Since the switch only sinks limited current (3mA), the use of GPIO from PC13 to PC15 in output mode is limited:

- ① The speed shall not exceed 2MHz when the heavy load is 30pF;
- ② Not used for current source (e.g. driving LED).

(2) For Pin 5 and Pin 6 of LQFP64 and LQFP48 package, the default configuration after the chip is reset is OSC_IN and OSC_OUT, the software can reset these two pins with PD0 and PD1 functions; for LQFP100 package, PD0 and PD1 are inherent function pins.

4. Functional description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32F103xC series products; for information about the Arm® Cortex®-M3 core, please refer to the Arm®Cortex®-M3 technical reference manual, which can be downloaded from ARM's website.

4.1. System architecture

4.1.1. System block diagram

Figure 5APM32F103xCTx System Block Diagram

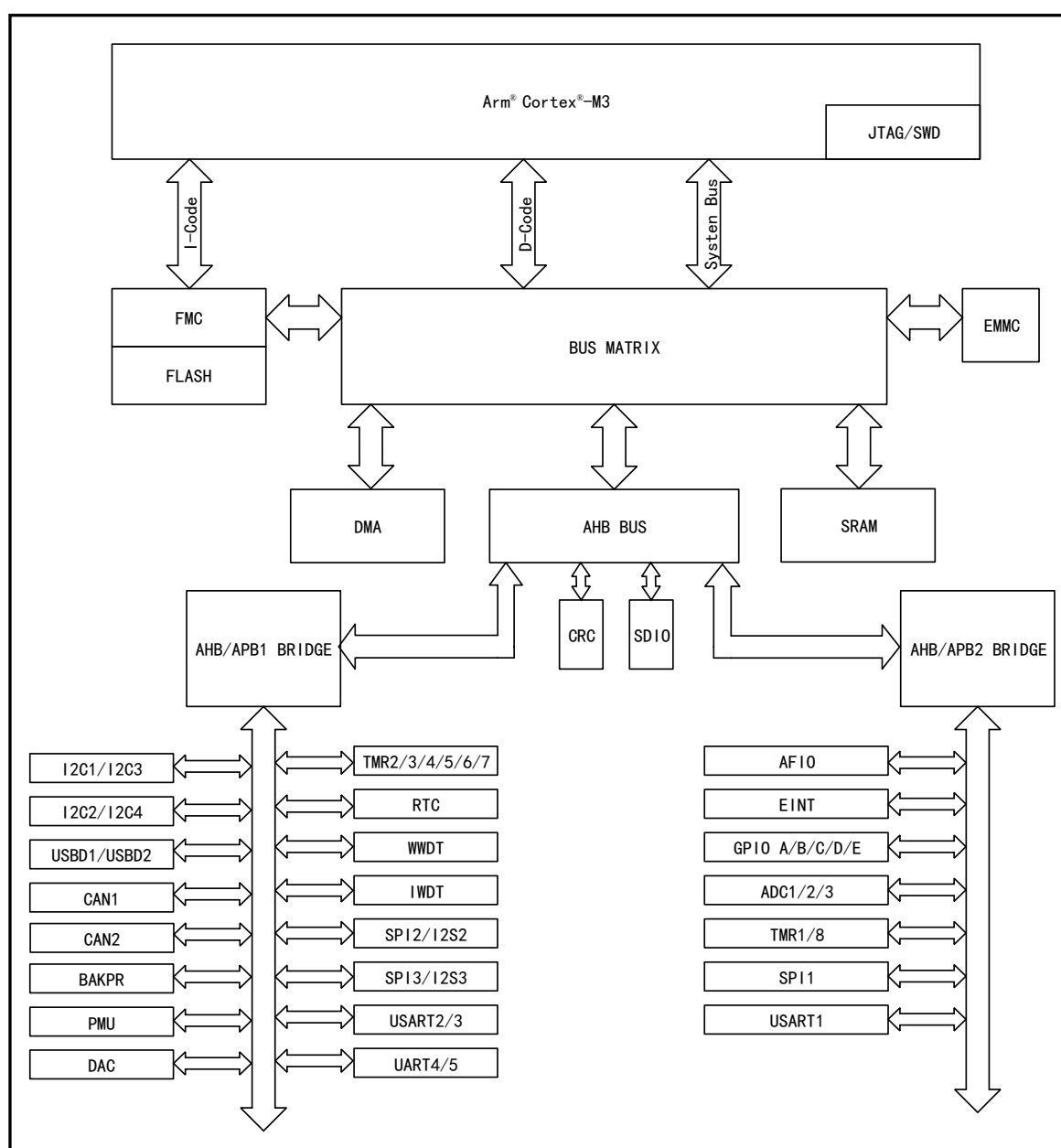
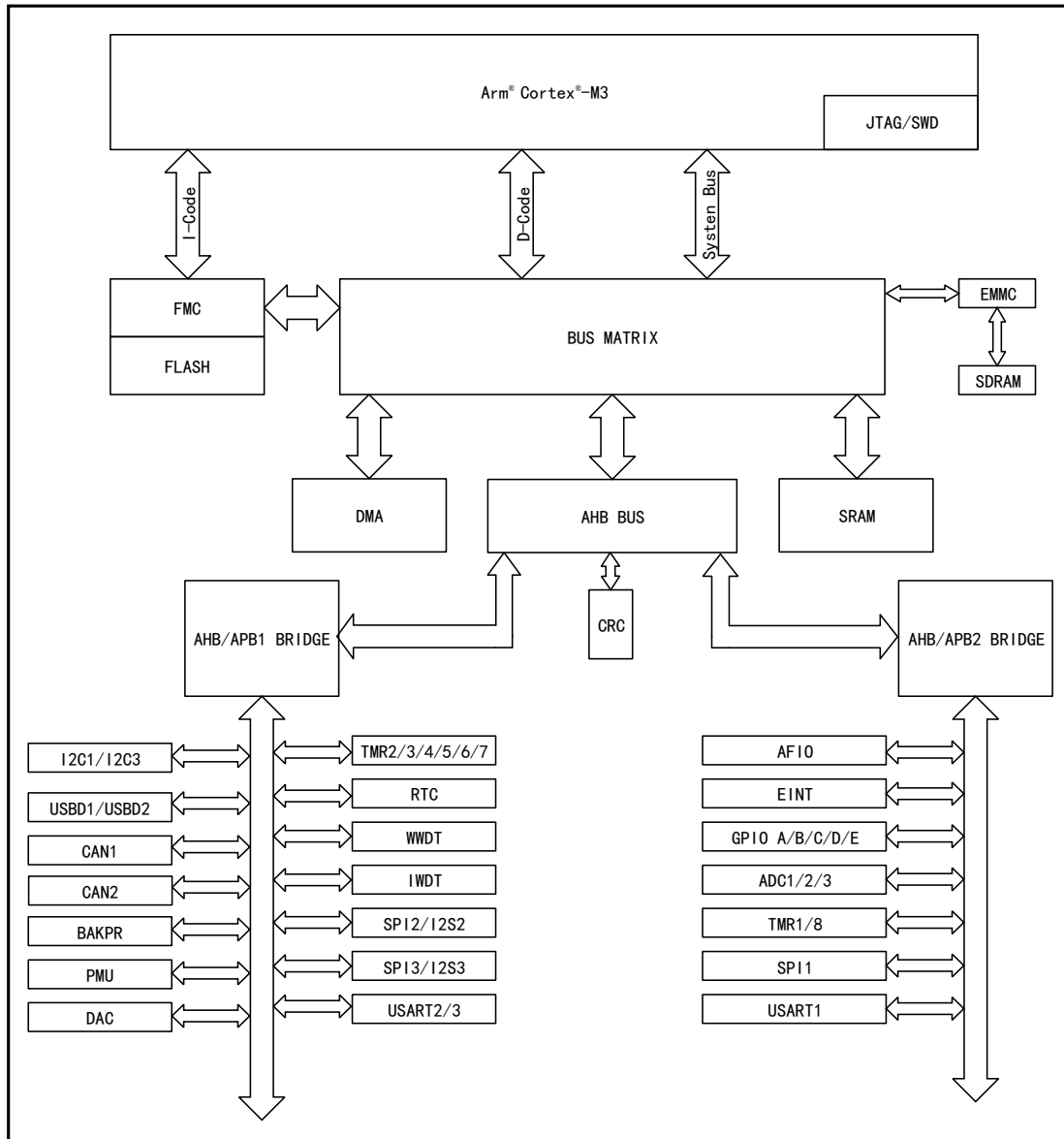


Figure 6 APM32F103xCTxS (Sealed SDRAM) System Block Diagram



4.1.2. Address mapping

Figure 7 PM32F103xCTx Series Address Mapping Diagram

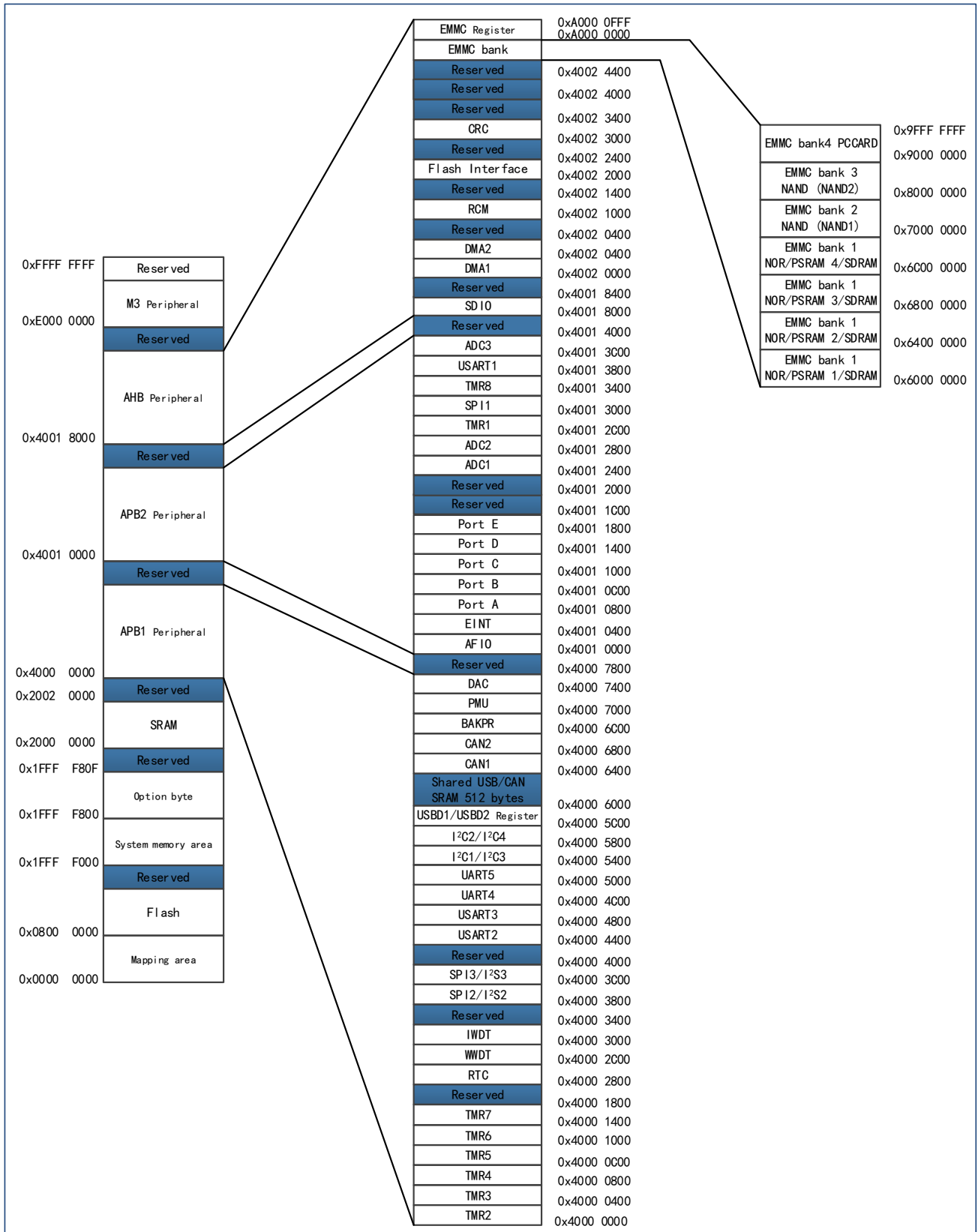
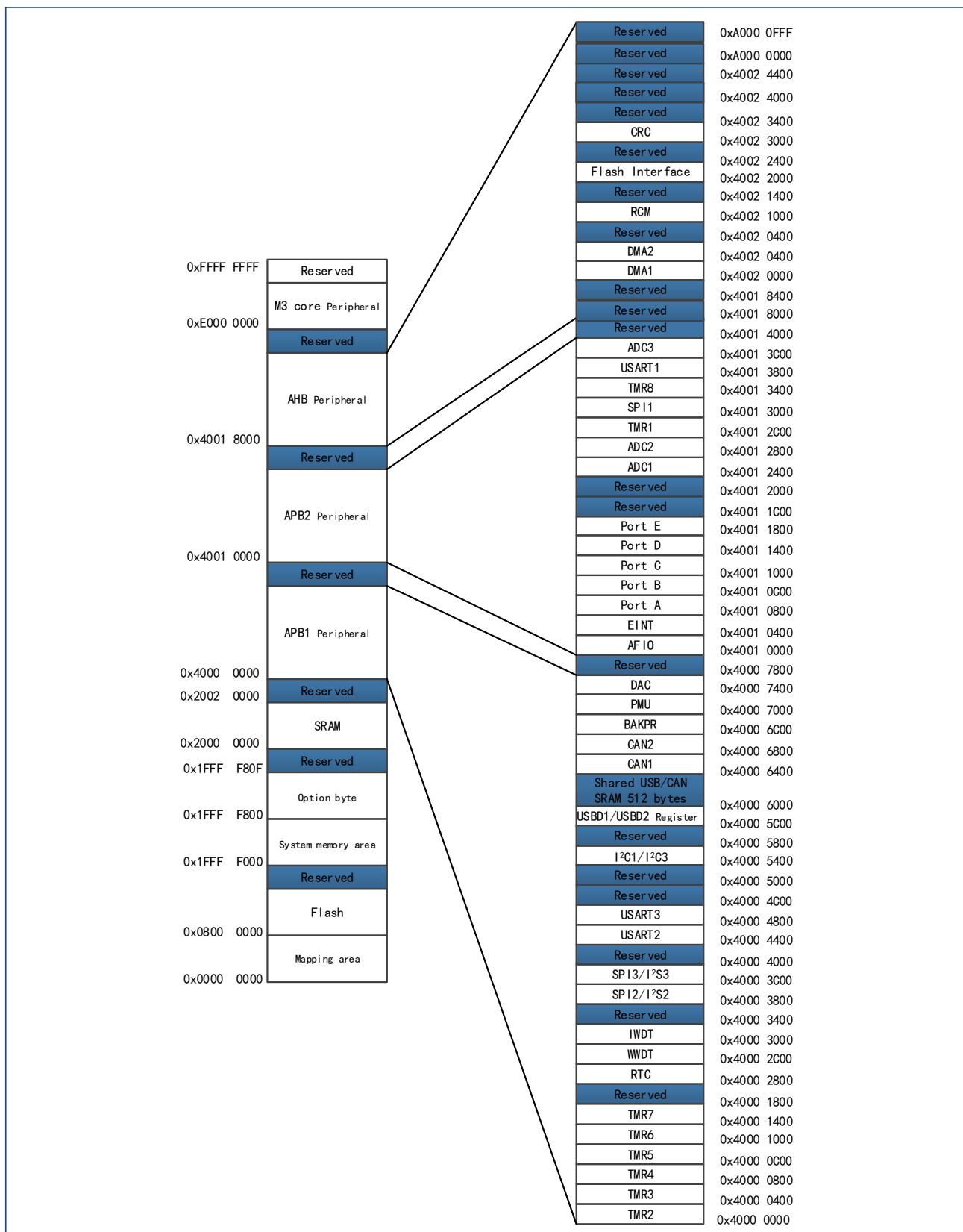


Figure 8 APM32F103xCTxS (Sealed SDRAM) Series Address Mapping Diagram



4.1.3. Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

The user can use USART interface to reprogram the user Flash if boot from BootLoader.

4.2. Core

The core of APM32F103xC is Arm® Cortex®-M3. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all ARM tools and software.

4.3. Interrupt controller

4.3.1. Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) that can handle up to 60 maskable interrupt channels (not including 16 interrupt lines of Cortex®-M3) and 16 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2. External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 19 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

4.4. On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program and cannot be erased.

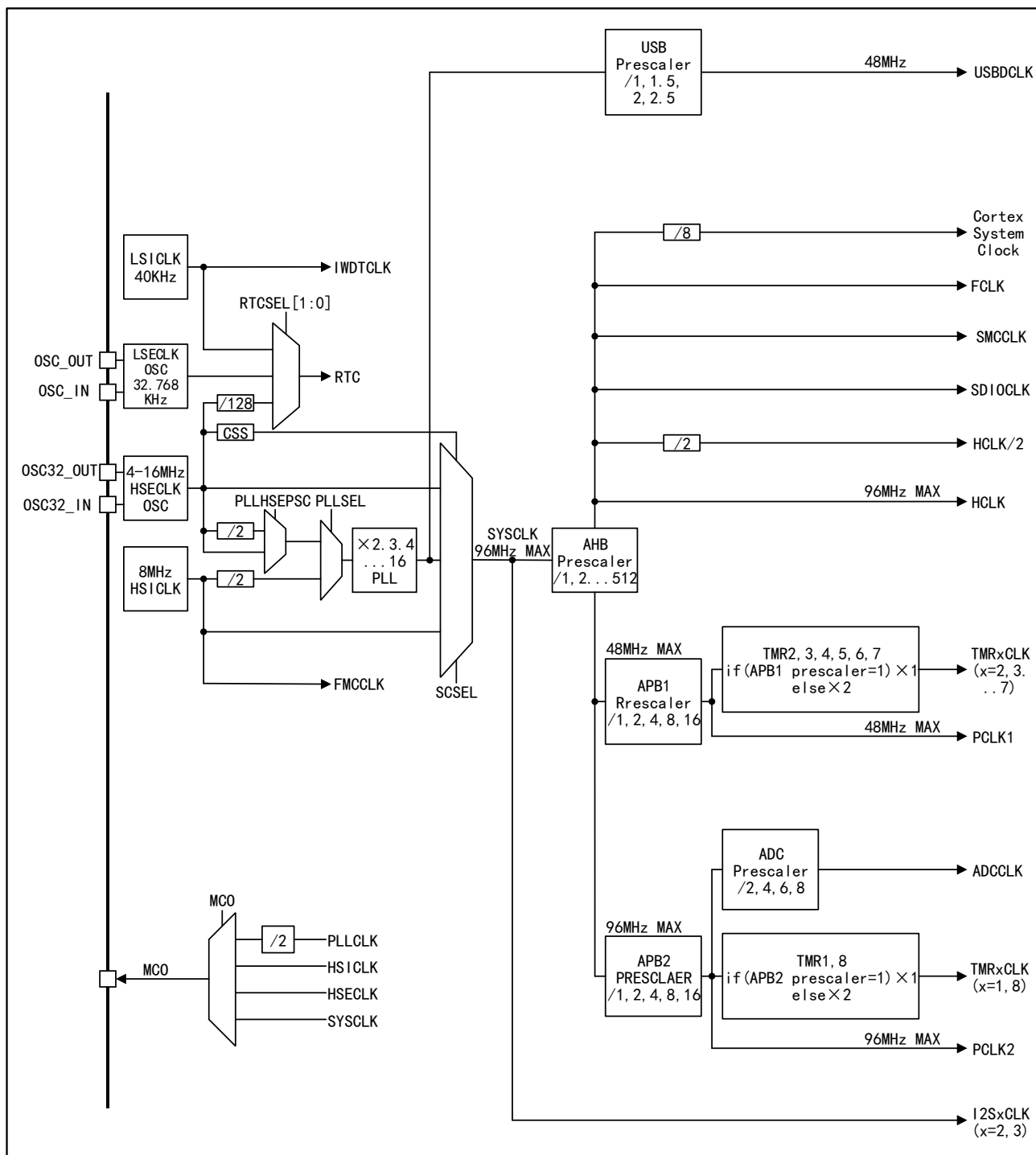
Table 5 On-chip Memory Area

| Memory | Maximum capacity | Function |
|--------------------|------------------|--|
| Main memory area | 256 KB | Store user programs and data. |
| SRAM | 64 KB | CPU can access at 0 waiting cycle (read/write). |
| System memory area | 2KB | Store BootLoader, 96-bit unique device ID, and main memory area capacity information |
| Option byte | 16Bytes | Configure main memory area read-write protection and MCU working mode |
| SDRAM | 2MB | Store a large amount of temporary data, data cache, read (only applicable to APM32F103xCTxS) |

4.5. Clock

Clock tree of APM32F103xC is shown in the figure below:

Figure 9 APM32F103xC Clock Tree



4.5.1. Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK; clock source is divided into internal clock and external clock according to the chip inside/outside; the internal clock includes HSICLK and LSICLK, and the external clock includes HSECLK and LSECLK, among which HSICLK is calibrated by the factory to $\pm 1\%$ accuracy.

4.5.2. System clock

HSICLK, HSICLK48, PLLCLK and HSECLK can be selected as system clock; the clock source of PLLCLK can be one of HSICLK, HSICLK48 and HSECLK; the required system clock can be

obtained by configuring PLL clock multiplier factor and frequency dividing coefficient.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock by himself. When HSECLK failure is detected, the system will automatically switch to the HSICLK, and if an interrupt is enabled, the software can receive the related interrupt.

4.5.3. Bus clock

AHB, APB1 and APB2 are built in. The clock source of AHB is SYSCLK, and the clock source of APB1 and APB2 is AHB_CLK; the required clock can be obtained by configuring the frequency dividing coefficient. The maximum frequency of AHB and high-speed APB2 is 96MHz, and the maximum frequency of APB1 is 48MHz.

4.6. Reset and power management

4.6.1. Power supply scheme

Table 5 Power Supply Scheme

| Name | Voltage range | Instruction |
|------------------------------------|---------------|--|
| V _{DD} | 2.0~3.6V | I/Os (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V _{DD} pin. |
| V _{DDA} /V _{SSA} | 2.0~3.6V | Power supply of ADC, DAC, reset module, RC oscillator and PLL analog part; when ADC or DAC is used, V _{DDA} shall not be less than 2.4V; V _{DDA} and V _{SSA} must be connected to V _{DD} and V _{SS} . |
| V _{BAT} | 1.8~3.6V | When V _{DD} is closed, RTC, external 32KHz oscillator and backup register are supplied through internal power switch. |

4.6.2. Voltage regulator

Table 6 Regulator Operating Mode

| Name | Instruction |
|----------------------|--|
| Master mode (MR) | Used in run mode |
| Low-power mode (LPR) | Used in shutdown mode |
| Power-down mode | Used in standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost. |

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3. Power supply voltage monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value (V_{POR/PDR}), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage regulator (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

4.7. Low-power mode

APM32F103xC supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual application requirements.

Table 7 Low Power Consumption Mode

| Mode | Instruction |
|---------------|---|
| Sleep mode | The core stops working, all peripherals are working, and it can be woken up through interrupts/events |
| Shutdown mode | Under the condition that SRAM and register data are not lost, the shutdown mode can achieve the lowest power consumption; The clock of the internal 1.5V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be prohibited, and the voltage regulator can be configured in normal mode or low power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC and USBDM. |
| Standby mode | The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.5V power supply modules are powered off, HSECLK crystal resonator, HSICLK and PLL clocks are turned off, SRAM and register data disappear, RTC area and backup register contents remain, and standby circuit still works; The external reset signal on NRST, IWDG reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode. |

4.8. DMA

2 built-in DMAs; DMA1 supports 7 channels and DMA2 supports 5 channels. Each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, and TMRx. Four levels of DMA channel priority can be configured. Support "memory→memory, memory→peripheral, peripheral→memory" transfer of data (the memory includes Flash、SRAM、SDRAM)

4.9. GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input、output. The general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speed of 2MHz, 10MHz and 50MHz can be configured; the higher the speed is, the greater the power and the noise will be.

4.10. Communication peripherals

4.10.1. USART/UART

Up to 5 universal synchronous/asynchronous transmitter receivers are built in the chip. The USART1 interface can communicate at a rate of 4.5Mbit/s, while other USART/UART interfaces can communicate at a rate of 2.25Mbit/s. All USART/UART interfaces can configure baud rate, parity check bit, stop bit, and data bit length; except UART5, all the other USART/UART can support DMA. USART/UART function differences are shown in the table below:

Table 8 USART/UART Function Differences

| USART mode/function | USART1 | USART2 | USART3 | UART4 | UART5 |
|---------------------------------|--------|--------|--------|-------|-------|
| Hardware flow control of modem | √ | √ | √ | — | — |
| Synchronous mode | √ | √ | √ | √ | √ |
| Smart card mode | √ | √ | √ | — | — |
| IrDASIR coder-encoder functions | √ | √ | √ | √ | √ |
| LIN mode | √ | √ | √ | √ | √ |

| USART mode/function | USART1 | USART2 | USART3 | UART4 | UART5 |
|------------------------------|--------|--------|--------|-------|-------|
| Single-line half-duplex mode | √ | √ | √ | √ | √ |
| Support DMA function | √ | √ | √ | √ | — |

Note: √ = support.

4.10.2. I2C

I2C1/2 and I2C3/4 bus interfaces are built in. I2C1 and I2C3 share hardware interface and register base address, and I2C2 and I2C4 share hardware interface and register base address. Therefore, I2C1 and I2C3 cannot be used at the same time, and I2C2 and I2C4 cannot be used simultaneously.

I2C1/2 both can work in multiple master modes or slave modes, support 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode; the communication rate supports standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s); hardware CRC generator/checker are built in; they can operate with DMA and support SMBus 2.0 version/PMBus.

I2C3/4 bus can operate in standard mode, fast mode and high-speed mode. The devices in high-speed mode and fast mode are downward compatible.

4.10.3. SPI/I2S

Three built-in SPIs, support full duplex and half duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, and communicate at a rate of up to 18Mbit/s.

2 built-in I2S (multiplexed with SPI2 and SPI3 respectively), support half duplex communication in master mode and slave mode, support synchronous transmission, and can be configured with 16-bit, 24-bit and 32-bit data transfer with 16-bit or 32-bit resolution. The configurable range of audio sampling rate is 8kHz~48kHz; when one or two I2S interfaces are configured as the master mode, the master clock can be output to external DAC or decoder (CODEC) at 256 times of sampling frequency.

4.10.4. CAN

2 built-in CANs (CAN1 and CAN2 can be used at the same time), compatible with 2.0A and 2.0B (active) specification, and can communicate at a rate of up to 1Mbit/s. It can receive and send standard frame of 11-bit identifier and extended frame of 29-bit identifier. It has 3 sending mailboxes and 2 receiving FIFO, 14 3-level adjustable filters.

4.10.5. USB

The product embeds USB modules (USB1 and USB2) compatible with full-speed USB devices, which comply with the standard of full-speed USB devices (12Mb/s), and the endpoints can be configured by software, and have standby/wake-up functions. The dedicated 48MHz clock for USB is directly generated by internal PLL. When using the USB function, the system clock can only be one of 48MHz, 72MHz, 96MHz and 120MHz, which can obtain 48MHz required for USB through 1 fractional frequency, 1.5 fractional frequency, 2 fractional frequency and 2.5 fractional frequency respectively.

USB1 and USB2 share register address and pin interface, so only one of them can be used at the same time.

1.1.1 Simultaneous use of USB and CAN interfaces

USB1 and CAN1, USB2 and CAN2 share a dedicated 512-byte SRAM memory for data transfer and receiving, so USB and CAN interfaces can be used at the same time in two

situations:

- CAN1 and USBD2 are used at the same time
- CAN2 and USBD1 are used at the same time

4.11. Analog peripherals

4.11.1. ADC

3 built-in ADCs with 12-bit accuracy, up to 16 external channels and 2 internal channels for each ADC. The internal channels measure the temperature sensor voltage and reference voltage respectively. ADC1 and ADC2 have 16 external channels, ADC3 generally has 8 external channels; A/D conversion mode of each channel has single, continuous, scan or intermittent modes, ADC conversion results can be left aligned or right aligned and stored in 16 bit data register; they support analog watchdog, and DMA.

4.11.1.1. Temperature sensor

A temperature sensor (TSensor) is built in, which is internally connected with ADC_IN16 channel. The voltage generated by the sensor changes linearly with temperature, and the converted voltage value can be obtained by ADC and converted into temperature.

4.11.1.2. Internal reference voltage

Built-in reference voltage V_{REFINT} , internally connected to ADC_IN17 channel, which can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC.

4.11.2. DAC

Two built-in 12-bit DACs, and each corresponding to an output channel, which can be configured in 8-bit and 12-bit modes, and the DMA function is supported. The waveform generation supports noise wave and triangle wave. The conversion mode supports independent or simultaneous conversion and the trigger mode supports external signal trigger and internal timer update trigger.

4.12. Timer

2 built-in 16-bit advanced timers (TMR1/8), 4 general-purpose timers (TMR2/3/4/5), 2 basic timers (TMR6/7), 1 independent watchdog timer, one window watchdog timer and 1 system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 9 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

| Timer type | System tick timer | Basic timer | | General-purpose timer | | | | Advanced timer | |
|-----------------------|-------------------|---------------------------------|------|---------------------------------|------|------|------|---------------------------------|------|
| | | TMR6 | TMR7 | TMR2 | TMR3 | TMR4 | TMR5 | TMR1 | TMR8 |
| Timer name | Sys Tick Timer | | | | | | | | |
| Counter resolution | 24-bit | 16 bits | | 16 bits | | | | 16 bits | |
| Counter type | Down | Up | | Up, down, up/down | | | | Up, down, up/down | |
| Prescaler coefficient | - | Any integer between 1 and 65536 | | Any integer between 1 and 65536 | | | | Any integer between 1 and 65536 | |

| Timer type | System tick timer | Basic timer | General-purpose timer | Advanced timer |
|----------------------------|--|--|---|--|
| General DMA request | - | OK | OK | OK |
| Capture/Comparison channel | - | - | 4 | 4 |
| Complementary outputs | - | No | No | Yes |
| Pin characteristics | - | - | There are 5 pins in total: 1-way external trigger signal input pins, 4-way channel (non-complementary channel) pins | There are 9 pins in total: 1-way external trigger signal input pins, 1-way braking input signal pins, 3-pair complementary channel pins, 1-way channel (non-complementary channel) pins |
| Function Instruction | Special for real-time operating system Automatic reloading function supported When the counter is 0, it can generate a maskable system interrupt Can program the clock source | Used to generate DAC trigger signals. Can be used as a 16-bit general-purpose timebase counter. | Synchronization or event chaining function provided Timers in debug mode can be frozen. -Can be used to generate PWM output Each timer has independent DMA request generation. It can handle incremental encoder signals | It has complementary PWM output with dead band insertion When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen, and PWM output is disabled. Synchronization or event chaining function provided. |

Table 10 Independent Watchdog and Window Watchdog Timers

| Name | Counter resolution | Counter type | Prescaler coefficient | Functional Description |
|----------------------|--------------------|--------------|-------------------------------|--|
| Independent watchdog | 12-bit | Down | Any integer between 1 and 256 | The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in shutdown and standby modes. The whole system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen. |
| Window watchdog | 7-bit | Down | - | Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function; Timers in debug mode can be frozen. |

4.13. RTC

1 RTC is built in, and there are LSECLK signal input pins (OS32_IN and OS32_OUT) and 1 TAMP input signal detection pin (TAMP); the clock source can select external 32.768kHz crystal oscillator, resonator or oscillator, LSICLK and HSECLK/32; it is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and RTC configuration and time data will not be lost; RTC configuration and time data are not lost in case of system resetting, software resetting and power resetting; it supports clock and calendar functions.

4.13.1. Backup register

84Bytes backup register is built in, and is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and the data in backup register will not be lost; the data in backup register will not be lost in case of system resetting, software resetting and power resetting.

4.14. CRC

A CRC (cyclic redundancy check) calculation unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

5. Electrical characteristics

5.1. Test conditions of electrical characteristics

5.1.1. Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at $T_A=25^{\circ}\text{C}$. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average $\pm 3\Sigma$) to get the maximum and minimum values.

5.1.2. Typical values

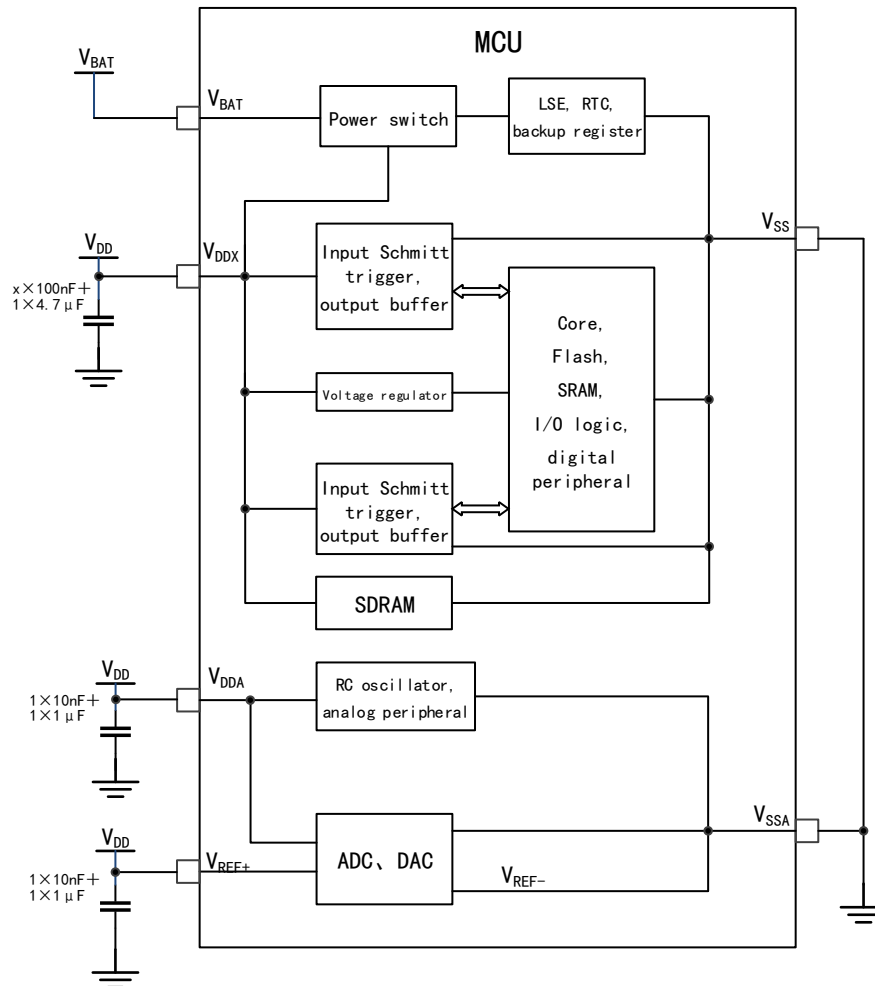
Unless otherwise specified, typical data are measured based on $T_A=25^{\circ}\text{C}$, $V_{DD}=V_{DDA}=3.3\text{V}$. these data are only used for design guidance.

5.1.3. Typical curve

Unless otherwise specified, typical curves will only be used for design guidance and will not be tested.

5.1.4. Power supply scheme

Figure 10 Power Supply Scheme



Notes: SDRAM is only applicable to APM32F103xCTxS. V_{DDX} in the figure means the number of V_{DD} is x

5.1.5. Load capacitance

Figure 11 Load conditions when measuring pin parameters

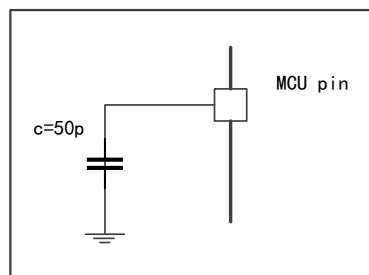


Figure 12 Pin Input Voltage Measurement Scheme

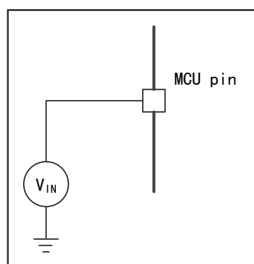
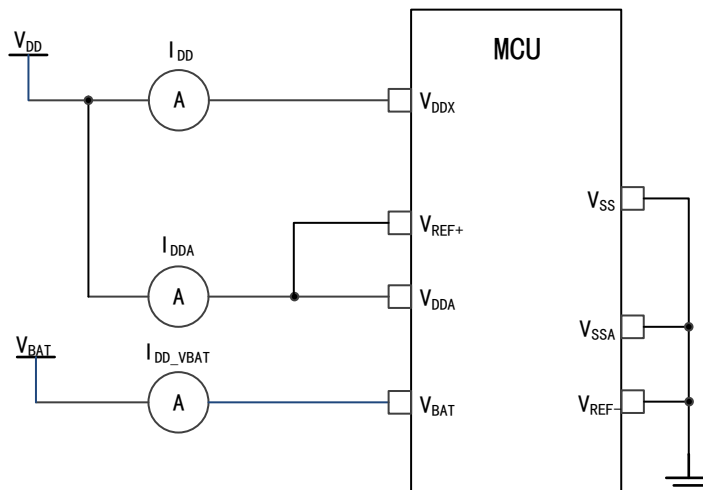


Figure 13 Power Consumption Measurement Scheme



5.2. Test under general operating conditions

Table 11 General Operating Conditions

| Symbol | Parameter | Conditions | Minimum value | Maximum value | Unit |
|--------------------|--|-------------------------------------|-----------------|---------------|------|
| f _{HCLK} | Internal AHB clock frequency | - | - | 96 | MHz |
| f _{PCLK1} | Internal APB1 clock frequency | - | - | 48 | |
| f _{PCLK2} | Internal APB2 clock frequency | - | - | 96 | |
| V _{DD} | Main power supply voltage | - | 2 | 3.6 | V |
| V _{DDA} | Analog power supply voltage (When neither ADC nor DAC is used) | Must be the same as V _{DD} | V _{DD} | 3.6 | V |
| | Analog power supply voltage (When ADC and DAC are used) | | 2.4 | 3.6 | |
| V _{BAT} | Power supply voltage of backup domain | - | 1.8 | 3.6 | V |
| T _A | Ambient temperature (temperature number 6) | Maximum power dissipation | -40 | 85 | °C |
| | Ambient temperature (temperature number 7) | Maximum power dissipation | -40 | 105 | °C |

5.3. Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent

damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1. Maximum temperature characteristics

Table 12 Temperature Characteristics

| Symbol | Description | Numerical Value | Unit |
|------------------|------------------------------|-----------------|------|
| T _{STG} | Storage temperature range | -55 ~ +150 | °C |
| T _J | Maximum junction temperature | 150 | °C |

5.3.2. Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 13 Maximum Rated Voltage Characteristics

| Symbol | Description | Minimum value | Maximum value | Unit |
|------------------------------------|---|----------------------|-----------------------|------|
| V _{DD} - V _{SS} | External main power supply voltage | -0.3 | 4.0 | V |
| V _{DDA} -V _{SSA} | External analog power supply voltage | -0.3 | 4.0 | |
| V _{BAT} -V _{SS} | Power supply voltage of external backup domain | -0.3 | 4.0 | |
| V _{DD} -V _{DDA} | Voltage difference allowed by V _{DD} >V _{DDA} | - | 0.3 | |
| V _{IN} | Input voltage on FT pins | V _{SS} -0.3 | 5.5 | |
| | Input voltage on other pins | V _{SS} -0.3 | V _{DD} + 0.3 | |
| ΔV _{DDx} | Voltage difference between different power supply pins | - | 50 | mV |
| V _{SSx} -V _{SS} | Voltage difference between different grounding pins | - | 50 | |

5.3.3. Maximum rated current features

Table 14 Current Characteristics

| Symbol | Description | Maximum | Unit |
|--|--|---------|------|
| I _{VDD} | Total current into V _{DD} /V _{DDA} power lines (source) ⁽¹⁾ | 150 | mA |
| I _{VSS} | Total current out of V _{SS} ground lines (sink) ⁽¹⁾ | 150 | |
| I _{IO} | Irrigation current on any I/O and control pins | 25 | |
| | Source current on any I/O and control pins | -25 | |
| I _{INJ(PIN)} ^{(2) (3)} | Injection current of 5T pin | ±5 | |
| | Injection current of other pins | ±5 | |
| ΣI _{INJ(PIN)} ⁽²⁾ | Total injection current on all I/O and control pins ⁽⁴⁾ | ±25 | |

- 1) All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to a power supply within the external allowable range.
- 2) Negative injection disturbs the analog performance of the device.

- 3) Positive injection is not possible on these I/Os. a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.
- 4) A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.
- 5) When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3.4. Electrostatic discharge (ESD)

Table 15 ESD Absolute Maximum Ratings

| type | Symbol | Parameter | Conditions | Maximum value | Unit |
|----------------|----------------|---|---|---------------|------|
| APM32F103xCTx | $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A = +25\text{ }^\circ\text{C}$, conforming to JESD22-A114 | 5500 | V |
| | $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charging device model) | $T_A = +25\text{ }^\circ\text{C}$, conforming to JESD22-C101 | 1700 | |
| APM32F103xCTxS | $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A = +25\text{ }^\circ\text{C}$, conforming to JESD22-A114 | 4000 | |
| | $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charging device model) | $T_A = +25\text{ }^\circ\text{C}$, conforming to JESD22-C101 | 2000 | |

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5. Static latch-up (LU)

Table 16 Static Latch-up

| Symbol | Parameter | Conditions | Type |
|--------|--------------------------|---|--------------------|
| LU | Class of static latch-up | $T_A = +25\text{ }^\circ\text{C}/105^\circ\text{C}$, conforming to EIA/JESD78E | $\pm 200\text{mA}$ |

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4. On-chip memory

5.4.1. Flash characteristics

Table 17 Flash Memory Characteristics

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|-------------|---------------------------|---|---------------|----------------|---------------|---------------|
| t_{prog} | 16-bit programming time | $T_A = -40\sim 105^\circ\text{C}$ $V_{DD} = 2.4\sim 3.6\text{V}$ | 33.50 | 34.60 | 35.42 | μs |
| t_{ERASE} | Page (2KBytes) erase time | $T_A = -40\sim 105^\circ\text{C}$ $V_{DD} = 2.4\sim 3.6\text{V}$ | 2.80 | 3.14 | 3.20 | ms |
| t_{ME} | Whole erase time | $T_A = 25^\circ\text{C}$ $V_{DD} = 3.3\text{V}$ | 11.90 | 12.34 | 12.70 | ms |
| V_{prog} | Programming voltage | $T_A = -40\sim 105^\circ\text{C}$ | 2 | - | 3.6 | V |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5. Clock

5.5.1. Characteristics of external clock source

5.5.1.1.1. High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 18 HSECLK4~16MHz Oscillator Characteristics

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|-------------------------|----------------------------|--|---------------|----------------|---------------|------|
| f _{OSC_IN} | Oscillator frequency | - | 4 | 8 | 16 | MHz |
| RF | Feedback resistance | - | - | 300.7 | - | kΩ |
| I _{DD(HSECLK)} | HSECLK current consumption | V _{DD} =3.3V, CL=10pF@8MHz | - | 0.29 | - | mA |
| t _{SU(HSECLK)} | Startup time | V _{DD} is stable | - | 0.99 | - | ms |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.1.1.2. Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 19 LSECLK Oscillator Characteristics (f_{LSECLK}=32.768KHz)

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|--|----------------------------|------------------------------|---------------|----------------|---------------|------|
| f _{OSF_IN} | Oscillator frequency | - | - | 32.768 | - | KHz |
| t _{SU(LSECLK)} ⁽¹⁾ | Startup time | V _{DDIOx} is stable | - | 0.99 | - | s |
| I _{DD(LSECLK)} | LSECLK current consumption | - | - | 0.9 | - | μA |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

- (1) t_{SU(LSECLK)} is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.5.2. Characteristics of internal clock source

5.5.2.1.1. High speed internal (HSICLK) RC oscillator

Table 20 HSICLK Oscillator Characteristics

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit | |
|-----------------------|-------------------------------|---------------------|---|----------------|---------------|------|---|
| f _{HSICLK} | Frequency | - | - | 8 | - | MHz | |
| A _{CHHSICLK} | Accuracy of HSICLK oscillator | Factory calibration | V _{DD} =3.3V, T _A =-25°C ⁽¹⁾ | -1 | - | 1 | % |
| | | | V _{DD} =2-3.6V, T _A =-40~105°C | -1.08 | - | 1.29 | % |

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|--------------------------|--|--|---------------|----------------|---------------|------|
| t _{SU(HSICLK)} | Startup time of HSICLK oscillator | V _{DD} =3.3V, T _A =-40~105°C | 0.60 | - | 1.16 | μs |
| I _{DDA(HSICLK)} | Power consumption of HSICLK oscillator | - | - | 61.6 | 64.3 | μA |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.2.1.2. Low speed internal (LSICLK) RC oscillator

Table 21 LSICLK Oscillator Characteristics

| Symbol | Parameter | Minimum value | Typical values | Maximum value | Unit |
|-------------------------|--|---------------|----------------|---------------|------|
| f _{LSICLK} | Frequency (V _{DD} =2-3.6V, T _A =-40~105°C) | 40.12 | 41.28 | 46.10 | KHz |
| t _{SU(LSICLK)} | LSICLK oscillator startup time, (V _{DD} =3.3V, T _A =-40~105°C) | - | - | 79.2 | μs |
| I _{DD(LSICLK)} | Power consumption of LSICLK oscillator | - | 0.5 | - | μA |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.3. PLL Characteristics

Table 22 PLL Characteristics

| Symbol | Parameter | Numerical Value | | | Unit |
|----------------------|---|-----------------|----------------|---------------|------|
| | | Minimum value | Typical values | Maximum value | |
| f _{PLL_IN} | PLL input clock | 1 | 8.0 | 25 | MHz |
| | PLL input clock duty cycle | 40 | - | 60 | % |
| f _{PLL_OUT} | PLL frequency doubling output clock, (V _{DD} =3.3V, T _A =-40~105°C) | 2 | - | 96 | MHz |
| t _{LOCK} | PLL phase locking time | - | - | 84.0 | μs |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.6. Reset and power management

5.6.1. Test of embedded reset and power control block characteristics

Table 23 Embedded Reset and Power Control Block Characteristics

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|----------------------|-------------------------------------|--------------|---------------|----------------|---------------|------|
| V _{POR/PDR} | Power-on/power-down reset threshold | Falling edge | 1.87 | 1.88 | 1.90 | V |
| | | Rising edge | 1.92 | 1.94 | 1.96 | V |
| V _{PDRhyst} | PDR hysteresis | - | 50.00 | 55.00 | 60.00 | mV |
| TRSTTEMPO | Reset duration | - | 0.98 | 1.27 | 3.06 | ms |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 24 Programmable Power Supply Voltage Detector Characteristics

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|-----------------------------|--|-----------------------------|---------------|----------------|---------------|------|
| V _{PVD} | Programmable power supply voltage detector voltage level selection | PLS[2:0]=000 (rising edge) | 2.18 | 2.20 | 2.22 | V |
| | | PLS[2:0]=000 (falling edge) | 2.08 | 2.09 | 2.11 | V |
| | | PLS[2:0]=001 (rising edge) | 2.29 | 2.30 | 2.32 | V |
| | | PLS[2:0]=001 (falling edge) | 2.18 | 2.19 | 2.21 | V |
| | | PLS[2:0]=010 (rising edge) | 2.39 | 2.40 | 2.42 | V |
| | | PLS[2:0]=010 (falling edge) | 2.28 | 2.29 | 2.31 | V |
| | | PLS[2:0]=011 (rising edge) | 2.48 | 2.49 | 2.52 | V |
| | | PLS[2:0]=011 (falling edge) | 2.38 | 2.39 | 2.41 | V |
| | | PLS[2:0]=100 (rising edge) | 2.58 | 2.60 | 2.62 | V |
| | | PLS[2:0]=100 (falling edge) | 2.47 | 2.48 | 2.51 | V |
| | | PLS[2:0]=101 (rising edge) | 2.68 | 2.69 | 2.72 | V |
| | | PLS[2:0]=101 (falling edge) | 2.57 | 2.59 | 2.61 | V |
| | | PLS[2:0]=110 (rising edge) | 2.78 | 2.79 | 2.82 | V |
| | | PLS[2:0]=110 (falling edge) | 2.67 | 2.68 | 2.71 | V |
| | | PLS[2:0]=111 (rising edge) | 2.87 | 2.88 | 2.91 | V |
| PLS[2:0]=111 (falling edge) | 2.77 | 2.78 | 2.81 | V | | |
| V _{PVDhyst} | PVD hysteresis | - | - | 107.08 | - | mV |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.7. Power consumption

Forms containing SDRAM are applicable to APM32F103xCTxS, otherwise applicable to APM32F103xCTx.

5.7.1. Power consumption test environment

- (1) The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.
- (2) All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- (3) Unless otherwise specified, all peripherals are turned off
- (4) The relationship between Flash waiting cycle setting and f_{HCLK} :
 - 0~24MHz: 0 waiting cycle
 - 24~48MHz: 1 waiting cycle
 - 48~72MHz: 2 waiting cycles
 - 72~96MHz: 3 waiting cycles
- (5) The instruction prefetch function is enabled (Note: it must be set before clock setting and bus frequency division)

(6) When the peripherals are enabled: $f_{PCLK1}=f_{HCLK}/2$, $f_{PCLK2}=f_{HCLK}$

5.7.2. Power consumption in run mode

Table 25 Power Consumption in Run Mode when the Program is Executed in Flash

| Parameter | Conditions | f _{HCLK} | Typical value (1) | | Maximum value (1) | |
|-------------------------------|--|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =105°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| Power consumption in run mode | HSECLK bypass ⁽²⁾ , enabling all peripherals | 96MHz | 206.63 | 39.25 | 228.52 | 41.52 |
| | | 72MHz | 153.24 | 31.21 | 169.65 | 33.25 |
| | | 48MHz | 102.26 | 21.04 | 115.06 | 22.51 |
| | | 36MHz | 78.50 | 16.86 | 90.10 | 18.18 |
| | | 24MHz | 57.57 | 11.67 | 67.95 | 12.60 |
| | | 16MHz | 44.88 | 8.48 | 54.36 | 9.31 |
| | | 8MHz | 2.66 | 4.66 | 5.69 | 5.32 |
| | HSECLK bypass ⁽²⁾ , turning off all peripherals | 96MHz | 206.59 | 20.92 | 227.42 | 22.04 |
| | | 72MHz | 153.19 | 17.40 | 169.33 | 18.41 |
| | | 48MHz | 102.28 | 11.98 | 114.86 | 12.77 |
| | | 36MHz | 78.47 | 10.04 | 89.99 | 10.80 |
| | | 24MHz | 57.53 | 7.01 | 67.89 | 7.68 |
| | | 16MHz | 44.87 | 5.40 | 54.38 | 6.01 |
| | | 8MHz | 2.69 | 3.12 | 5.46 | 3.65 |
| | HSICLK ⁽²⁾ , enabling all peripherals | 64MHz | 196.28 | 27.82 | 216.47 | 29.20 |
| | | 48MHz | 162.92 | 20.79 | 179.89 | 22.32 |
| | | 36MHz | 139.39 | 16.66 | 154.46 | 17.86 |
| | | 24MHz | 118.22 | 11.44 | 132.16 | 12.28 |
| | | 16MHz | 105.50 | 8.19 | 119.21 | 8.97 |
| | | 8MHz | 63.79 | 4.38 | 73.87 | 4.96 |
| | HSICLK ⁽²⁾ , turning off all peripherals | 64MHz | 196.33 | 15.34 | 215.85 | 16.21 |
| | | 48MHz | 162.86 | 11.70 | 179.35 | 12.45 |
| | | 36MHz | 139.41 | 9.77 | 154.14 | 10.46 |
| | | 24MHz | 118.21 | 6.72 | 132.07 | 7.34 |
| 16MHz | | 105.50 | 5.12 | 119.16 | 5.66 | |
| 8MHz | | 63.84 | 2.85 | 73.83 | 3.30 | |

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 26 Power Consumption in Run Mode when the Program is Executed in RAM

| Parameter | Conditions | f _{HCLK} | Typical value (1) | | Maximum value (1) | |
|-------------------------------|--|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =105°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| Power consumption in run mode | HSECLK bypass ⁽²⁾ , enabling all peripherals | 96MHz | 206.51 | 39.25 | 227.45 | 40.97 |
| | | 72MHz | 153.23 | 29.63 | 169.48 | 31.34 |
| | | 48MHz | 102.29 | 20.00 | 115.08 | 21.63 |
| | | 36MHz | 78.50 | 15.46 | 90.03 | 16.76 |
| | | 24MHz | 57.51 | 10.65 | 67.95 | 11.79 |
| | | 16MHz | 44.87 | 7.45 | 54.3 | 8.65 |
| | | 8MHz | 2.66 | 4.10 | 5.22 | 5.18 |
| | HSECLK bypass ⁽²⁾ , turning off all peripherals | 96MHz | 206.56 | 20.82 | 227.44 | 22.39 |
| | | 72MHz | 153.16 | 15.92 | 169.37 | 17.26 |
| | | 48MHz | 102.24 | 10.90 | 114.94 | 12.18 |
| | | 36MHz | 78.46 | 8.41 | 90.01 | 9.67 |
| | | 24MHz | 57.54 | 5.95 | 67.91 | 7.15 |
| | | 16MHz | 44.86 | 4.27 | 54.24 | 5.47 |
| | | 8MHz | 2.66 | 2.59 | 5.26 | 3.76 |
| | HSICLK ⁽²⁾ , enabling all peripherals | 64MHz | 196.24 | 26.10 | 215.14 | 27.90 |
| | | 48MHz | 162.89 | 19.74 | 178.89 | 21.34 |
| | | 36MHz | 139.38 | 15.13 | 154.16 | 16.61 |
| | | 24MHz | 118.17 | 10.37 | 132.06 | 11.55 |
| | | 16MHz | 105.50 | 7.15 | 119.05 | 8.33 |
| | | 8MHz | 63.79 | 3.82 | 73.8 | 4.95 |
| | HSICLK ⁽²⁾ , turning off all peripherals | 64MHz | 196.25 | 14.09 | 215.09 | 15.52 |
| | | 48MHz | 162.84 | 10.61 | 178.95 | 11.99 |
| | | 36MHz | 139.36 | 8.14 | 154.10 | 9.53 |
| | | 24MHz | 118.15 | 5.68 | 132.00 | 6.93 |
| 16MHz | | 105.47 | 3.99 | 119.09 | 5.22 | |
| 8MHz | | 63.81 | 2.31 | 73.76 | 3.50 | |

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 27 SDRAM is in the Run Mode, Power Consumption in Run Mode when the Program is Executed in Flash

| Parameter | Conditions | f _{HCLK} | Typical value (1) | | Maximum value (1) | |
|-------------------------------|--|---|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =105°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| Power consumption in run mode | HSECLK bypass ⁽²⁾ , enabling all peripherals | 96MHz | 207.38 | 58.71 | 246.03 | 65.08 |
| | | 72MHz | 153.96 | 50.06 | 181.80 | 57.55 |
| | | 48MHz | 102.91 | 39.07 | 122.96 | 44.89 |
| | | 36MHz | 78.75 | 34.46 | 97.08 | 39.00 |
| | | 24MHz | 57.50 | 28.85 | 75.12 | 32.64 |
| | | 16MHz | 44.75 | 25.42 | 61.97 | 28.84 |
| | | 8MHz | 2.60 | 21.43 | 10.91 | 24.01 |
| | HSECLK bypass ⁽²⁾ , turning off all peripherals | 96MHz | 207.33 | 36.00 | 240.91 | 40.58 |
| | | 72MHz | 153.88 | 32.72 | 180.55 | 36.74 |
| | | 48MHz | 102.86 | 27.52 | 123.04 | 31.10 |
| | | 36MHz | 78.75 | 25.73 | 97.27 | 29.36 |
| | | 24MHz | 57.48 | 22.95 | 75.57 | 26.16 |
| | | 16MHz | 44.74 | 21.42 | 62.62 | 24.50 |
| | | 8MHz | 2.59 | 19.25 | 9.24 | 22.06 |
| | HSICLK ⁽²⁾ , enabling all peripherals | 64MHz | 195.51 | 45.68 | 223.35 | 52.74 |
| | | 48MHz | 162.08 | 38.64 | 186.03 | 44.49 |
| | | 36MHz | 138.38 | 34.19 | 161.24 | 38.87 |
| | | 24MHz | 116.92 | 28.59 | 139.48 | 32.25 |
| | | 16MHz | 104.17 | 25.03 | 127.08 | 28.30 |
| | | 8MHz | 62.63 | 21.10 | 73.63 | 23.74 |
| | | HSICLK ⁽²⁾ , turning off all peripherals | 64MHz | 195.55 | 30.73 | 227.47 |
| | 48MHz | | 162.04 | 27.24 | 189.93 | 30.54 |
| | 36MHz | | 138.37 | 25.46 | 164.53 | 28.55 |
| | 24MHz | | 116.89 | 22.66 | 142.41 | 25.60 |
| 16MHz | 104.2 | | 21.12 | 129.70 | 23.96 | |
| 8MHz | 62.63 | | 18.99 | 75.77 | 21.66 | |

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 28 SDRAM is in the Low Power Mode, Power Consumption in Run Mode when the Program is Executed in Flash

| Parameter | Conditions | f _{HCLK} | Typical value ⁽¹⁾ | | Maximum value ⁽¹⁾ | |
|-------------------------------|--|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =125°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| Power consumption in run mode | HSECLK bypass ⁽²⁾ , enabling all peripherals | 96MHz | 219.23 | 44.48 | 240.46 | 50.50 |
| | | 72MHz | 164.57 | 36.02 | 178.84 | 42.82 |
| | | 48MHz | 110.85 | 25.20 | 121.19 | 30.76 |
| | | 36MHz | 85.94 | 20.80 | 95.73 | 24.45 |
| | | 24MHz | 64.97 | 14.90 | 73.86 | 18.72 |
| | | 16MHz | 52.57 | 11.54 | 60.66 | 14.63 |
| | | 8MHz | 2.63 | 7.39 | 7.76 | 10.14 |
| | HSECLK bypass ⁽²⁾ , turning off all peripherals | 96MHz | 219.37 | 29.97 | 239.29 | 34.95 |
| | | 72MHz | 164.64 | 25.50 | 178.43 | 28.96 |
| | | 48MHz | 110.87 | 19.26 | 121.05 | 24.64 |
| | | 36MHz | 85.97 | 16.80 | 95.60 | 23.69 |
| | | 24MHz | 65.07 | 13.42 | 74.03 | 14.23 |
| | | 16MHz | 52.63 | 11.38 | 60.96 | 12.00 |
| | | 8MHz | 2.64 | 8.87 | 7.49 | 8.93 |
| | HSICLK ⁽²⁾ , enabling all peripherals | 64MHz | 204.81 | 32.30 | 219.11 | 36.82 |
| | | 48MHz | 169.45 | 25.45 | 182.42 | 28.89 |
| | | 36MHz | 145.12 | 20.72 | 157.94 | 24.66 |
| | | 24MHz | 123.88 | 15.14 | 136.56 | 17.77 |
| | | 16MHz | 111.45 | 11.86 | 123.53 | 14.26 |
| | | 8MHz | 66.94 | 7.63 | 74.92 | 9.65 |
| | HSICLK ⁽²⁾ , turning off all peripherals | 64MHz | 205.09 | 23.07 | 218.98 | 26.05 |
| | | 48MHz | 169.39 | 19.00 | 182.27 | 23.82 |
| | | 36MHz | 144.96 | 16.48 | 157.80 | 23.04 |
| | | 24MHz | 123.76 | 13.09 | 136.49 | 13.32 |

| Parameter | Conditions | f _{HCLK} | Typical value ⁽¹⁾ | | Maximum value ⁽¹⁾ | |
|-----------|------------|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =125°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| | | 16MHz | 111.35 | 11.09 | 123.60 | 11.27 |
| | | 8MHz | 66.82 | 8.58 | 74.48 | 8.24 |

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

5.7.3. Power consumption in sleep mode

Table 29 Power Consumption in Sleep Mode when the Program is Executed in Flash

| Parameter | Conditions | f _{HCLK} | Typical value ⁽¹⁾ | | Maximum value ⁽¹⁾ | |
|---------------------------------|--|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =105°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| Power consumption in sleep mode | HSECLK bypass ⁽²⁾ , enabling all peripherals | 96 MHz | 206.61 | 26.91 | 227.53 | 27.85 |
| | | 72MHz | 153.22 | 20.59 | 169.51 | 21.20 |
| | | 48MHz | 102.26 | 13.96 | 115.04 | 14.62 |
| | | 36MHz | 78.49 | 10.72 | 89.95 | 11.30 |
| | | 24MHz | 57.54 | 7.52 | 67.93 | 8.15 |
| | | 16MHz | 44.87 | 5.31 | 54.33 | 5.88 |
| | | 8MHz | 2.66 | 3.10 | 5.31 | 3.58 |
| | HSECLK bypass ⁽²⁾ , turning off all peripherals | 96 MHz | 206.62 | 6.03 | 227.52 | 6.54 |
| | | 72MHz | 153.16 | 4.79 | 169.35 | 5.22 |
| | | 48MHz | 102.21 | 3.55 | 114.87 | 3.97 |
| | | 36MHz | 78.45 | 2.91 | 89.89 | 3.37 |
| | | 24MHz | 57.57 | 2.28 | 67.89 | 2.74 |
| | | 16MHz | 44.85 | 1.86 | 54.35 | 2.30 |
| | | 8MHz | 2.67 | 1.37 | 5.24 | 1.80 |
| | HSICLK ⁽²⁾ , enabling all peripherals | 64MHz | 196.28 | 18.20 | 215.44 | 18.73 |
| | | 48MHz | 162.87 | 13.69 | 179.09 | 14.57 |
| | | 36MHz | 139.39 | 10.47 | 154.12 | 11.17 |
| | | 24MHz | 118.18 | 7.24 | 132.1 | 7.79 |
| 16MHz | | 105.49 | 5.05 | 119.13 | 5.55 | |
| 8MHz | | 63.82 | 2.81 | 73.87 | 3.23 | |
| | | 64MHz | 196.28 | 4.08 | 215.30 | 4.52 |

| Parameter | Conditions | f _{HCLK} | Typical value ⁽¹⁾ | | Maximum value ⁽¹⁾ | |
|-----------|---|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =105°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| | HSICLK ⁽²⁾ , turning off all peripherals | 48MHz | 162.78 | 3.24 | 178.89 | 3.64 |
| | | 36MHz | 139.31 | 2.61 | 154.16 | 3.00 |
| | | 24MHz | 118.11 | 1.98 | 132.08 | 2.60 |
| | | 16MHz | 105.47 | 1.56 | 119.07 | 2.24 |
| | | 8MHz | 63.79 | 1.08 | 73.77 | 1.74 |
| | | | | | | |

Table 30 Power Consumption in Sleep Mode when the Program is Executed in RAM

| Parameter | Conditions | f _{HCLK} | Typical value ⁽¹⁾ | | Maximum value ⁽¹⁾ | |
|---------------------------------|--|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =105°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| Power consumption in sleep mode | HSECLK bypass ⁽²⁾ , enabling all peripherals | 96MHz | 206.61 | 26.59 | 227.46 | 28.59 |
| | | 72MHz | 153.18 | 20.34 | 169.39 | 21.84 |
| | | 48MHz | 102.25 | 13.79 | 115.00 | 15.433 |
| | | 36MHz | 78.48 | 10.64 | 90.05 | 12.03 |
| | | 24MHz | 57.53 | 7.48 | 67.93 | 8.90 |
| | | 16MHz | 44.86 | 5.30 | 54.29 | 6.60 |
| | | 8MHz | 2.68 | 3.07 | 5.20 | 4.38 |
| | HSECLK bypass ⁽²⁾ , turning off all peripherals | 96MHz | 206.56 | 6.06 | 227.52 | 7.34 |
| | | 72MHz | 153.11 | 4.77 | 169.35 | 6.15 |
| | | 48MHz | 102.22 | 3.53 | 114.85 | 4.81 |
| | | 36MHz | 78.41 | 2.90 | 89.90 | 4.21 |
| | | 24MHz | 57.48 | 2.27 | 67.99 | 3.56 |
| | | 16MHz | 44.84 | 1.86 | 54.23 | 3.16 |
| | | 8MHz | 2.66 | 1.37 | 5.28 | 2.66 |
| | HSICLK ⁽²⁾ , enabling all peripherals | 64MHz | 196.27 | 17.94 | 214.87 | 19.60 |
| | | 48MHz | 162.87 | 13.48 | 178.97 | 15.27 |
| | | 36MHz | 139.33 | 10.34 | 154.00 | 11.86 |
| | | 24MHz | 118.13 | 7.20 | 131.99 | 8.50 |
| | | 16MHz | 105.48 | 5.01 | 119.02 | 6.38 |
| | | 8MHz | 63.82 | 2.79 | 73.82 | 4.05 |
| | | | 64MHz | 196.23 | 4.06 | 214.79 |

| Parameter | Conditions | f _{HCLK} | Typical value ⁽¹⁾ | | Maximum value ⁽¹⁾ | |
|-----------|---|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =105°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| | HSICLK ⁽²⁾ , turning off all peripherals | 48MHz | 162.77 | 3.23 | 178.80 | 4.53 |
| | | 36MHz | 139.31 | 2.60 | 153.92 | 3.86 |
| | | 24MHz | 118.12 | 1.97 | 131.99 | 3.26 |
| | | 16MHz | 105.45 | 1.56 | 118.97 | 2.81 |
| | | 8MHz | 63.79 | 1.08 | 73.73 | 2.34 |

Note:

(1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL

Table 31 SDRAM is in the Run Mode, Power Consumption in Sleep Mode when the Program is Executed in Flash

| Parameter | Conditions | f _{HCLK} | Typical value (1) | | Maximum value (1) | |
|---------------------------------|--|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =105°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| Power consumption in sleep mode | HSECLK bypass ⁽²⁾ , enabling all peripherals | 96MHz | 207.40 | 46.54 | 243.23 | 52.99 |
| | | 72MHz | 153.97 | 39.16 | 182.24 | 45.06 |
| | | 48MHz | 102.89 | 32.22 | 124.28 | 36.77 |
| | | 36MHz | 78.75 | 28.49 | 98.29 | 32.56 |
| | | 24MHz | 57.51 | 24.87 | 76.49 | 28.24 |
| | | 16MHz | 44.73 | 22.32 | 63.42 | 25.47 |
| | | 8MHz | 2.59 | 19.80 | 8.58 | 22.53 |
| | HSECLK bypass ⁽²⁾ , turning off all peripherals | 96MHz | 207.41 | 21.99 | 243.02 | 24.74 |
| | | 72MHz | 153.93 | 20.82 | 182.13 | 23.49 |
| | | 48MHz | 102.87 | 19.62 | 124.10 | 22.24 |
| | | 36MHz | 78.74 | 19.04 | 98.15 | 21.53 |
| | | 24MHz | 57.50 | 18.42 | 76.21 | 20.88 |
| | | 16MHz | 44.74 | 18.04 | 63.29 | 20.44 |
| | | 8MHz | 2.59 | 17.57 | 8.55 | 19.95 |
| | HSICLK ⁽²⁾ , enabling all peripherals | 64MHz | 195.54 | 36.52 | 229.41 | 41.55 |
| | | 48MHz | 162.08 | 31.76 | 191.41 | 36.14 |
| 36MHz | | 138.38 | 28.21 | 165.76 | 34.89 | |
| 24MHz | | 116.91 | 24.64 | 143.34 | 27.55 | |

| Parameter | Conditions | f _{HCLK} | Typical value (1) | | Maximum value (1) | |
|-----------|---|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =105°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| | | 16MHz | 104.20 | 22.03 | 130.41 | 24.88 |
| | | 8MHz | 62.65 | 19.50 | 76.30 | 21.97 |
| | HSICKL ⁽²⁾ , turning off all peripherals | 64MHz | 195.55 | 20.13 | 229.14 | 22.41 |
| | | 48MHz | 162.06 | 19.36 | 191.09 | 21.70 |
| | | 36MHz | 138.38 | 18.73 | 165.38 | 21.07 |
| | | 24MHz | 116.92 | 18.13 | 143.02 | 20.45 |
| | | 16MHz | 104.19 | 17.74 | 130.08 | 19.92 |
| | | 8MHz | 62.64 | 17.31 | 76.02 | 19.51 |

Note:

(1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 32 SDRAM is in the Low Power Mode, Power Consumption in Sleep Mode when the Program is Executed in Flash

| Parameter | Conditions | f _{HCLK} | Typical value (1) | | Maximum value (1) | |
|---------------------------------|--|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =125°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| Power consumption in sleep mode | HSECLK bypass ⁽²⁾ , enabling all peripherals | 96 MHz | 205.82 | 32.97 | 240.41 | 37.83 |
| | | 72MHz | 152.49 | 25.78 | 179.31 | 29.22 |
| | | 48MHz | 101.73 | 18.46 | 121.54 | 21.52 |
| | | 36MHz | 77.66 | 14.96 | 95.95 | 17.98 |
| | | 24MHz | 56.48 | 11.35 | 74.41 | 13.46 |
| | | 16MHz | 43.67 | 8.81 | 61.17 | 10.93 |
| | | 8MHz | 2.59 | 6.28 | 7.33 | 8.24 |
| | HSECLK bypass ⁽²⁾ , turning off all peripherals | 96 MHz | 205.85 | 15.26 | 240.02 | 19.43 |
| | | 72MHz | 152.47 | 13.16 | 178.96 | 15.22 |
| | | 48MHz | 101.71 | 10.99 | 121.48 | 15.74 |
| | | 36MHz | 77.65 | 9.88 | 95.94 | 9.93 |
| | | 24MHz | 56.48 | 8.71 | 74.58 | 8.25 |
| | | 16MHz | 43.68 | 7.96 | 61.50 | 7.87 |
| | | | 8MHz | 2.59 | 7.16 | 7.50 |
| | | 64MHz | 193.71 | 23.25 | 219.46 | 27.04 |

| Parameter | Conditions | f _{HCLK} | Typical value ⁽¹⁾ | | Maximum value ⁽¹⁾ | |
|-----------|---|-------------------|---|----------------------|--|----------------------|
| | | | T _A =25°C, V _{DD} =3.3V | | T _A =125°C, V _{DD} =3.6V | |
| | | | I _{DDA} (μA) | I _{DD} (mA) | I _{DDA} (μA) | I _{DD} (mA) |
| | HSICLK ⁽²⁾ , enabling all peripherals | 48MHz | 160.46 | 18.25 | 182.24 | 21.78 |
| | | 36MHz | 136.83 | 14.67 | 157.75 | 17.43 |
| | | 24MHz | 115.36 | 10.98 | 136.35 | 12.96 |
| | | 16MHz | 102.61 | 8.54 | 123.64 | 10.41 |
| | | 8MHz | 62.07 | 5.99 | 74.24 | 7.76 |
| | | 64MHz | 193.78 | 12.11 | 219.48 | 14.87 |
| | HSICLK ⁽²⁾ , turning off all peripherals | 48MHz | 160.46 | 10.68 | 182.29 | 14.97 |
| | | 36MHz | 136.80 | 9.57 | 157.74 | 11.56 |
| | | 24MHz | 115.37 | 8.41 | 136.44 | 9.88 |
| | | 16MHz | 102.57 | 7.66 | 123.64 | 8.80 |
| | | 8MHz | 62.06 | 6.85 | 123.64 | 7.71 |

Note:

(1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

5.7.4. Power consumption in stop mode and standby mode

Table 33 Power Consumption in Stop Mode and Standby Mode

| Parameter | Conditions | Typical value ⁽¹⁾ , (T _A =25°C) | | | | | | Maximum value ⁽¹⁾ , (V _{DD} =3.6V) | | Unit |
|------------------------------------|--|---|-----------------|-----------------------|-----------------|-----------------------|-----------------|--|-----------------|------|
| | | V _{DD} =2.4V | | V _{DD} =3.3V | | V _{DD} =3.6V | | T _A =105°C | | |
| | | I _{DDA} | I _{DD} | I _{DDA} | I _{DD} | I _{DDA} | I _{DD} | I _{DDA} | I _{DD} | |
| Power consumption in shutdown mode | Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog) | 2.64 | 25.23 | 2.76 | 25.56 | 2.46 | 25.06 | 3.97 | 236.41 | μA |
| | Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog) | 2.58 | 12.76 | 2.70 | 12.93 | 2.44 | 12.80 | 3.96 | 214.83 | |
| Power consumption in standby mode | Low-speed internal RC oscillator and independent watchdog ON | 2.89 | 0.85 | 2.99 | 0.99 | 2.69 | 0.78 | 3.46 | 6.83 | |
| | Low-speed internal RC oscillator on, independent watchdog OFF | 2.91 | 0.74 | 2.98 | 0.84 | 2.68 | 0.62 | 3.44 | 6.87 | |
| | Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF | 2.42 | 0.34 | 2.52 | 0.40 | 2.28 | 0.30 | 3.10 | 6.37 | |

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.5. Backup domain power consumption

Table 34 Backup Domain Power Consumption

| Symbol | Conditions | Typical value ⁽¹⁾ , T _A =25°C | | | Maximum value ⁽¹⁾ , V _{BAT} =3.6V | | | Unit |
|---------------------------|--|---|------------------------|------------------------|---|----------------------|-----------------------|------|
| | | V _{BAT} =1.8V | V _{BAT} =2.4V | V _{BAT} =3.3V | T _A =25°C | T _A =85°C | T _A =105°C | |
| ID _{DD_VB} AT | The low-speed oscillator and RTC are in ON state | 0.79 | 0.97 | 1.21 | 2.78 | 2.6 | 4.2 | μA |

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.6. Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, fPCLK=fHCLK=1M.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 35 Peripheral Power Consumption

| Parameter | Peripheral | Typical value ⁽¹⁾ T _A =25°C, V _{DD} =3.3V | Unit |
|------------------------------|-------------|--|--------|
| Peripheral power consumption | BusMatrix | 3.875 | μA/MHz |
| | DMA1 | 5.25 | |
| | DMA2 | 3.50 | |
| | EMMC | 19.25 | |
| | CRC | 0.86 | |
| | SDIO | 10.88 | |
| | ALL_AHB | 43.62 | |
| | APB1 Bridge | 1.00 | |
| | TMR2 | 18.25 | |
| | TMR3 | 17.75 | |
| | TMR4 | 16.75 | |
| | TMR5 | 17.75 | |
| | TMR6 | 4.00 | |
| | TMR7 | 4.00 | |
| | WWDT | 2.50 | |
| | IWDT | 3.87 | |
| | SPI2/I2S2 | 2.88 | |
| | SPI3/I2S3 | 2.88 | |
| | USART2 | 6.88 | |
| USART3 | 6.75 | | |
| UART4 | 6.38 | | |

| Parameter | Peripheral | Typical value ⁽¹⁾ TA =25°C, VDD =3.3V | Unit |
|-----------|-------------|--|------|
| | UART5 | 6.25 | |
| | I2C1 | 7.13 | |
| | I2C2 | 7.00 | |
| | USB1/USB2 | 10.75 | |
| | CAN1 | 10.38 | |
| | CAN2 | 10.38 | |
| | BAKPR | 2.38 | |
| | PMU | 1.50 | |
| | DAC | 4.13 | |
| | ALL_APB1 | 150.28 | |
| | APB2 Bridge | 2.75 | |
| | GPIOA | 5.00 | |
| | GPIOB | 5.00 | |
| | GPIOC | 4.75 | |
| | GIOD | 4.75 | |
| | GPIOE | 4.63 | |
| | GPIOF | 4.00 | |
| | ADC1 | 10.50 | |
| | ADC2 | 10.50 | |
| | ADC3 | 10.50 | |
| | TMR1 | 26.5 | |
| | TMR8 | 25.5 | |
| | SPI1 | 1.13 | |
| | USART1 | 8.00 | |
| | ALL_APB2 | 113.01 | |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.8. Wake-up time in low power mode

The measurement of wake-up time in low power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which $V_{DD}=V_{DDA}$.

Table 36 Wake Up Time in Low-power Mode

| Symbol | Parameter | Conditions | Typical value (T _A =25°C) | | | Maximum value | Unit |
|----------------------|----------------------------|--|--------------------------------------|-------|-------|---------------|------|
| | | | 2V | 3.3V | 3.6V | | |
| t _{WUSLEEP} | Wake-up from sleep mode | - | 1.13 | 1.32 | 1.36 | 1.43 | μs |
| t _{WUSTOP} | Wake up from shutdown mode | The voltage regulator is in run mode | 3.09 | 3.08 | 3.04 | 3.39 | |
| | | The voltage regulator is in low power mode | 5.74 | 4.43 | 4.26 | 6.34 | |
| t _{WUSTDBY} | Wake up from standby mode | - | 38.89 | 32.62 | 31.65 | 47.58 | |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.9. Pin characteristics

5.9.1. I/O pin characteristics

Table 37 DC Characteristics (test condition of V_{DD}=2.7~3.6V, T_A=-40~105°C)

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|------------------|---|--|---------------|----------------|---------------|------|
| V _{IL} | Low level input voltage | CMOS port | - | 1.40 | - | V |
| V _{IH} | High level input voltage | | 1.76 | - | 1.81 | |
| V _{IL} | Low level input voltage | TTL port | 1.25 | - | 1.39 | |
| V _{IH} | High level input voltage | | 1.58 | - | 1.74 | |
| V _{hys} | Standard I/O Schmitt trigger voltage hysteresis | - | 360 | - | - | mV |
| | I/O FT Schmitt trigger voltage hysteresis | | 330 | - | - | mV |
| I _{lkg} | Input leakage current | V _{SS} ≤ V _{IN} ≤ V _{DD} Standard I/O port | - | - | 0.16 | μA |
| | | V _{IN} =5V, I/O FT port | - | - | 0.16 | |
| R _{PU} | Weak pull-up equivalent resistance | V _{IN} =V _{SS} | 37 | 42 | 47 | kΩ |
| R _{PD} | Weak pull-down equivalent resistance | V _{IN} =V _{DD} | 37 | 42 | 47 | kΩ |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 38 AC Characteristics

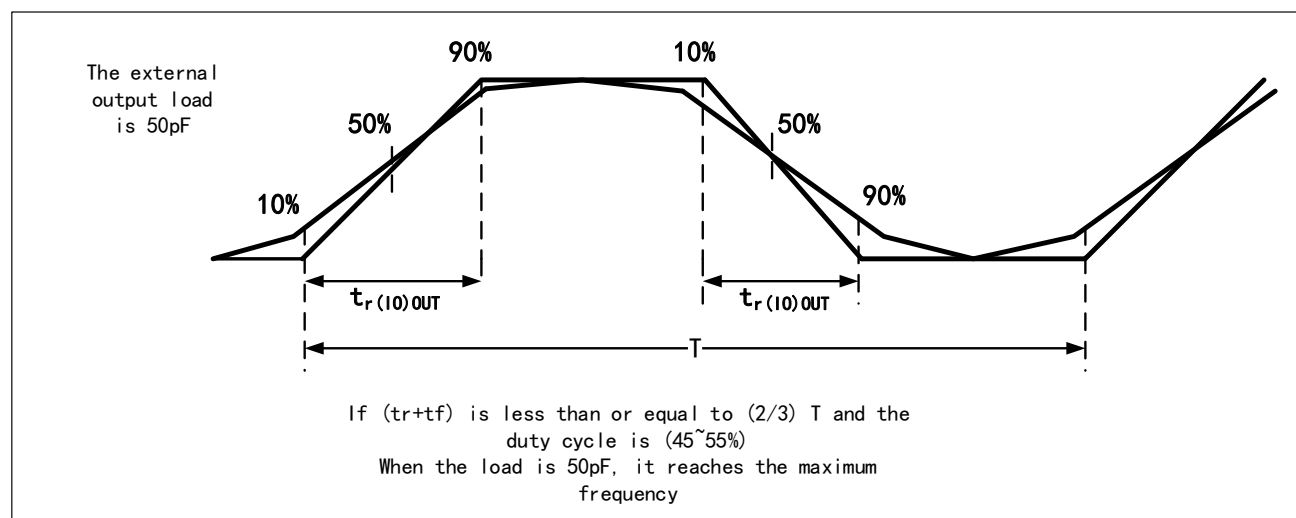
| MODEy[1:0] Configuration | Symbol | Parameter | Conditions | Minimum value | Maximum value | Unit |
|--------------------------|--------------------------------------|---|--------------------------------------|---------------|---------------|------|
| 10 (2MHz) | f _{max} (IO) _{out} | Maximum frequency | CL=50 pF, V _{DD} =2~3.6V | - | 2.00 | MHz |
| | t _f (IO) _{out} | Output fall time from high to low level | CL=50 pF, V _{DD} =2~3.6V | 11.52 | 26.81 | ns |
| | t _r (IO) _{out} | Output rise time from low to high level | | 9.24 | 21.90 | |
| 01 (10MHz) | f _{max} (IO) _{out} | Maximum frequency | CL=50 pF, V _{DD} =2~3.6V | - | 10.01 | MHz |
| | t _f (IO) _{out} | Output fall time from high to low level | CL=50 pF, V _{DD} =2~3.6V | 8.51 | 17.93 | ns |
| | t _r (IO) _{out} | Output rise time from low to high level | | 6.71 | 17.92 | |

| MODEy[1:0] Configuration | Symbol | Parameter | Conditions | Minimum value | Maximum value | Unit |
|--------------------------|-------------|---|--|---------------|---------------|------|
| 11 (50MHz) | fmax(IO)out | Maximum frequency | CL=30 pF, V _{DD} =2.7~3.6V | - | 50.25 | MHz |
| | tf(IO)out | Output fall time from high to low level | CL=30 pF, V _{DD} =2.7~3.6V | 7.65 | 9.69 | ns |
| | tr(IO)out | Output rise time from low to high level | | 3.79 | 6.48 | |

Note: (1) The rate of I/O port can be configured through MODEy.

(2) The data are obtained from a comprehensive evaluation and is not tested in production.

Figure 14 I/O AC Characteristics Definition



Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table39 Output Drive Current Characteristics (test condition V_{DD}=2.7~3.6V, T_A=-40~105°C)

| Symbol | Parameter | Conditions | Minimum value | Maximum value | Unit |
|-----------------|---|---|----------------------|---------------|------|
| V _{OL} | Output low level voltage for an I/O pin when 8 pins are sunk at same time | I _{IO} = +8mA 2.7V<V _{DD} <3.6V | - | 0.49 | V |
| V _{OH} | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | V _{DD} -0.4 | - | |
| V _{OL} | Output low level voltage for an I/O pin when 8 pins are sunk at same time | I _{IO} = +20mA 2.7V<V _{DD} <3.6V | - | 1.50 | V |
| V _{OH} | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | V _{DD} -1.2 | - | |

5.9.2. NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}.

Table 40 NRST Pin Characteristics (test condition V_{DD}=3.3V, T_A=-40~105°C)

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|------------------------|---|------------|---------------|----------------|---------------|------|
| V _{IL(NRST)} | NRST low level input voltage | - | 1.36 | 1.44 | 1.48 | V |
| V _{IH(NRST)} | NRST high level input voltage | - | 1.72 | 1.76 | 1.8 | |
| V _{hys(NRST)} | NRST Schmitt trigger voltage hysteresis | - | - | 290 | - | mV |

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|--------|------------------------------------|-------------------|---------------|----------------|---------------|------------|
| RPU | Weak pull-up equivalent resistance | $V_{IN} = V_{SS}$ | 30 | 40 | 53 | k Ω |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.10. Communication peripherals

5.10.1. I2C peripheral characteristics

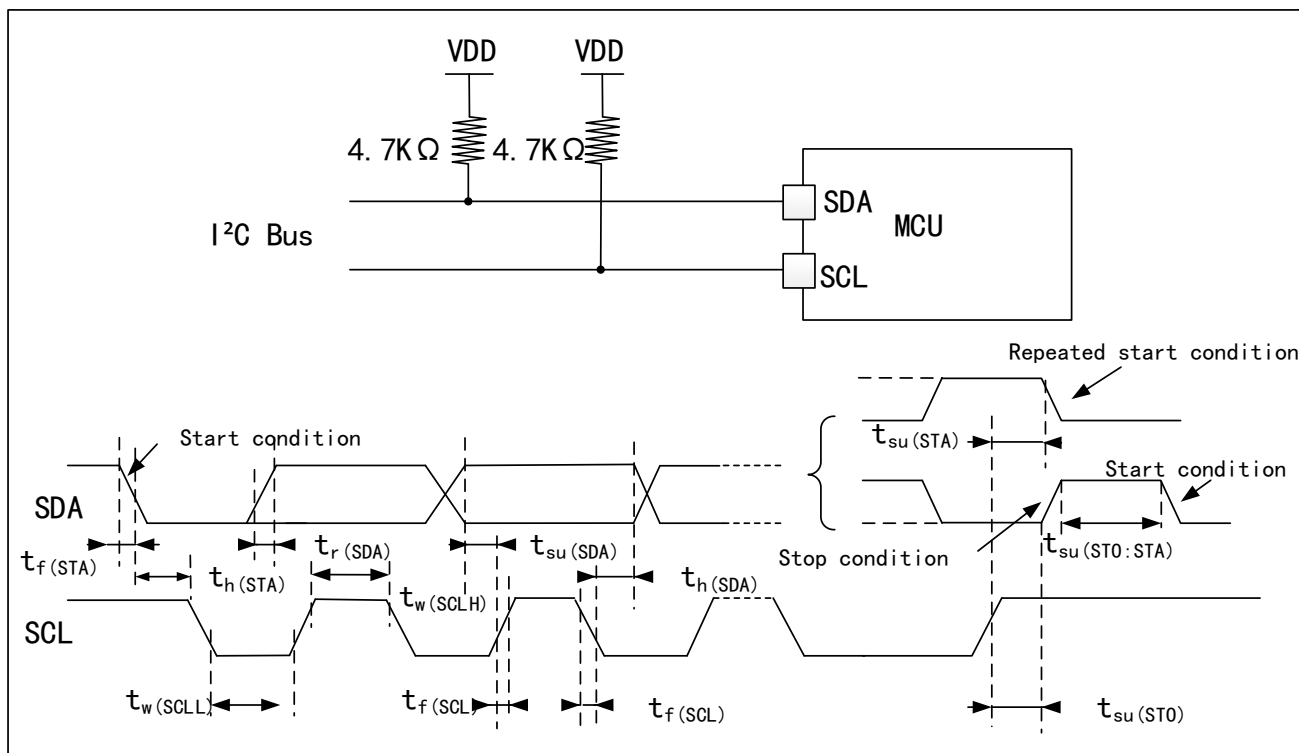
To achieve maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

Table 41 I2C Interface Characteristics ($T_A=25^{\circ}C$, $V_{DD}=3.3V$)

| Symbol | Parameter | Standard I2C | | Fast I2C | | Unit |
|---------------------|--|---------------|---------------|---------------|---------------|---------|
| | | Minimum value | Maximum value | Minimum value | Maximum value | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.88 | - | 1.77 | - | μs |
| $t_{w(SCLH)}$ | SCL clock high time | 5.10 | - | 0.72 | - | |
| $t_{su(SDA)}$ | SDA setup time | 1080 | - | 1000 | - | ns |
| $t_h(SDA)$ | SDA data hold time | 0 | 451.85 | 0 | 457.77 | |
| $t_r(SDA)/t_r(SCL)$ | SDA and SCL rise time | - | 381.63 | - | 389.56 | |
| $t_f(SDA)/t_f(SCL)$ | SDA and SCL fall time | - | 4.33 | - | 3.79 | |
| $t_h(STA)$ | Start condition hold time | 4.94 | - | 0.82 | - | μs |
| $t_{su(STA)}$ | Repeated start condition setup time | 4.99 | - | 0.81 | - | |
| $t_{su(STO)}$ | Setup time of stop condition | 4.92 | - | 0.81 | - | |
| $t_w(STO:STA)$ | Time from stop condition to start condition (bus idle) | 5.36 | - | 2.06 | - | |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 15 I2C Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.10.2. SPI peripheral characteristics

Table 42 SPI Characteristics ($T_A=25^{\circ}C$, $V_{DD}=3.3V$)

| Symbol | Parameter | Conditions | Minimum value | Maximum value | Unit |
|------------------------------|-------------------------------|--|---------------|---------------|------|
| f_{SCK} $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 18 | MHz |
| | | Slave mode | - | 10 | |
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SI clock rise and fall time | Load capacitance: $C = 30pF$ | - | 9.7 | ns |
| $t_{su(NSS)}$ | NSS setup time | Slave mode | 106.89 | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | 80.67 | - | ns |
| $t_w(SCKH)$ $t_w(SCKL)$ | SCK high and low time | Main mode, $f_{PCLK} = 36MHz$, Prescaler coefficient=4 | 54 | 57 | ns |
| $t_{su(MI)}$ $t_{su(SI)}$ | Data input setup time | Master mode | 17 | - | ns |
| | | Slave mode | 20.93 | - | |
| $t_{h(MI)}$ $t_{h(SI)}$ | Data input hold time | Master mode | 32.86 | - | ns |
| | | Slave mode | 25.11 | - | |
| $t_a(SO)$ | Data output access time | Slave mode, $f_{PCLK} = 20MHz$ | 6.48 | 8.08 | ns |
| $t_{dis(SO)}$ | Data output prohibition time | Slave mode | 14.28 | - | ns |
| $t_v(SO)$ | Effective time of data output | Slave mode (after enable edge) | - | 11.89 | ns |

| Symbol | Parameter | Conditions | Minimum value | Maximum value | Unit |
|-------------|-------------------------------|---------------------------------|---------------|---------------|------|
| $t_{v(MO)}$ | Effective time of data output | Master mode (after enable edge) | - | 5.4 | ns |
| $t_{h(SO)}$ | Data output hold time | Slave mode (after enable edge) | 9.5 | - | ns |
| $t_{h(MO)}$ | | Master mode (after enable edge) | 1.05 | - | |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 16 SPI Timing Diagram - Slave Mode and CPHA=0

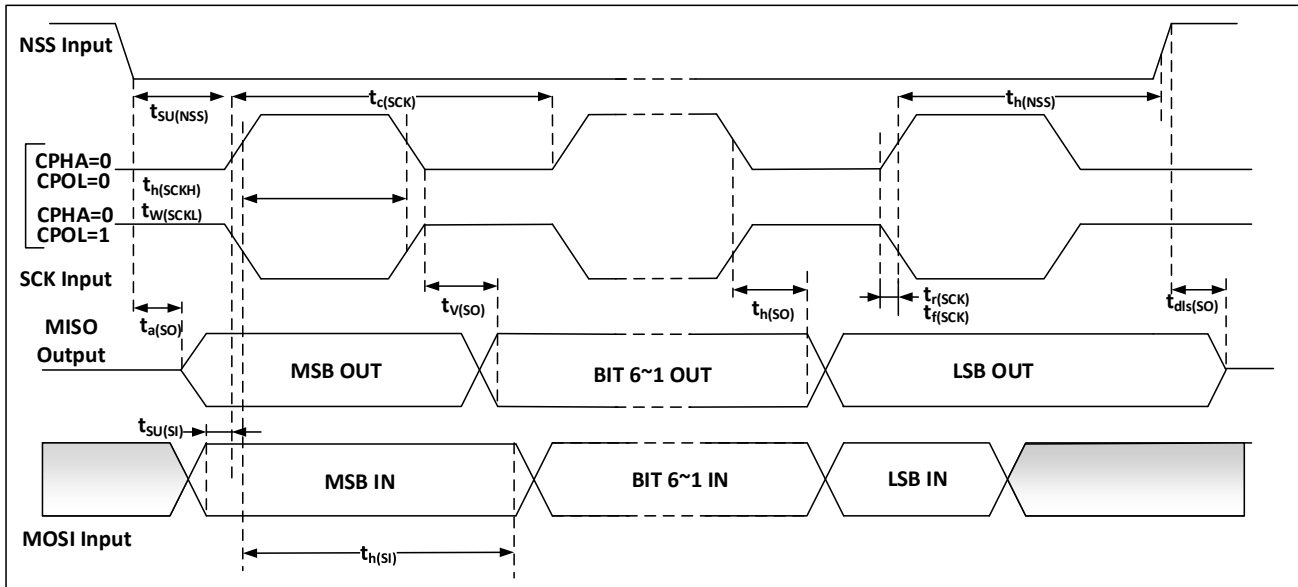
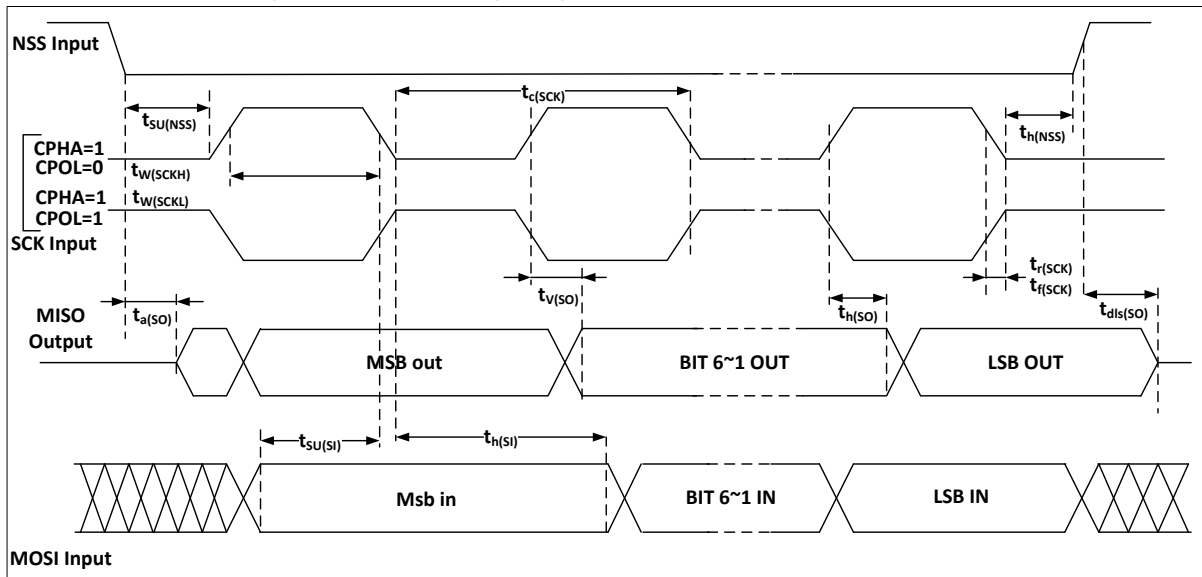
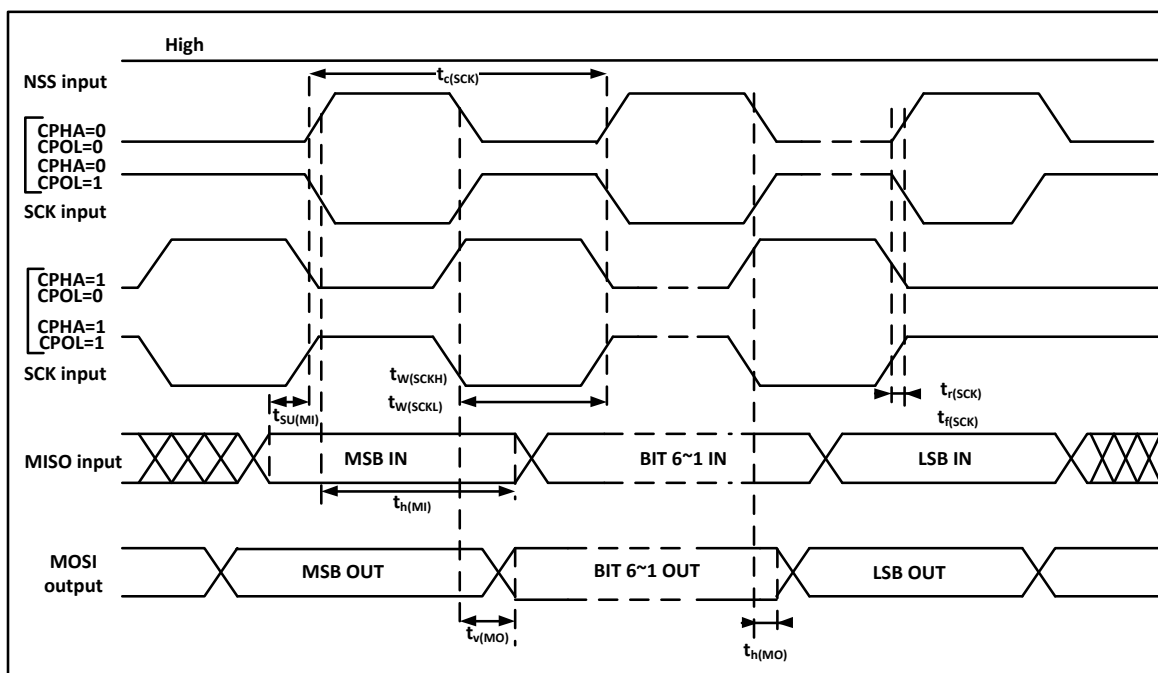


Figure 17 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 18 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

5.11. Analog peripherals

5.11.1. ADC

Test parameter description:

- Sampling rate: the number of conversion of analog quantity to digital quantity by ADC per second

$$\text{Sample rate} = \text{ADC clock} / (\text{number of sampling periods} + \text{number of conversion periods})$$

5.11.1.1. 12-bit ADC characteristics

Table 43 12-bit ADC Characteristics

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|-------------------|---|---|---------------|----------------|---------------|------|
| V _{DDA} | Power supply voltage | - | 2.4 | - | 3.6 | V |
| I _{DDA} | ADC power consumption | V _{DDA} =3.3V, f _{ADC} =14MHz, Sampling time=1.5 f _{ADC} | - | 1 | - | mA |
| f _{ADC} | ADC frequency | - | 0.6 | - | 14 | MHz |
| C _{ADC} | Internal sampling and holding capacitance | - | - | 8 | - | pF |
| R _{ADC} | Sampling resistor | - | - | - | 1000 | Ω |
| t _s | Sample Time | f _{ADC} =14MHz | 0.107 | - | 17.1 | μs |
| T _{CONV} | Sampling and conversion time | f _{ADC} =14MHz, 12-bit conversion | 1 | - | 18 | μs |

Table 44 12-bit ADC Accuracy

| Symbol | Parameter | Conditions | Typical values | Maximum value | Unit |
|--------|---------------------------|---|----------------|---------------|------|
| ET | Composite error | $f_{PCLK}=56M,$ $f_{ADC}=14M,$ $V_{DDA}=2.4V-3.6V$ $T_A=-40^{\circ}C\sim 105^{\circ}C$ | - | 5 | LSB |
| EO | Offset error | | - | 3.5 | |
| EG | Gain error | | - | 3 | |
| ED | Differential linear error | | - | 3 | |
| EL | Integral linear error | | - | 4 | |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.1.2. Test of Built-in Reference Voltage Characteristics

Table 45 Embedded Reference Voltage Characteristics

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|------------------|--|--|---------------|----------------|---------------|------------------|
| V_{REFINT} | Built-in Reference Voltage | $-40^{\circ}C < T_A <$ $+105^{\circ}C$ $V_{DD}= 2-3.6 V$ | 1.2 | 1.23 | 1.26 | V |
| $T_{S_vrefint}$ | Sampling time of ADC when reading out internal reference voltage | - | - | 5.1 | 17.1 | μs |
| V_{RERINT} | Built-in reference voltage extends to temperature range | $V_{DD}=3V \pm 10mV$ | - | - | 18 | mV |
| T_{coeff} | Temperature coefficient | - | - | - | 104 | ppm/ $^{\circ}C$ |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.2. DAC

Test parameter description:

- DNL differential non-linear error: the deviation between two consecutive codes is-1 LSB
- INL integral non-linear error: the difference between the measured value at code i and the value at code i on the connection between code 0 and the last code 4095

Table 46 DAC Characteristics

| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|------------|-----------------------------|---|---------------|----------------|---------------|------------|
| V_{DDA} | Analog power supply voltage | - | 2.4 | - | 3.6 | V |
| R_{LOAD} | Resistive load | Load is connected to VSSA with buffer on | 5 | - | - | k Ω |
| R_o | Output impedance | The resistive load between DAC_OUT and VSS is 1.5M Ω with buffer off | - | - | 15 | k Ω |

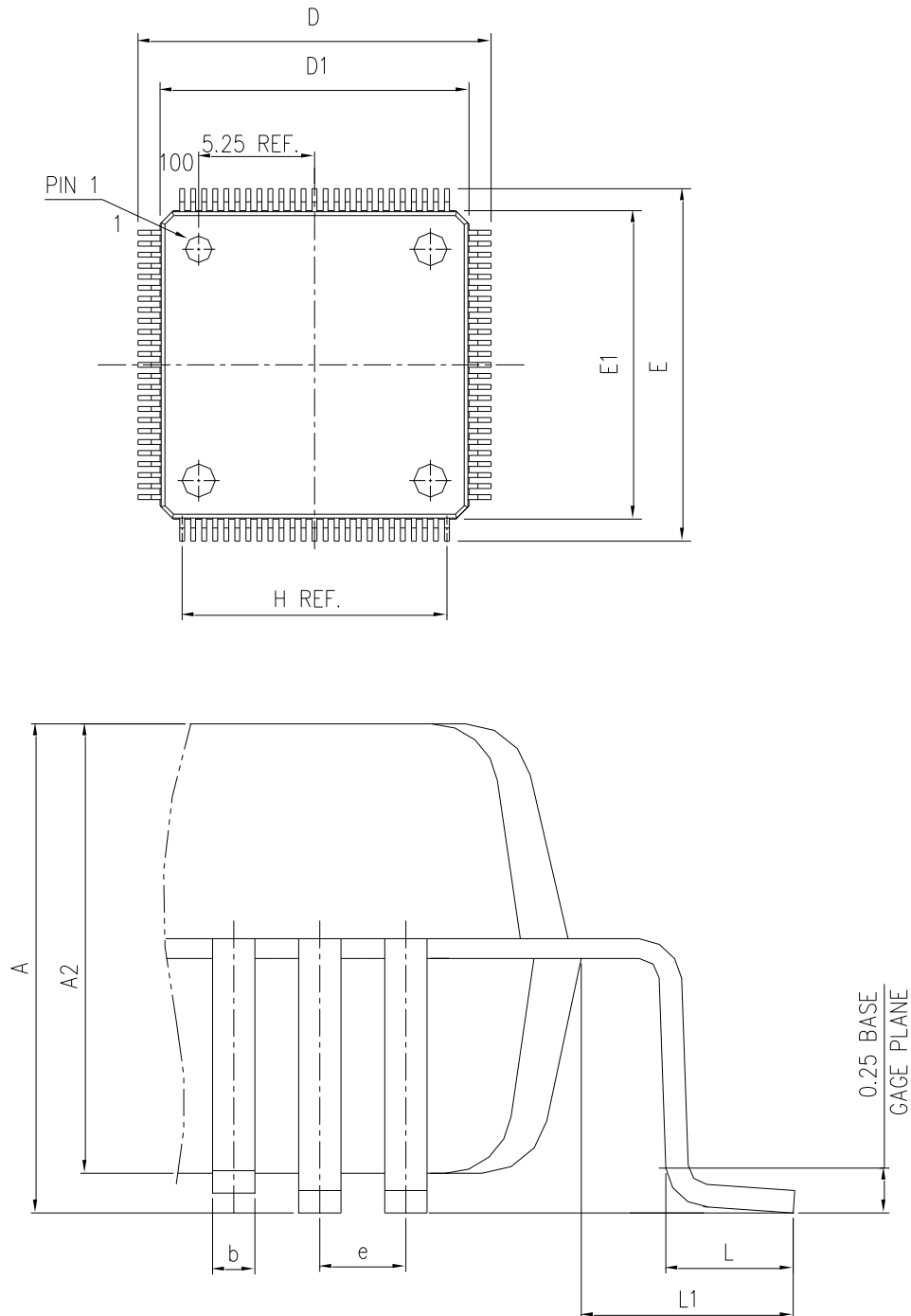
| Symbol | Parameter | Conditions | Minimum value | Typical values | Maximum value | Unit |
|------------------------|--|---|---------------|----------------|-----------------------|------|
| C _{LOAD} | Capacitive load | Maximum capacitive load at DAC_OUT pin with buffer on | - | - | 50 | pF |
| DAC_OUT _{min} | Low DAC_OUT voltage with buffer | Maximum output offset of DAC, (0x0E1) corresponding to 12-bit input code to V _{REF+} = (0xF1B) at 3.6V and V _{REF+} = (0x154) at 2.4V and (0xEAC) | 0.2 | - | - | V |
| DAC_OUT _{max} | High output voltage with buffer | | - | - | V _{DDA} -0.2 | V |
| I _{DDA} | Power consumption of DAC in quiescent mode | Non-load, the input terminal adopts intermediate code (0x800) | - | - | 295 | uA |
| | | Non-load, the input terminal adopts difference code (0xF1C) | - | - | 340 | uA |
| DNL | Differential non-linear error | Configured with 12-bit DAC | - | - | ±2 | LSB |
| INL | Integral non-linear error | Configured with 12-bit DAC | - | - | ±8 | LSB |
| Offset | Offset error | V _{REF+} =3.6V, configuring 12-bit DAC | - | - | ±4 | LSB |
| Gain error | Gain error | Configured with 12-bit DAC | - | - | ±0.4 | % |

Note: It is obtained from a comprehensive evaluation and is not tested in production.

6. Package information

6.1. LQFP100 package diagram

Figure 19 LQFP100 Package Diagram



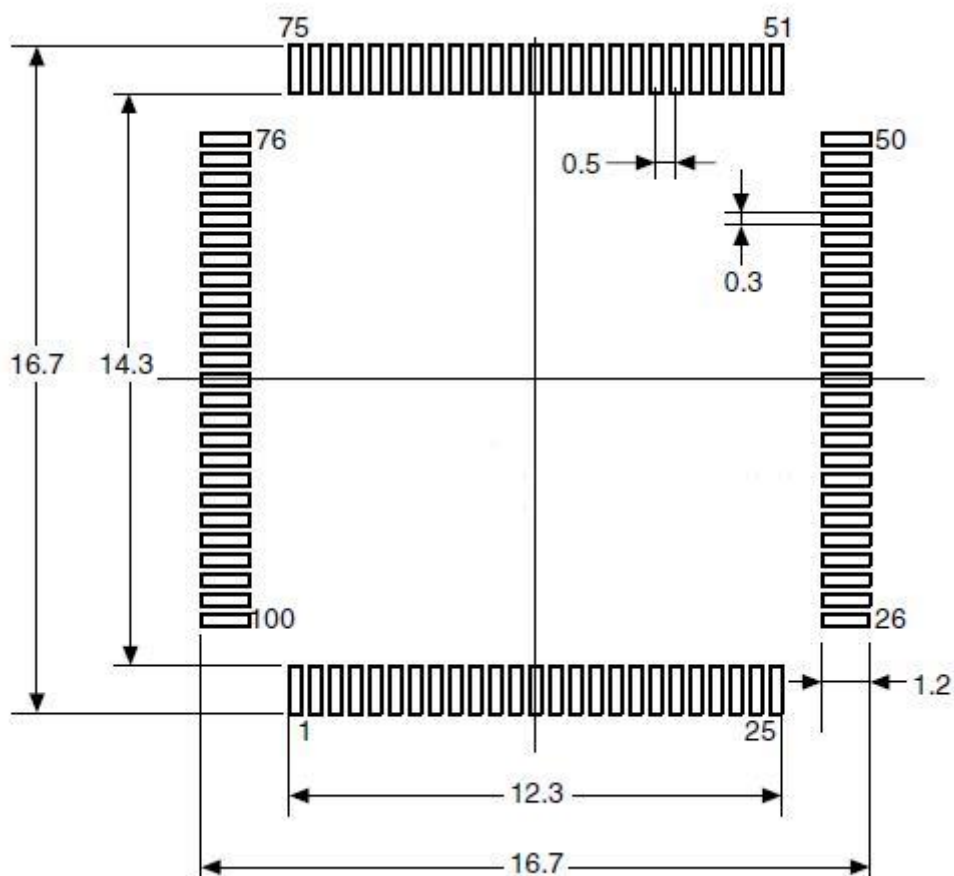
- (1) The figure is not drawn to scale.
- (1) All pins should be soldered to the PC

Table 47 LQFP100 Package Data

| DIMENSION LIST (FOOTPRINT: 2.00) | | | |
|----------------------------------|---------|--------------|-----------------|
| S/N | SYM | DIMENSIONS | REMARKS |
| 1 | A | MAX. 1.600 | OVERALL HEIGHT |
| 2 | A2 | 1.400±0.050 | PKG THICKNESS |
| 3 | D | 16.000±0.200 | LEAD TIP TO TIP |
| 4 | D1 | 14.000±0.100 | PKG LENGTH |
| 5 | E | 16.000±0.200 | LEAD TIP TO TIP |
| 6 | E1 | 14.000±0.100 | PKG WPTH |
| 7 | L | 0.600±0.150 | FOOT LENGTH |
| 8 | L1 | 1.000 REF | LEAD LENGTH |
| 9 | e | 0.500 BASE | LEAD PITCH |
| 10 | H (REF) | (12.00) | CUM LEAD PITCH |
| 11 | b | 0.22±0.050 | LEAD WIDTH |

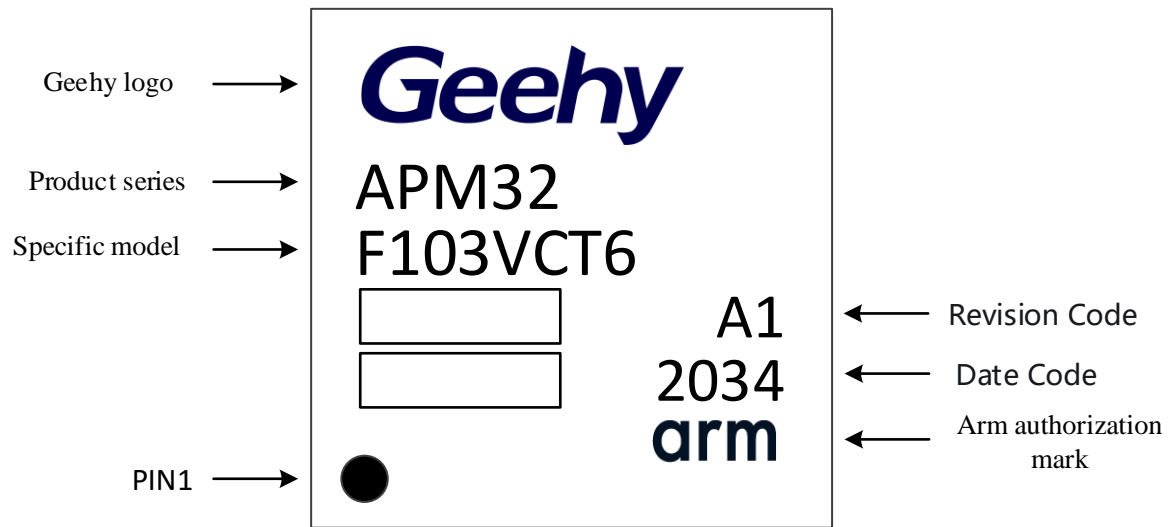
(1) Dimensions are displayed in mm

Figure 20 LQFP100-100 pins, 14×14mm recommended welding Layout



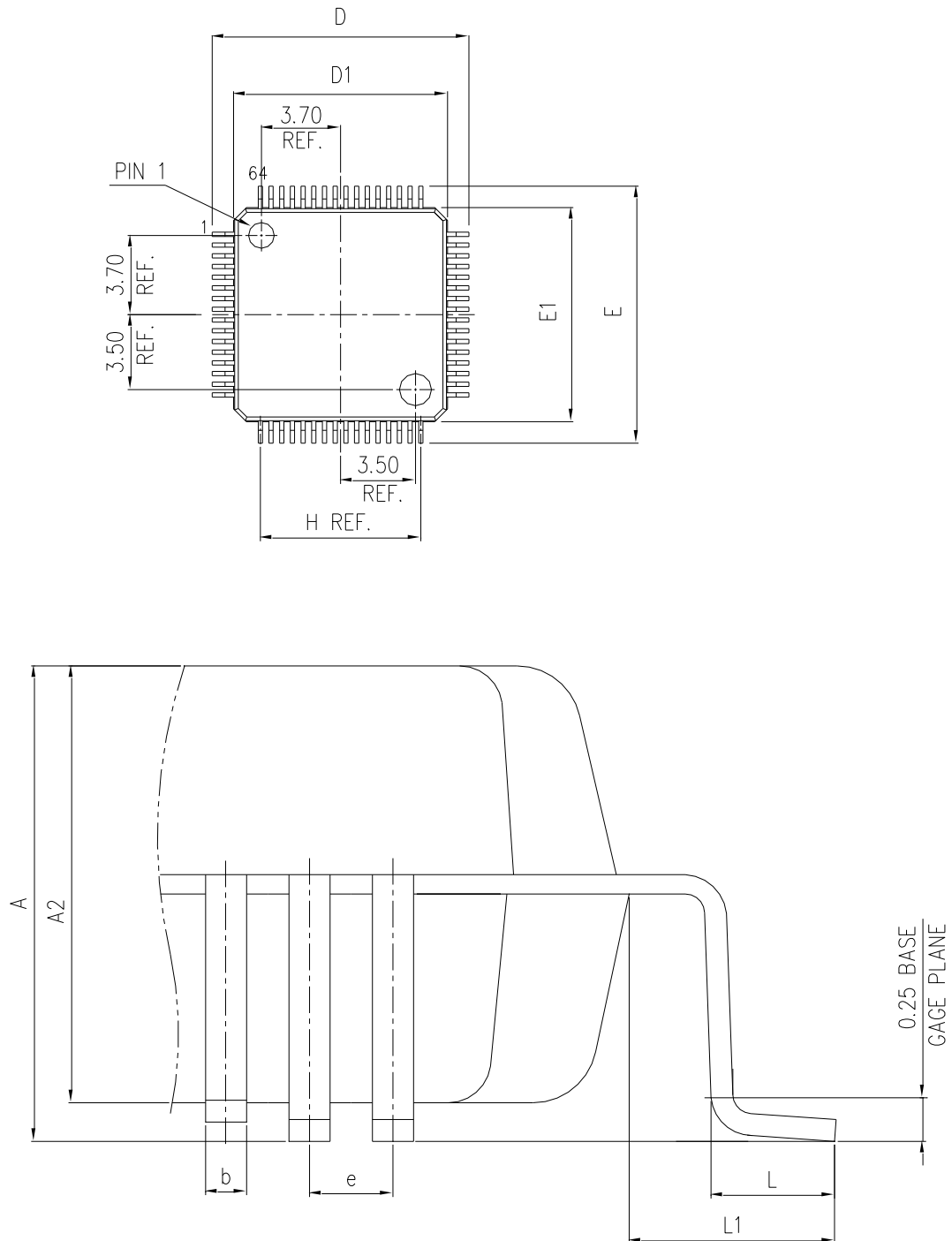
(1) Dimensions are expressed in mm

Figure 21LQFP100-100 pins, 14×14mm package identification



6.2. LQFP64 package diagram

Figure 22 LQFP64 Package Diagram



- (1) The figure is not drawn to scale.
- (2) All pins should be soldered to the PCB

Table 48 LQFP64 Package Data

| DIMENSION LIST (FOOTPRINT: 2.00) | | | |
|----------------------------------|---------|--------------|-----------------|
| S/N | SYM | DIMENSIONS | REMARKS |
| 1 | A | MAX. 1.600 | OVERALL HEIGHT |
| 2 | A2 | 1.400±0.050 | PKG THICKNESS |
| 3 | D | 12.000±0.200 | LEAD TIP TO TIP |
| 4 | D1 | 10.000±0.100 | PKG LENGTH |
| 5 | E | 12.000±0.200 | LEAD TIP TO TIP |
| 6 | E1 | 10.000±0.100 | PKG WPTH |
| 7 | L | 0.600±0.150 | FOOT LENGTH |
| 8 | L1 | 1.000 REF | LEAD LENGTH |
| 9 | e | 0.500 BASE | LEAD PITCH |
| 10 | H (REF) | (7.500) | CUM LEAD PITCH |
| 11 | b | 0.22±0.050 | LEAD WIDTH |

(1) Dimensions are expressed in mm

Figure 23 LQFP64-64 pins, 10×10mm recommended welding Layout

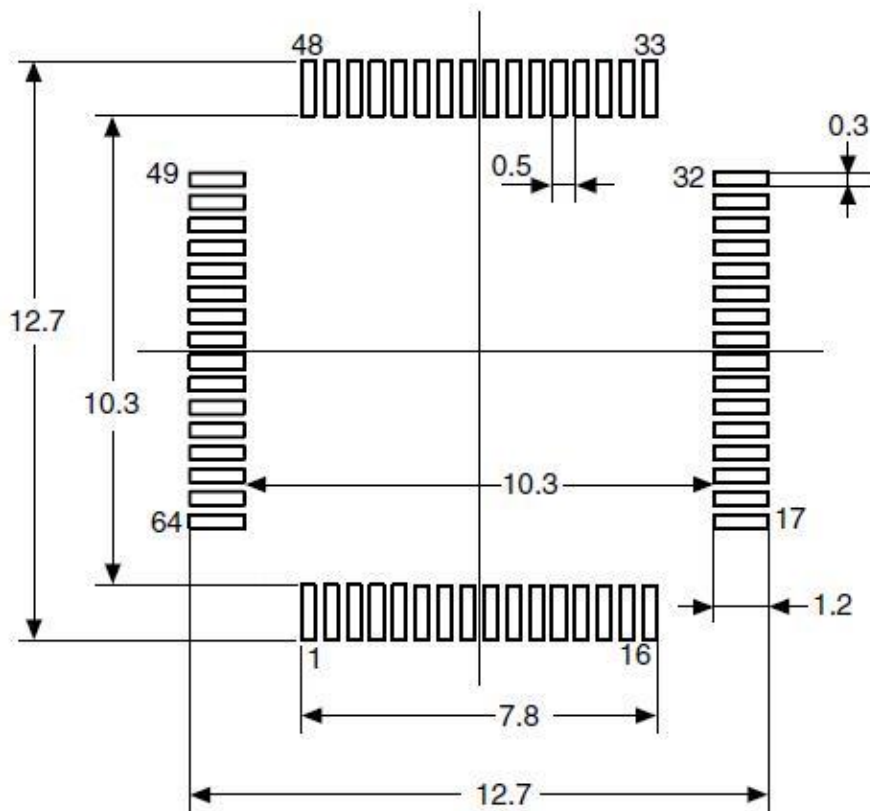
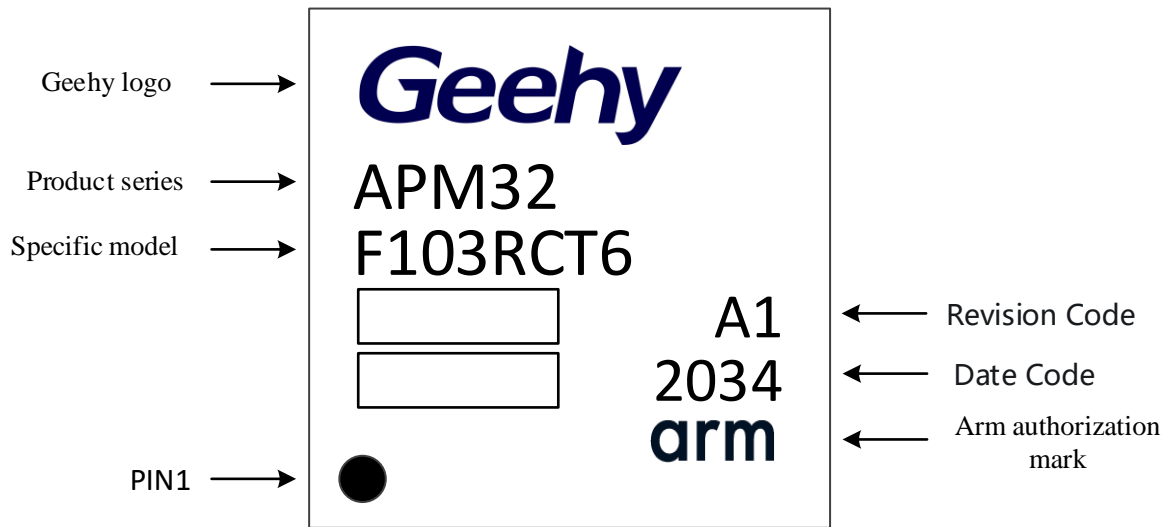
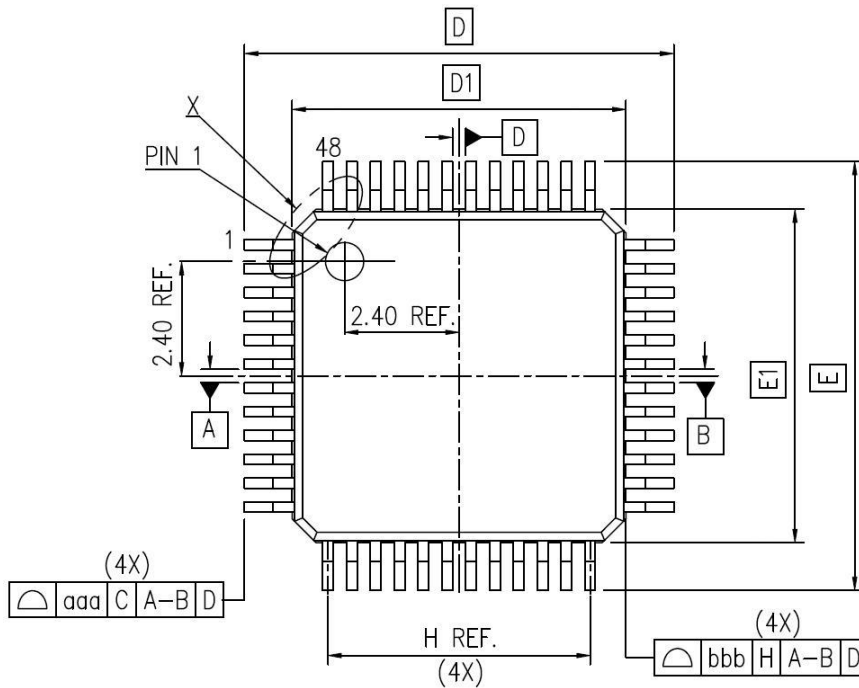


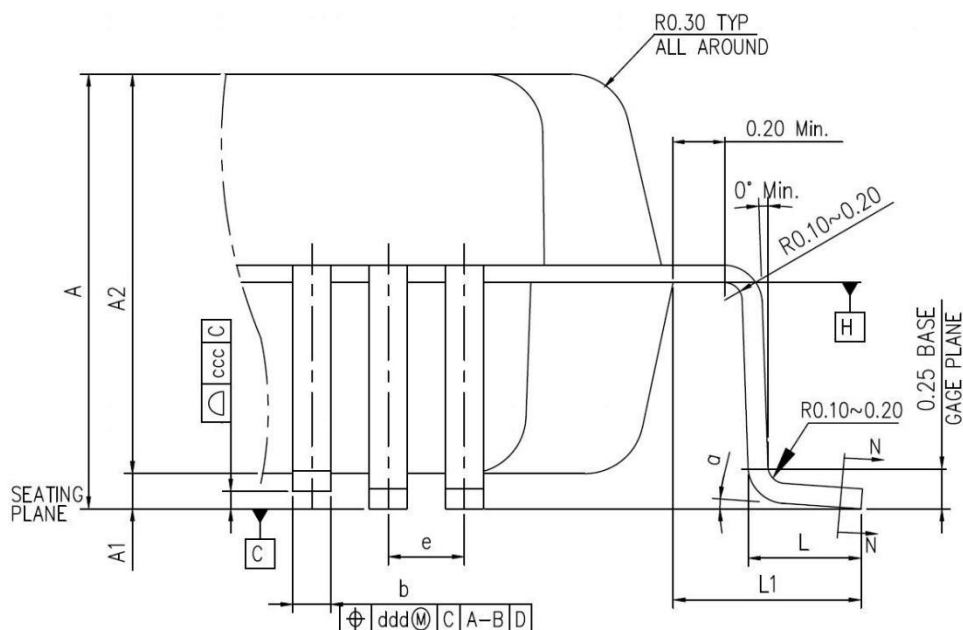
Figure 24 LQFP64-64 pins, 10×10mm package identification



6.3. LQFP48 Package Diagram

Figure 25 LQFP48 Package Diagram





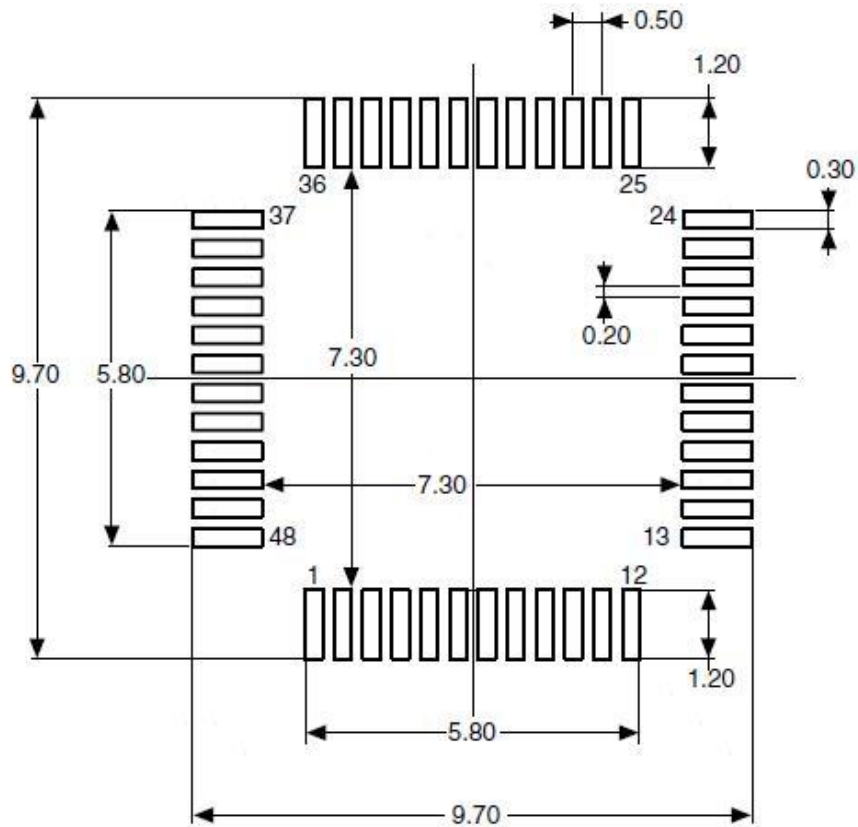
- (1) The figure is not drawn to scale.
- (2) All pins should be soldered to the PCB

Table 49 LQFP48 Package Data

| DIMENSION LIST(FOOTPRINT: 2.00) | | | |
|---------------------------------|---------|------------|---------------------------|
| S/N | SYM | DIMENSIONS | REMARKS |
| 1 | A | MAX. 1.60 | OVERALL HEIGHT |
| 2 | A1 | 0.1±0.05 | STANDOFF |
| 3 | A2 | 1.40±0.05 | PKG THICKNESS |
| 4 | D | 9.00±0.20 | LEAD TIP TO TIP |
| 5 | D1 | 7.00±0.10 | PKG LENGTH |
| 6 | E | 9.00±0.20 | LEAD TIP TO TIP |
| 7 | E1 | 7.00±0.10 | PKG WIDTH |
| 8 | L | 0.60±0.15 | FOOT LENGTH |
| 9 | L1 | 1.00 REF | LEAD LENGTH |
| 10 | T | 0.15 | LEAD THICKNESS |
| 11 | T1 | 0.127±0.03 | LEAD BASE METAL THICKNESS |
| 12 | a | 0°~7° | FOOT ANGLE |
| 13 | b | 0.22±0.02 | LEAD WIDTH |
| 14 | b1 | 0.20±0.03 | LEAD BASE METAL WIDTH |
| 15 | e | 0.50 BASE | LEAD PITCH |
| 16 | H(REF.) | (5.50) | CUM. LEAD PITCH |
| 17 | aaa | 0.2 | PROFILE OF LEAD TIPS |
| 18 | bbb | 0.2 | PROFILE OF MOLD SURFACE |
| 19 | ccc | 0.08 | FOOT COPLANARITY |
| 20 | ddd | 0.08 | FOOT POSITION |

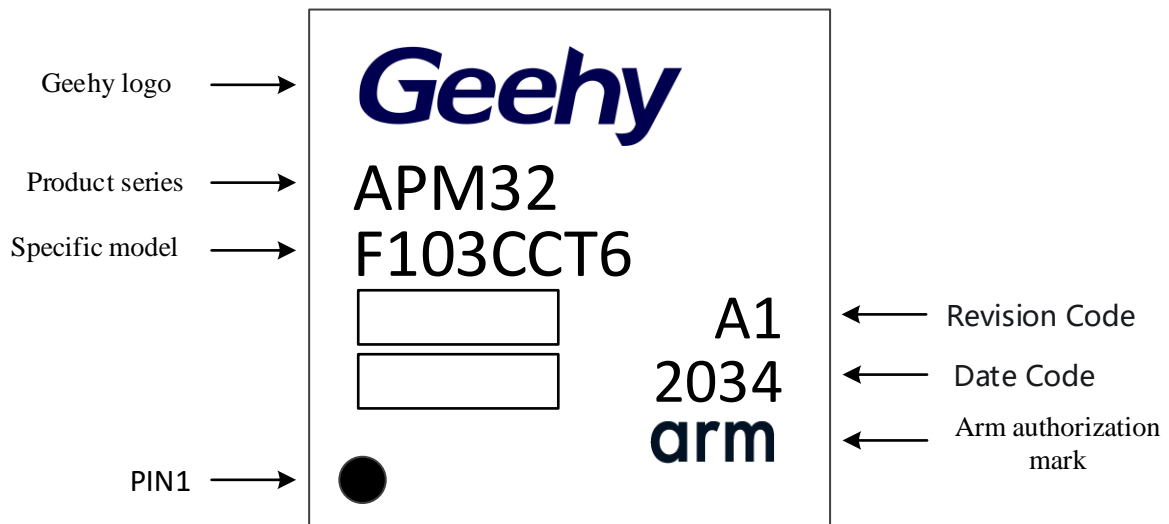
- (1) Dimensions are expressed in mm

Figure 26 LQFP48, 7×7mm recommended welding Layout



(1) Dimensions are expressed in mm

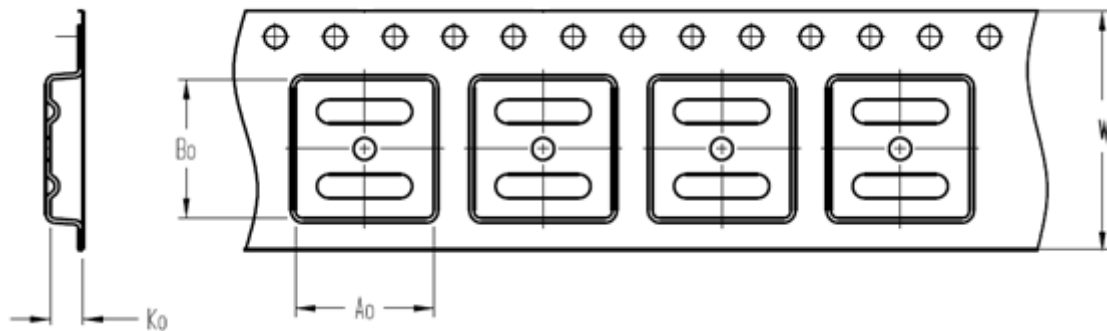
Figure 27 LQFP48-48 pins, 7×7mm identification diagram



7. Packaging information

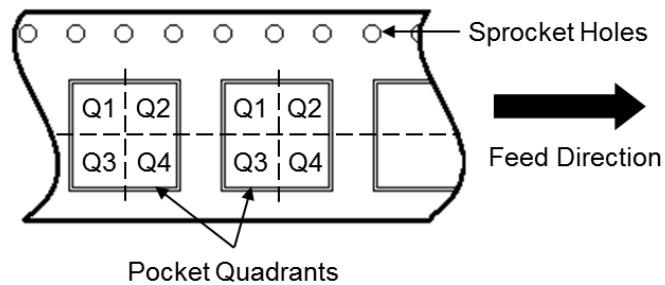
7.1. Reel packaging

Figure 28 Specification Drawing of Reel Packaging

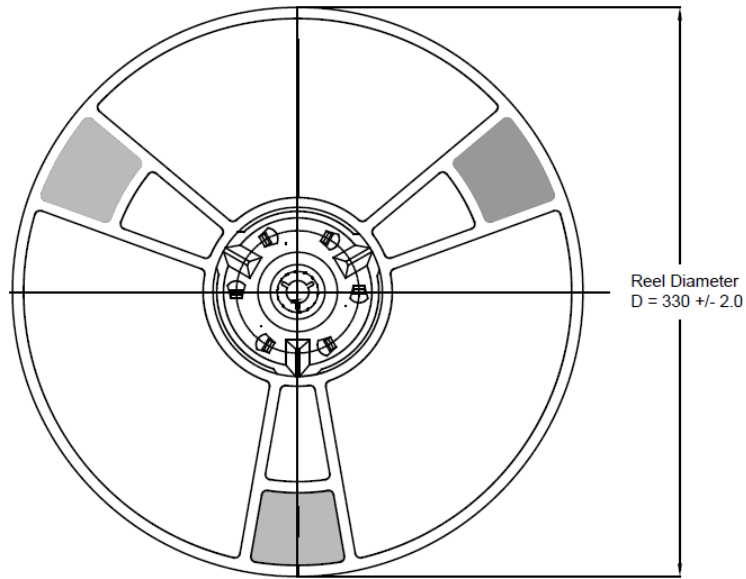


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



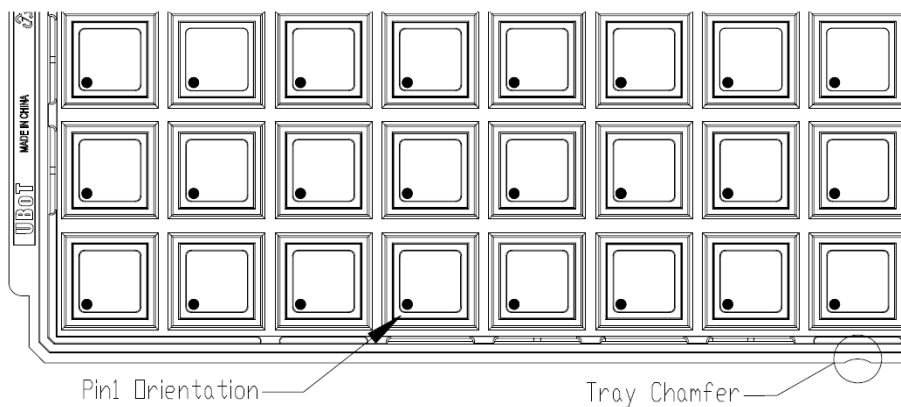
All photos are for reference only, and the appearance is subject to the product.

Table 50 Reel Packaging Parameter Specification Table

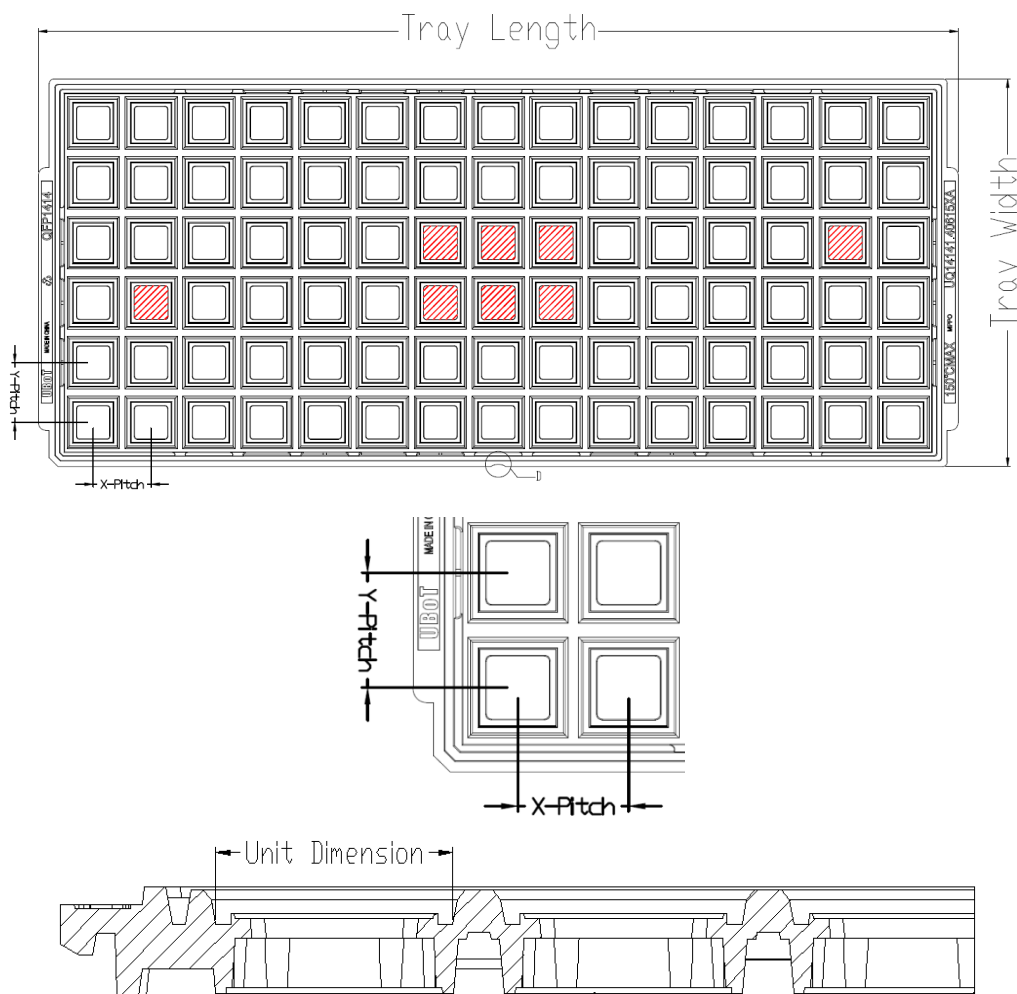
| Device | Package Type | Pins | SPQ | Reel Diameter (mm) | A0 (mm) | B0 (mm) | K0 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|------|------|--------------------|---------|---------|---------|--------|---------------|
| APM32F103RCT6 | LQFP | 64 | 1000 | 330 | 12.35 | 12.35 | 2.2 | 24 | Q1 |
| APM32F103CCT6 | LQFP | 48 | 2000 | 330 | 9.3 | 9.3 | 2.2 | 16 | Q1 |
| APM32F103RCT7 | LQFP | 64 | 1000 | 330 | 12.35 | 12.35 | 2.2 | 24 | Q1 |
| APM32F103CCT7 | LQFP | 48 | 2000 | 330 | 9.3 | 9.3 | 2.2 | 16 | Q1 |

7.2. Tray packaging

Figure 29 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product.

Table 51 Tray Packaging Parameter Specification Table

| Device | Package Type | Pins | SPQ | X-Dimension (mm) | Y-Dimension (mm) | X-Pitch (mm) | Y-Pitch (mm) | Tray Length (mm) | Tray Width (mm) |
|----------------|--------------|------|------|------------------|------------------|--------------|--------------|------------------|-----------------|
| APM32E103VCT6S | LQFP | 100 | 900 | 16.6 | 16.6 | 20.3 | 21 | 322.6 | 135.9 |
| APM32E103VCT6 | LQFP | 100 | 900 | 16.6 | 16.6 | 20.3 | 21 | 322.6 | 135.9 |
| APM32F103RCT6 | LQFP | 64 | 1600 | 12.3 | 12.3 | 15.2 | 15.7 | 322.6 | 135.9 |
| APM32F103CCT6 | LQFP | 48 | 2500 | 9.7 | 9.7 | 12.2 | 12.6 | 322.6 | 135.9 |
| APM32E103VCT7S | LQFP | 100 | 900 | 16.6 | 16.6 | 20.3 | 21 | 322.6 | 135.9 |
| APM32E103VCT7 | LQFP | 100 | 900 | 16.6 | 16.6 | 20.3 | 21 | 322.6 | 135.9 |
| APM32F103RCT7 | LQFP | 64 | 1600 | 12.3 | 12.3 | 15.2 | 15.7 | 322.6 | 135.9 |
| APM32F103CCT7 | LQFP | 48 | 2500 | 9.7 | 9.7 | 12.2 | 12.6 | 322.6 | 135.9 |

8. Ordering information

Figure 30 Product Naming Rules

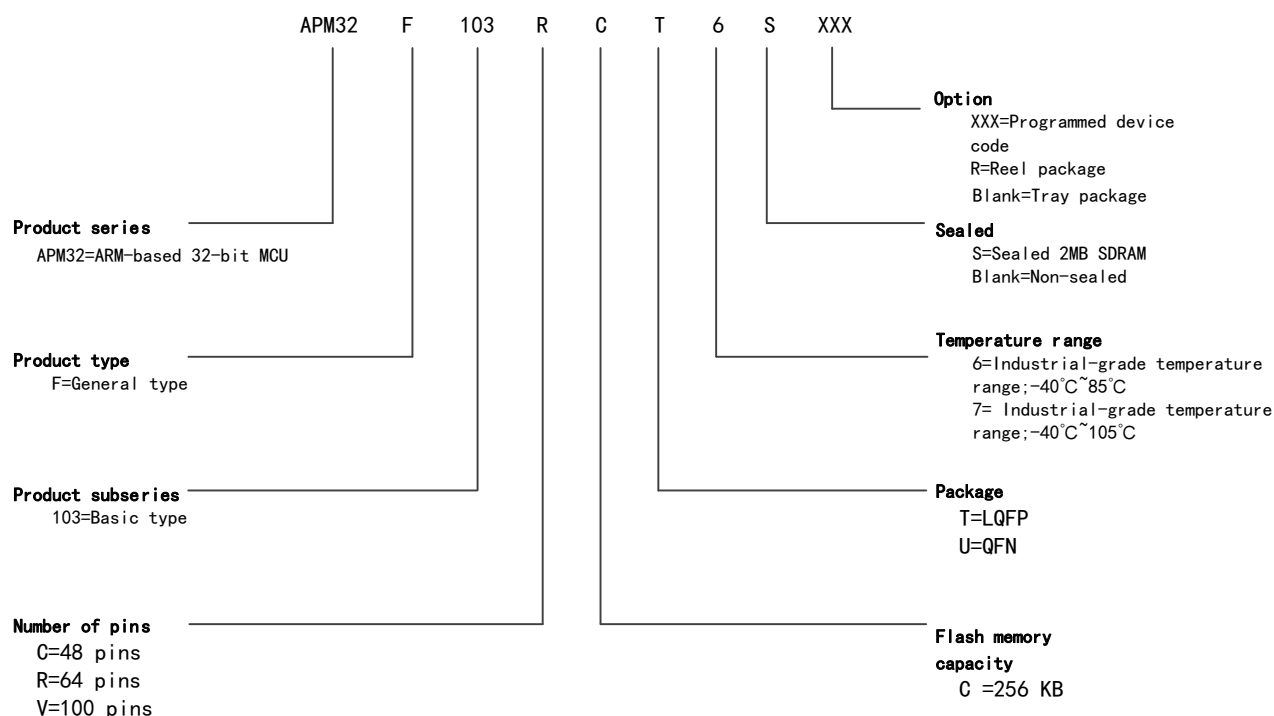


Table 52 Ordering Information Table

| Order Code | Flash (KB) | SRAM (KB) | Package | SPQ | Temperature Range |
|-----------------|------------|-----------|---------|------|------------------------------|
| APM32F103CCT6-R | 256 | 64 | LQFP48 | 2000 | Industrial grade -40°C~85°C |
| APM32F103CCT6 | 256 | 64 | LQFP48 | 2500 | Industrial grade -40°C~85°C |
| APM32F103RCT6-R | 256 | 64 | LQFP64 | 1000 | Industrial grade -40°C~85°C |
| APM32F103RCT6 | 256 | 64 | LQFP64 | 1600 | Industrial grade -40°C~85°C |
| APM32F103VCT6 | 256 | 64 | LQFP100 | 900 | Industrial grade -40°C~85°C |
| APM32F103VCT6S | 256 | 64 | LQFP100 | 900 | Industrial grade -40°C~85°C |
| APM32F103CCT7-R | 256 | 64 | LQFP48 | 2000 | Industrial grade -40°C~105°C |
| APM32F103CCT7 | 256 | 64 | LQFP48 | 2500 | Industrial grade -40°C~105°C |
| APM32F103RCT7-R | 256 | 64 | LQFP64 | 1000 | Industrial grade -40°C~105°C |
| APM32F103RCT7 | 256 | 64 | LQFP64 | 1600 | Industrial grade -40°C~105°C |
| APM32F103VCT7 | 256 | 64 | LQFP100 | 900 | Industrial grade -40°C~105°C |
| APM32F103VCT7S | 256 | 64 | LQFP100 | 900 | Industrial grade -40°C~105°C |

Note :SPQ= Minimum number of packages

9. Commonly used function module denomination

Table 53 Commonly Used Function Module Denomination

| Chinese description | Short name |
|---|------------|
| Reset management unit | RMU |
| Clock management unit | CMU |
| Reset and clock management | RCM |
| External interrupt | EINT |
| Genera-purpose IO | GPIO |
| Multiplexing IO | AFIO |
| Wake up controller | WUPT |
| Buzzer | BUZZER |
| Independent watchdog timer | IWDT |
| Window watchdog timer | WWDT |
| Timer | TMR |
| CRC controller | CRC |
| Power Management Unit | PMU |
| DMA controller | DMA |
| Analog-to-digital converter | ADC |
| Real-time clock | RTC |
| External memory controller | EMMC |
| Controller local area network | CAN |
| I2C interface | I2C |
| Serial peripheral interface | SPI |
| Universal asynchronous transmitter receiver | UART |
| Universal synchronous and asynchronous transmitter receiver | USART |
| Flash interface control unit | FMC |

10. Revision history

Table 54 Document Revision History

| Date | Revision | Change |
|------------------|----------|--|
| January 10, 2021 | 1.0 | New |
| May 20, 2021 | 1.1 | (1) Modify the header, front and back cover and the logo of the package drawing (2) Increase ESD and power consumption data of APM32F103xCTxS |
| June 30, 2021 | 1.2 | Add Maximum Rated Current Features |