Synchronous Buck-Boost DC/DC Converter with 2 A Switches (V_{IN} = 2.0 V to 5.5 V, 1ch)

BD83070GWL

General Description

The BD83070GWL is a synchronous buck-boost DC/DC convertor providing 3.3 V or 2.5 V output from single-cell Li-ion battery or other input between 2.0 V and 5.5 V. It has the capability to support up to 1 A output over input voltage range of 2.7 V to 5.5 V. It seamlessly changes between buck and boost operations depending on the input voltage.
It is based on pulse width modulation (PWM) and provides high efficiency for heavy load. While in PWM operation, internal FETs switch at fixed frequency 1.5 MHz typical. It automatically changes over control system to hysteresis pulse frequency modulation (PFM) to suppress switching loss and current consumption during light load. Battery drain fall down to only 2.8 µA typical at no load current. It is possible to disable auto-PFM/PWM mode by the MODE pin for suppressing output ripple and fixed frequency switching.
The device is packaged in a 1.2 mm x 1.6 mm WLCSP package.

Features

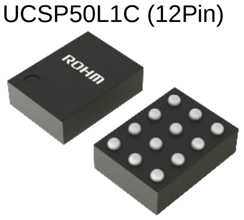
- Synchronous Buck-Boost DC/DC Converter
- Automatic PFM/PWM Transition
- Output Current: Up To 1 A (V_{IN} > 2.7 V, V_{OUT} = 3.3 V)
- Selectable Output Voltage: 2.5 V or 3.3 V
- Efficiency: Up To 95 %
- UVLO Detection: 1.61 V(Max)
- Built-in Thermal, Over Voltage, And Over Current Protection

Key Specifications

- Input Voltage Range: 2.0 V to 5.5 V
- Output Voltage: 2.5 V or 3.3 V
- Output Current: 1 A(Max)
- Switching Frequency: 1.5 MHz(Typ)
- Quiescent VIN Current: 2.8 µA(Typ)
- Operating Temperature Range: -40 °C to +85 °C

Package

Package	W(Typ) x D(Typ) x H(Max)
UCSP50L1C (12Pin)	1.20 mm × 1.60 mm × 0.57 mm



Applications

- Single Cell Li-ion or 3 Cell NiMH Battery-Powered Portable Products
- Tablet Terminal Device
- Smartphone

Typical Application Circuit

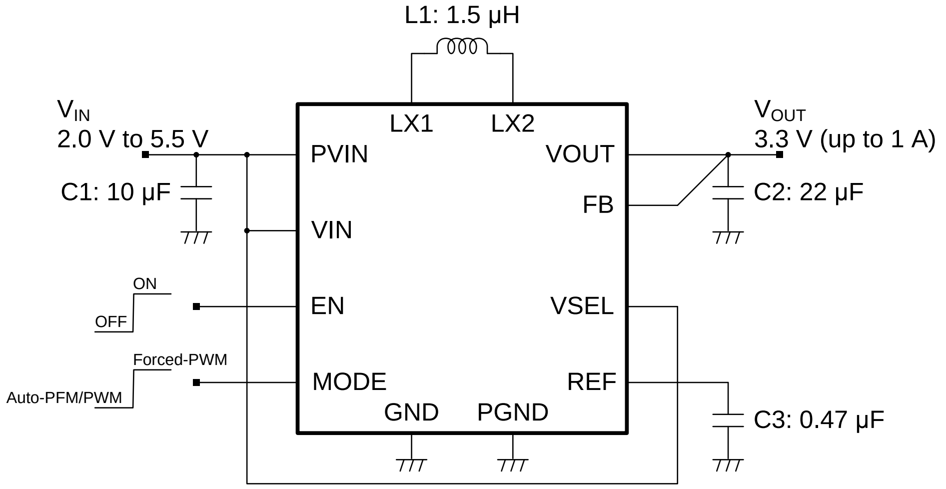


Figure 1. Typical Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

Contents

Pin Configuration

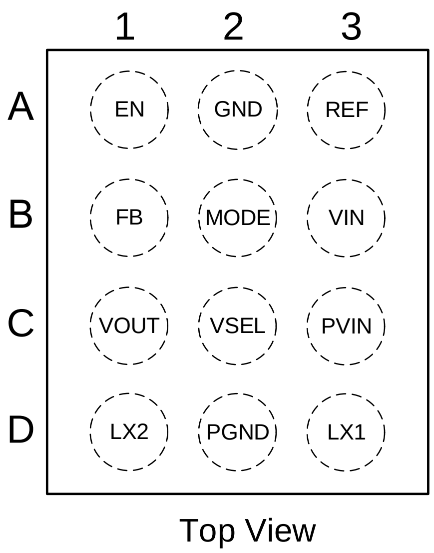


Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Function
A1	EN	Enable pin of the DC/DC converter. Inputting high (≥ 1.2 V) the EN pin turns on the regulator. Inputting low (≤ 0.4 V) or open the EN pin turns off the regulator.
A2	GND	Ground for sensing
A3	REF	Linear regulator output for power supply of internal circuits. Connect ceramic capacitor (0.47 μF) between this pin and the GND pin for output stability. Do not connect the other devices.
B1	FB	Voltage feedback pin. Connect this pin to the VOUT pin.
B2	MODE	Mode selection pin. Low (≤ 0.4 V): Auto-PFM/PWM mode. High (≥ 1.2 V): Forced-PWM mode. Do not leave this pin floating.
B3	VIN	Power supply input of controller. Connect this pin to the PVIN pin.
C1	VOUT	Output pin of the DC/DC converter. Connect ceramic capacitor (22 μF recommended) between this pin and the PGND pin for output stability.
C2	VSEL	Output voltage selection pin. High (V_{IN}): 3.3 V. Low (GND): 2.5 V. Connect this pin to either the VIN pin or the GND pin.
C3	PVIN	Power supply input of the DC/DC converter and LX1 side gate drivers. Connect ceramic capacitor (≥ 10 μF) between this pin and the PGND pin for power supply noise reduction.
D1	LX2	Inductor connection pin. Connect inductor (1.5 μH) between this pin and the LX1 pin.
D2	PGND	Ground of power FET, discharge, and gate drivers.
D3	LX1	Inductor connection pin. Connect inductor (1.5 μH) between this pin and the LX2 pin.

Block Diagram

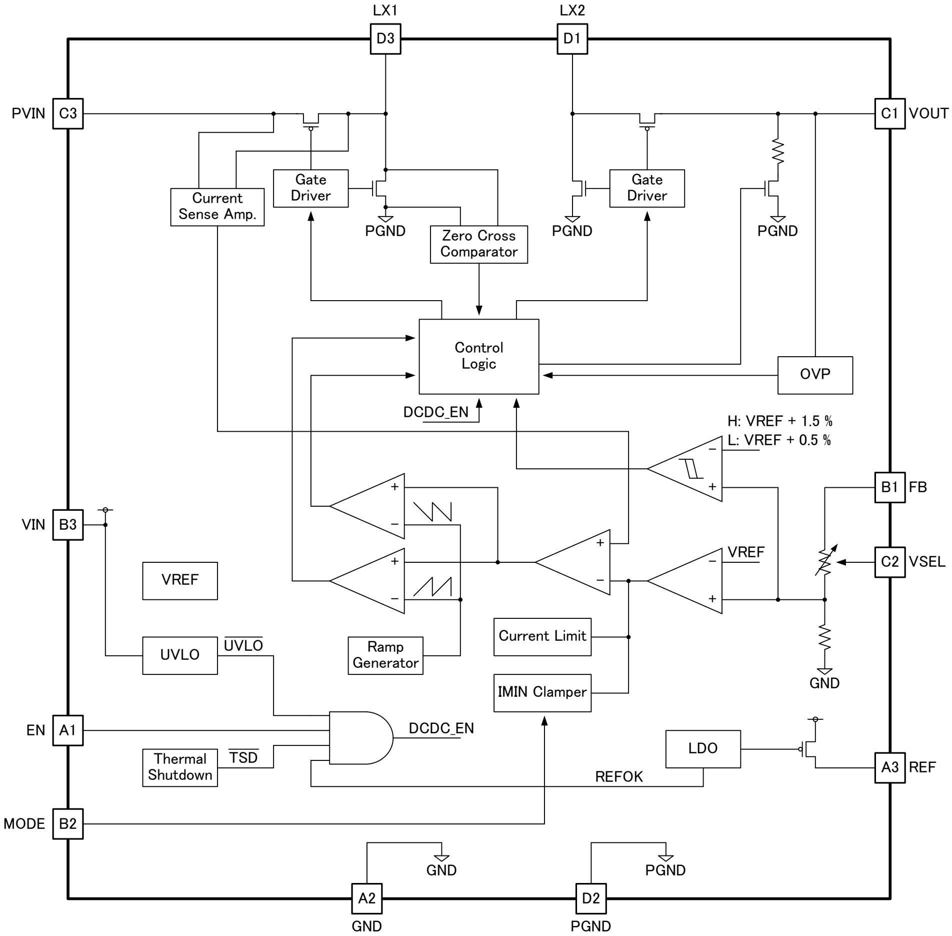


Figure 3. Block Diagram

Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Ratings	Unit
Voltage Range in Pins: VIN, PVIN, VOUT, FB, EN, MODE	V_{MAXVIN}, $V_{MAXPVIN}$, $V_{MAXVOUT}$, V_{MAXFB}, V_{MAXEN}, $V_{MAXMODE}$	-0.3 to +6.0	V
Voltage Range in Pins: LX1, LX2 *(Note 1)*	V_{MAXLX1}, V_{MAXLX2}	-1.0 to +7.0	V
Voltage Range in Pin: REF	V_{MAXREF}	-0.3 to +2.1	V
Voltage Range in Pin: PGND	$V_{MAXPGND}$	-0.3 to +0.3	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +125	°C

(Note 1) Voltage transients on the LX1 or the LX2 pins beyond the DC limits specified in the absolute maximum ratings are non-disruptive to normal operation when using good layout practices as described elsewhere in the data sheet and application notes and as seen on the product demo board.

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance (Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s (Note 3)	2s2p (Note 3)	
UCSP50L1C				
Junction to Ambient	θ_{JA}	-	186.6	°C/W

(Note 2) Based on JESD51-2A(Still-Air).
(Note 3) Using a PCB board based on JESD51-9.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.5 mm x 101.5 mm x 1.6 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.5 mm x 101.5 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	99.5 mm x 99.5 mm	35 µm	99.5 mm x 99.5 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{IN}	2.0	3.6	5.5	V
Operating Temperature	Topr	-40	+25	+85	°C
REF Connection Capacitor (Note 1)	C_{REF}	0.22	0.47	1.00	µF

(Note 1) The minimum value capacitance must be met this specification over full operating condition. Ceramic capacitors are recommended for input/output capacitors.

Electrical Characteristics (Unless otherwise specified VIN=PVIN=EN=VSEL=3.6 V, C_{REF}=0.47 µF, Ta=25 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
DC/DC Converter						
Switching Frequency during PWM	f_{SW}	1.35	1.50	1.65	MHz	MODE=V_{IN}
Maximum Duty	D_{MAX}	80	87	95	%	MODE=V_{IN}
LX1 High Side FET ON Resistance	R_{ON1H}	-	50	-	mΩ	
LX1 Low Side FET ON Resistance	R_{ON1L}	-	60	-	mΩ	
LX2 High Side FET ON Resistance	R_{ON2H}	-	55	-	mΩ	V_{OUT}=3.3 V
LX2 Low Side FET ON Resistance	R_{ON2L}	-	65	-	mΩ	V_{OUT}=3.3 V
Over Current Protection	I_{OCP}	2.0	-	-	A	PVIN=3.6 V
Output Voltage 1	V_{OUT1}	3.267	3.300	3.333	V	MODE=V_{IN}, VSEL=V_{IN}, No Load
Output Voltage 2	V_{OUT2}	2.468	2.500	2.532	V	MODE=V_{IN}, VSEL=0 V, No Load
Load Regulation	V_{LR}	-	0.5	-	mV	MODE=V_{IN}, VSEL=V_{IN} I_{OUT}=0 mA to 1000 mA

Electrical Characteristics - continued (Unless otherwise specified VIN=PVIN=EN=VSEL=3.6 V, C_{REF}=0.47 µF, Ta=25 °C)

Parameter		Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
DC/DC Converter - continued							
Over Voltage Threshold	Detect	V_{OVPDET}	5.3	5.5	5.7	V	V_{OUT} voltage increasing
	Release	V_{OVPRST}	5.2	5.4	5.6	V	V_{OUT} voltage decreasing
Startup Delay Time		t_{ST}	-	4.9	-	ms	From EN=High to V_{OUT}=100 mV
Startup Slew Rate		SR_{ST}	2.5	5.0	10.0	mV/µs	
Discharge Resistance		R_{DCG}	40	85	200	Ω	EN=0 V
Short Circuit Threshold	Detect	V_{SCPDET}	1.3	1.4	1.5	V	FB voltage decreasing
	Release	V_{SCPRST}	1.51	1.61	1.71	V	FB voltage increasing
Main Controller							
Under Voltage Lockout Threshold	Up	V_{UVLOUP}	-	1.740	1.990	V	V_{IN} voltage increasing
	Down	V_{UVLODN}	1.51	1.56	1.61	V	V_{IN} voltage decreasing
EN Pin Control Voltage	ON	V_{ENH}	1.2	-	5.5	V	
	OFF	V_{ENL}	-0.3	-	+0.4	V	
EN Pin Input Current		I_{EN}	-	200	500	nA	
MODE Pin Control Voltage	High	V_{MODEH}	1.2	-	5.5	V	
	Low	V_{MODEL}	-0.3	-	+0.4	V	
VSEL Pin Control Voltage	High	V_{VSELH}	V_{IN}-0.3	-	V_{IN}+0.3	V	
	Low	V_{VSELL}	-0.3	-	+0.3	V	
REF Output Voltage		V_{REF}	1.45	1.50	1.55	V	I_{REF}=-100 µA
Whole Device							
Quiescent VIN Current		I_{VIN}	-	2.8	5.6	µA	MODE=0 V, FB=3.5 V
Quiescent FB Current		I_{FB}	-	0.2	0.4	µA	MODE=0 V, FB=3.5 V
Shutdown VIN Current		I_{SHD}	-	0.1	1.0	µA	EN=0 V

Detailed Descriptions

1. Startup and Shutdown Control
   When the EN pin goes from low (input under 0.4 V or open) to high (input over 1.2 V), the BD83070GWL turns on internal LDO, REF, and the DC/DC converter. There is typically 4.9 ms delay from the EN high edge to startup of DC/DC converter (t_{ST}). It has a soft-start structure and ramps up the output voltage in 5 mV/µs typically (SR_{ST}). On the other hand, when the EN pin goes from high to low, it disables the internal LDO and DC/DC immediately. While in shutdown, it turns discharge switch on to pull V_{OUT} to ground through 85 Ω typically. If the EN pin goes again from low to high during discharge sequence, the output voltage is ramped up from remaining voltage to target voltage in 5 mV/µs(Typ).

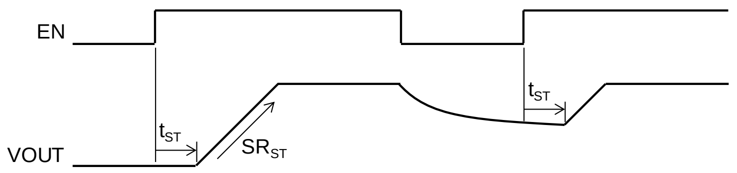


Figure 4. Startup Sequence

2. MODE Pin
   In the case of the MODE pin is pulled high (over 1.2 V), the BD83070GWL operates in forced PWM mode and uses fixed frequency 1.5 MHz regardless its loads. If the MODE pin is pulled low (under 0.4 V), it operates in automatic PFM-PWM mode and automatically changes over form PWM to hysteresis PFM operation depending on its loads. Do not leave this pin floating because it is neither pulled down nor up, internally.

3. Output Voltage Setting
   The BD83070GWL has internal feedback resistors. It is possible to select target output voltage from either 2.5 V or 3.3 V by the VSEL pin. If the VSEL pin is connected to ground, the nominal output voltage is 2.5 V. On the other hand when the VSEL is connected to V_{IN}, the nominal output voltage is 3.3 V. It is not recommended to change while in EN is logic high.

4. Maximum Load Current
   The maximum load current varies depending on PVIN voltage and output voltage setting. When using the recommended application, the maximum load current becomes as follows.

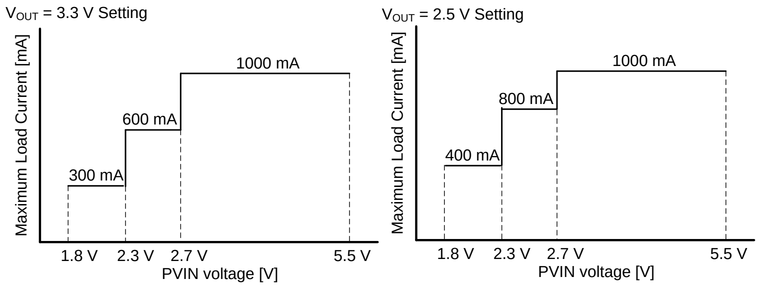


Figure 5. Maximum Load Current

5. Current Limit Protection
   The BD83070GWL has a current limit protection circuit to prevent excessive electric stress on itself and external inductor at overload condition.

6. Short Circuit Protection
   If FB voltage drops less than 1.4 V(Typ), the current limit value is reduced to about half of the normal that. The current limit value returns to the normal that when the FB voltage exceeds 1.61 V(Typ).

7. Over Voltage Protection
   The BD83070GWL has an over voltage comparator. When the FB pin becomes open, the output voltage rises beyond target voltage. If the VOUT pin reaches 5.5 V(Typ), it stops switching to prevent over voltage stress on its power FETs. If the VOUT pin voltage falls lower than 5.4 V(Typ), it restarts switching.

8. Under Voltage Lockout (UVLO)
   The BD83070GWL has a UVLO comparator to turn the device off and prevent malfunction when the input voltage is too low. As same as UVLO, it has a REFOK comparator to monitor REF voltage, internal LDO output, and turns the device off when the REF voltage is too low.

9. Thermal Shutdown
   The BD83070GWL has a Thermal Shutdown Circuit (TSD Circuit). When the temperature of its chip is higher than 175 °C typical, the TSD circuit turns off the DC/DC converter. There is the hysteresis width of 20 °C between the detection point and release point to prevent malfunctions from temperature fluctuations. Because TSD Circuit is only designed for protecting the device from thermal over load, it is not recommended to design the application as TSD working in normal condition.

Typical Performance Curves

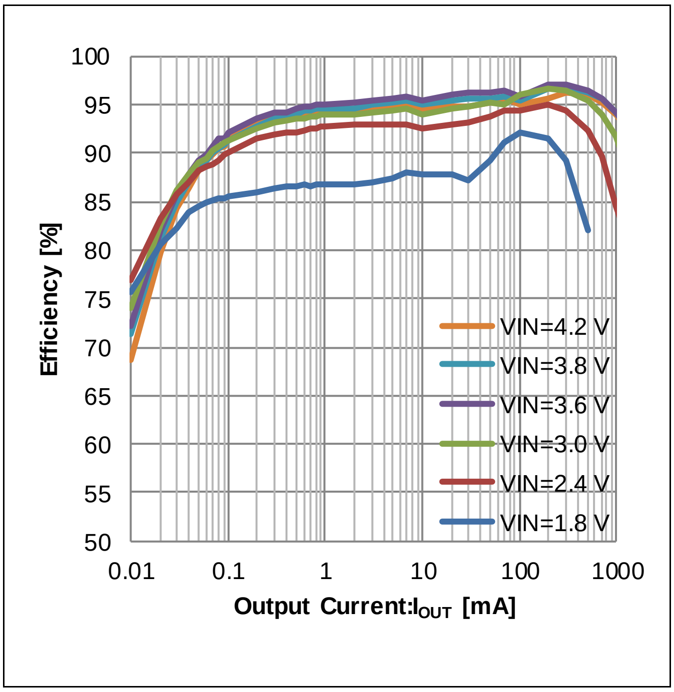


Figure 6. Efficiency vs Output Current
(VSEL=High, MODE=Low: Auto-PFM/PWM)

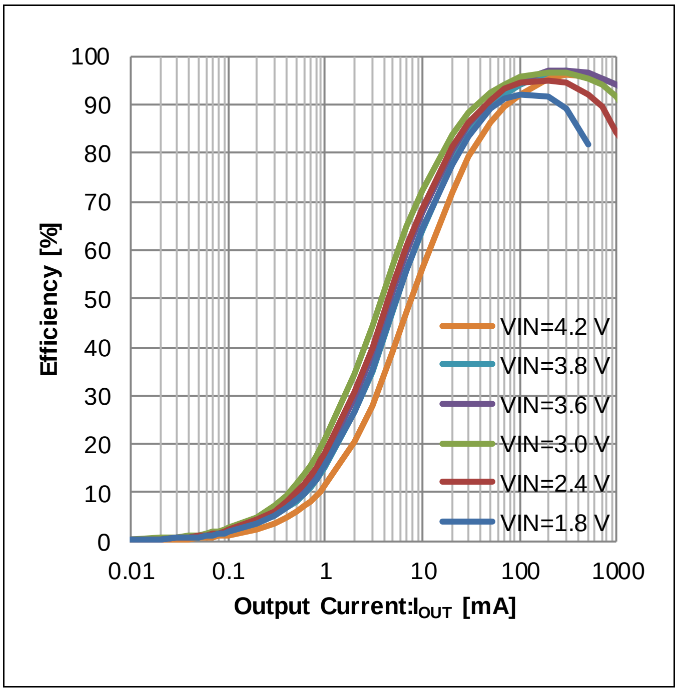


Figure 7. Efficiency vs Output Current
(VSEL=High, MODE=High: Forced-PWM)

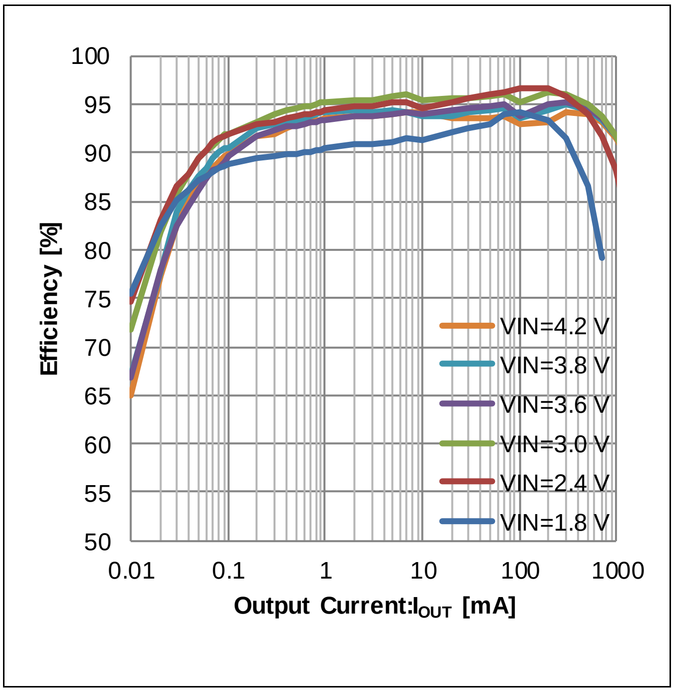


Figure 8. Efficiency vs Output Current
(VSEL=Low, MODE=Low: Auto-PFM/PWM)

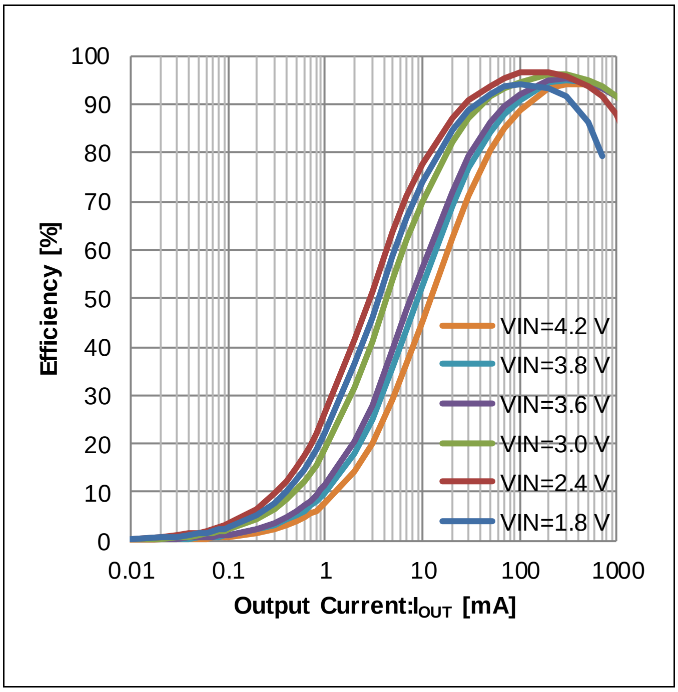


Figure 9. Efficiency vs Output Current
(VSEL=Low, MODE=High: Forced-PWM)

Typical Performance Curves - continued

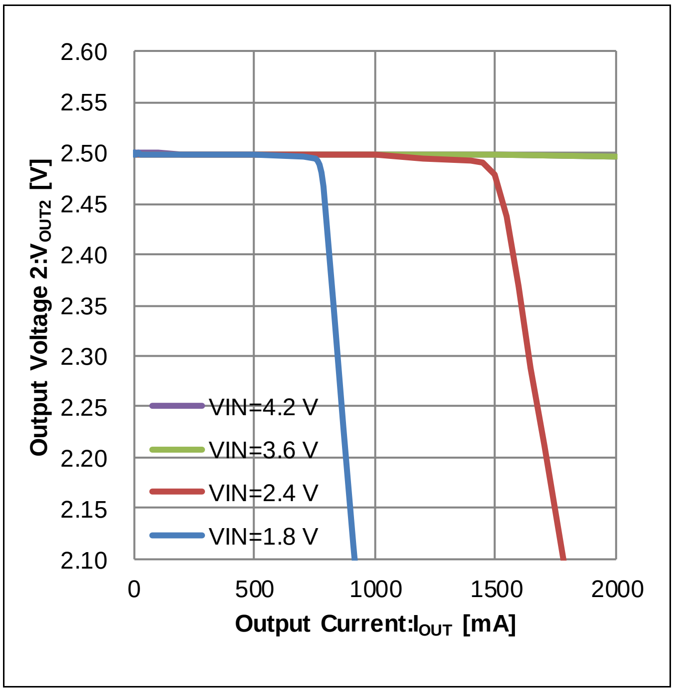


Figure 10. Output Voltage 2 vs Output Current
(“Load Regulation”, VSEL=Low, MODE=High: Forced-PWM)

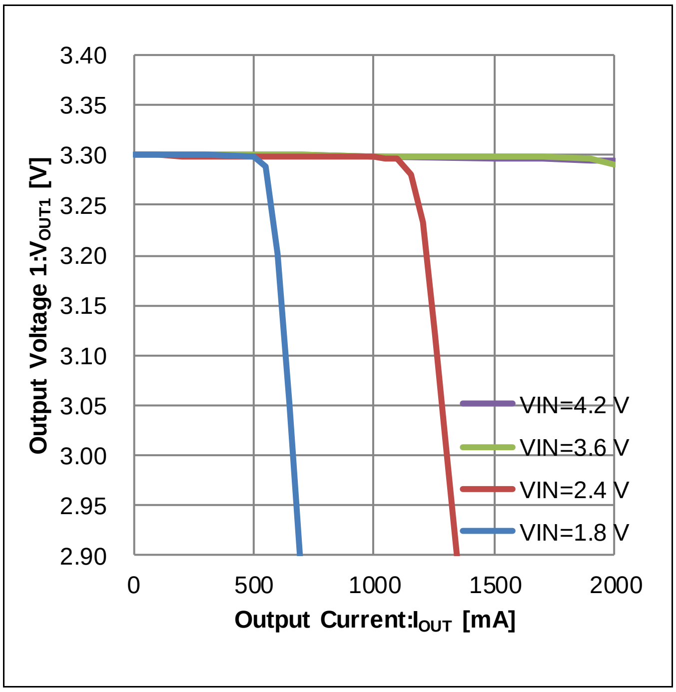


Figure 11. Output Voltage 1 vs Output Current
(“Load Regulation”, VSEL=High, MODE=High: Forced-PWM)

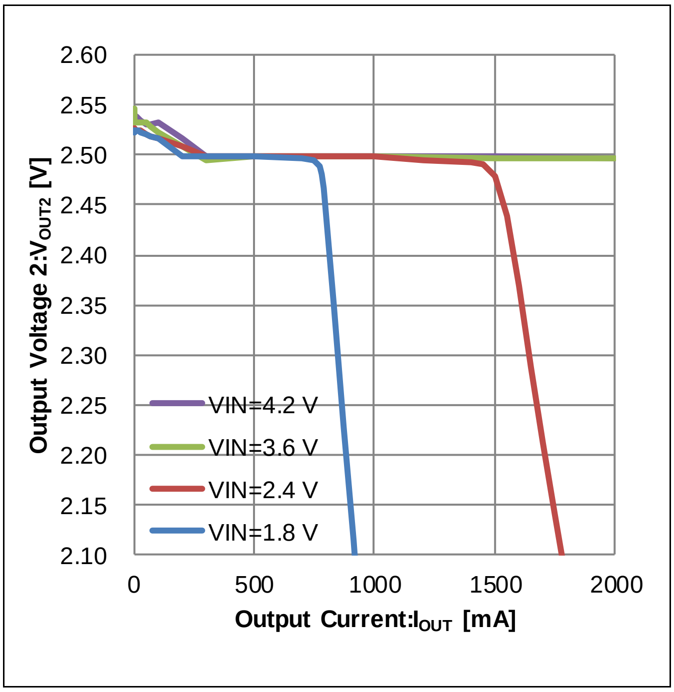


Figure 12. Output Voltage 2 vs Output Current
(“Load Regulation”, VSEL=Low, MODE=Low: Auto-PFM/PWM)

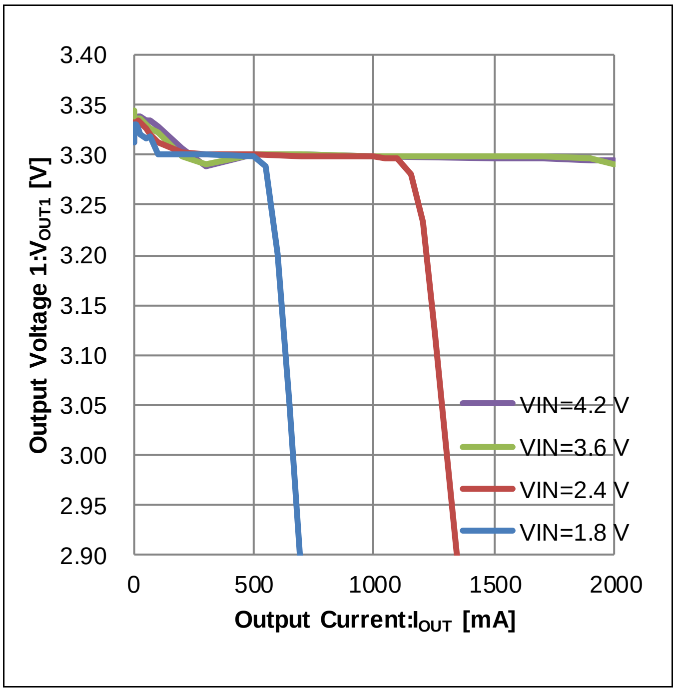


Figure 13. Output Voltage 1 vs Output Current
(“Load Regulation”, VSEL=High, MODE=Low: Auto-PFM/PWM)

Typical Performance Curves - continued

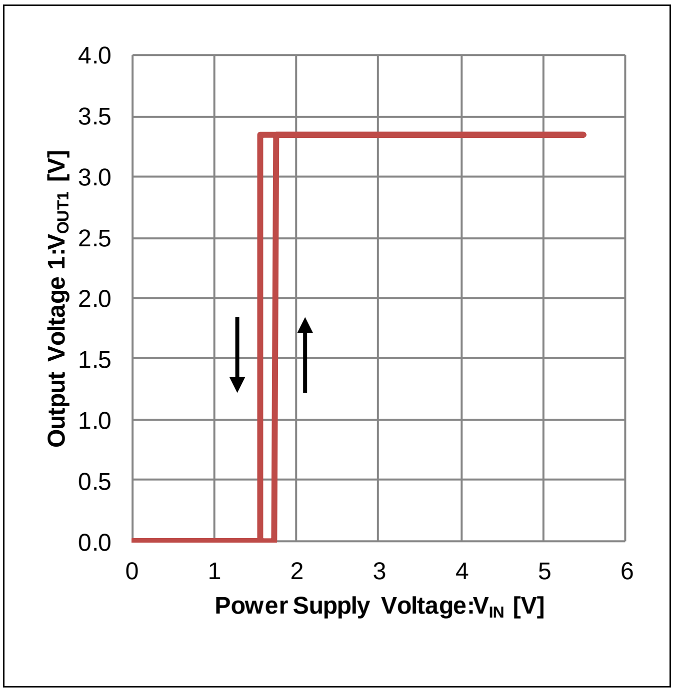


Figure 14. Output Voltage 1 vs Power Supply Voltage
(“Line Regulation”, EN=VSEL=High, MODE=Low:
Auto-PFM/PWM, 3.3 kΩ resistive load)

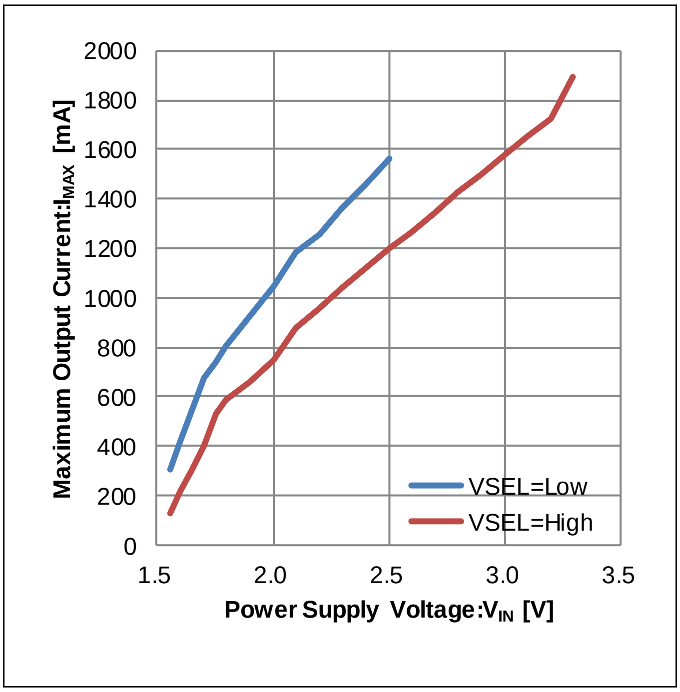


Figure 15. Maximum Output Current vs Power Supply Voltage

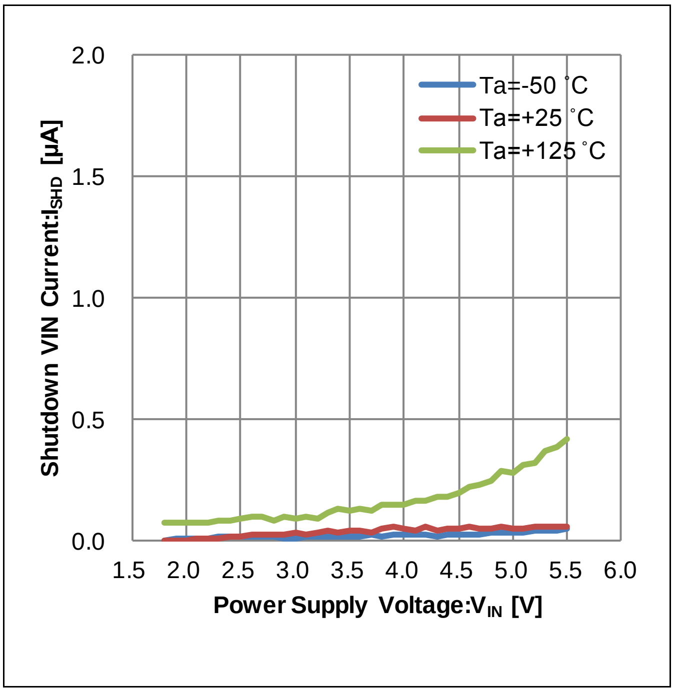


Figure 16. Shutdown VIN Current vs Power Supply Voltage
(EN=MODE=Low, No load)

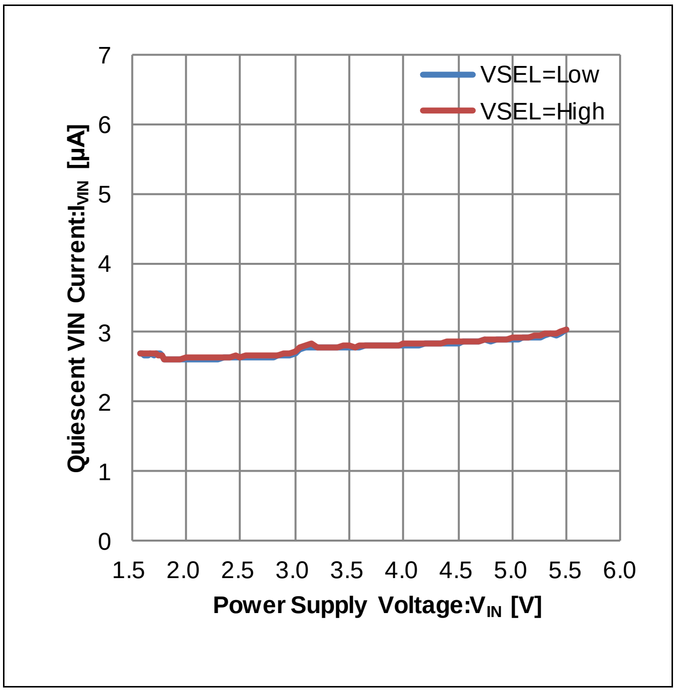


Figure 17. Quiescent VIN Current vs Power Supply Voltage
(MODE=Low: Auto-PFM/PWM, FB=3.5 V, No load)

Typical Performance Curves - continued

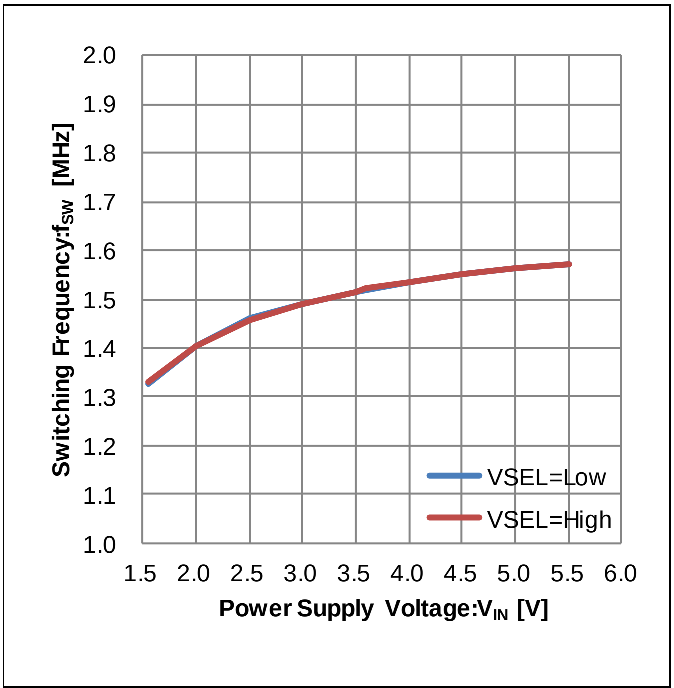


Figure 18. Switching Frequency vs Power Supply Voltage
(MODE=High: Forced-PWM, No load)

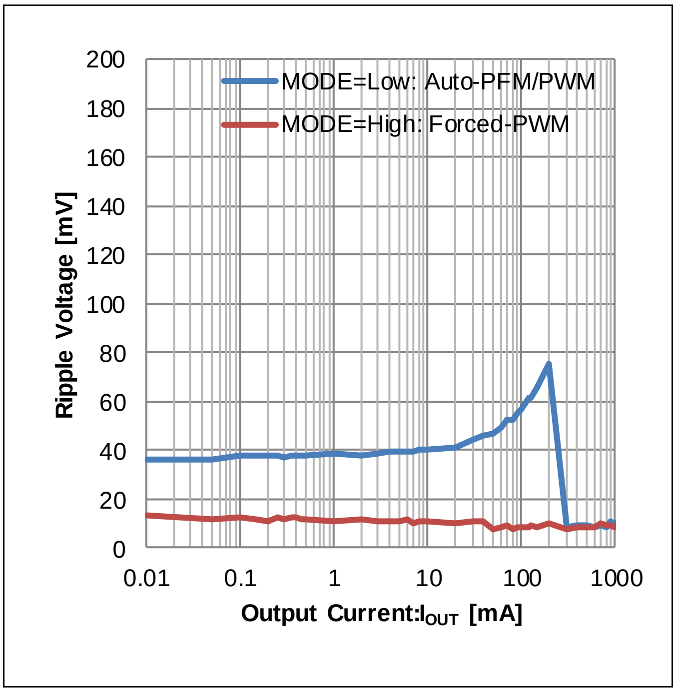


Figure 19. Ripple Voltage vs Output Current
(VIN=3.6 V, VSEL=High)

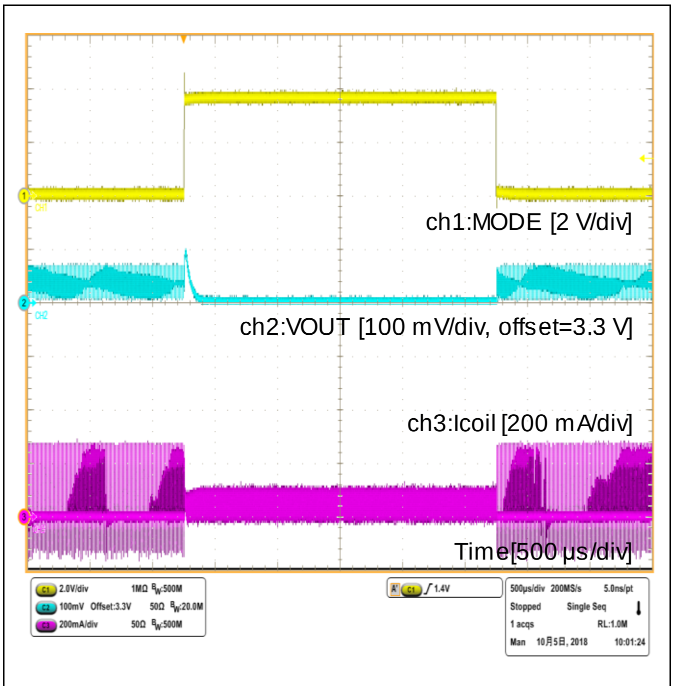


Figure 20. Transient Response
(“Mode Change”, VIN=3.6 V, VSEL=High,
MODE=Low<->High, Output current 50 mA)

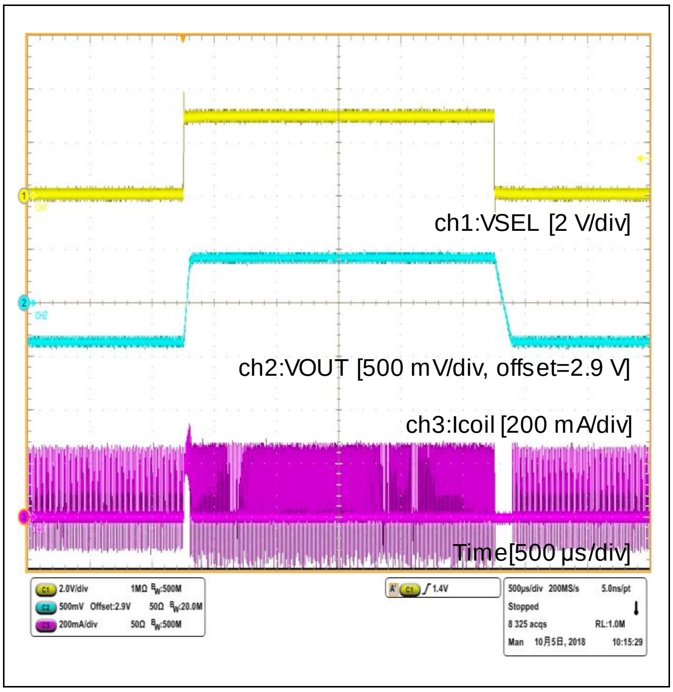


Figure 21. Transient Response
(“Output Voltage Change”, VIN=2.9 V, VSEL=Low<->High,
MODE=Low: Auto-PFM/PWM, Output current 50 mA)

Typical Performance Curves - continued

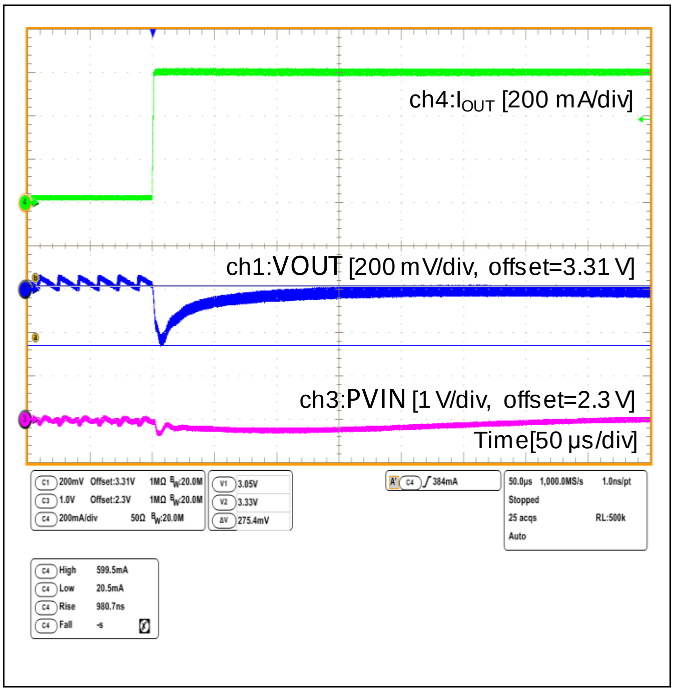


Figure 22. Transient Response
(VIN=2.3 V, VSEL=High, MODE=Low: Auto-PFM/PWM,
Output current 20 mA->600 mA)

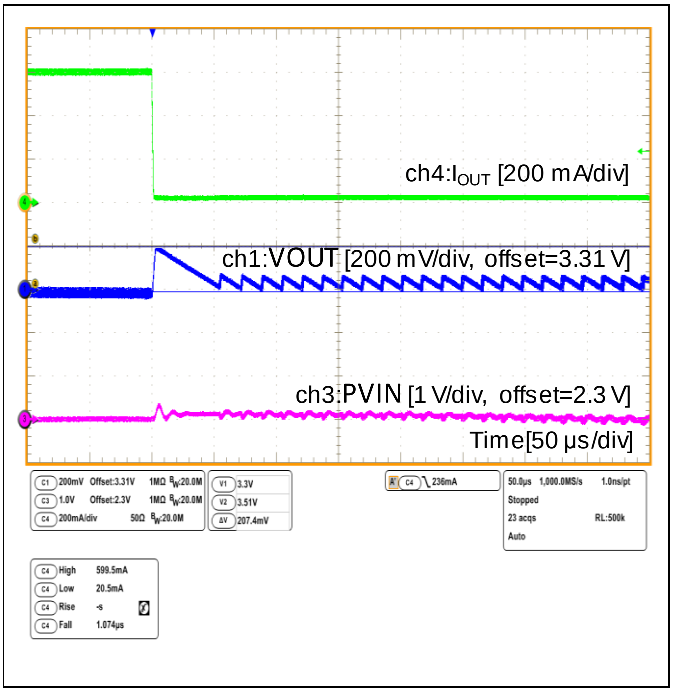


Figure 23. Transient Response
(VIN=2.3 V, VSEL=High, MODE=Low: Auto-PFM/PWM,
Output current 600 mA->20 mA)

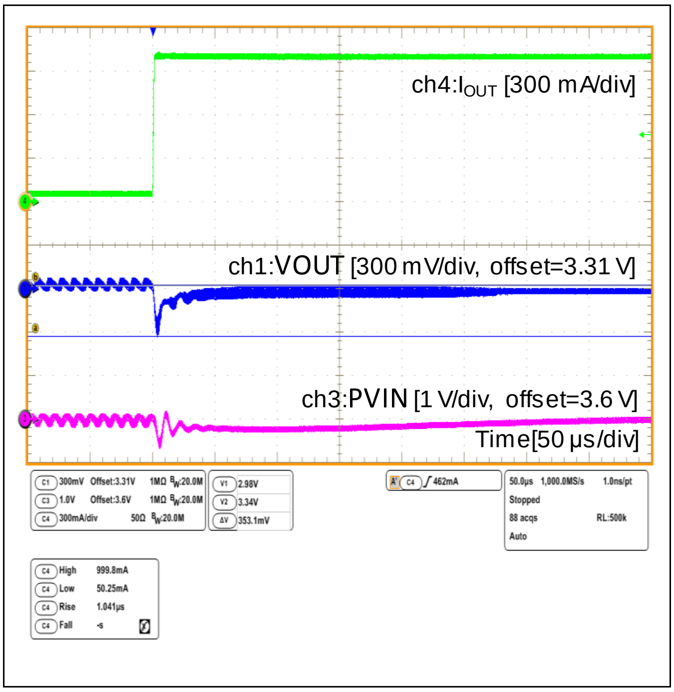


Figure 24. Transient Response
(VIN=3.6 V, VSEL=High, MODE=Low: Auto-PFM/PWM,
Output current 50 mA->1000 mA)

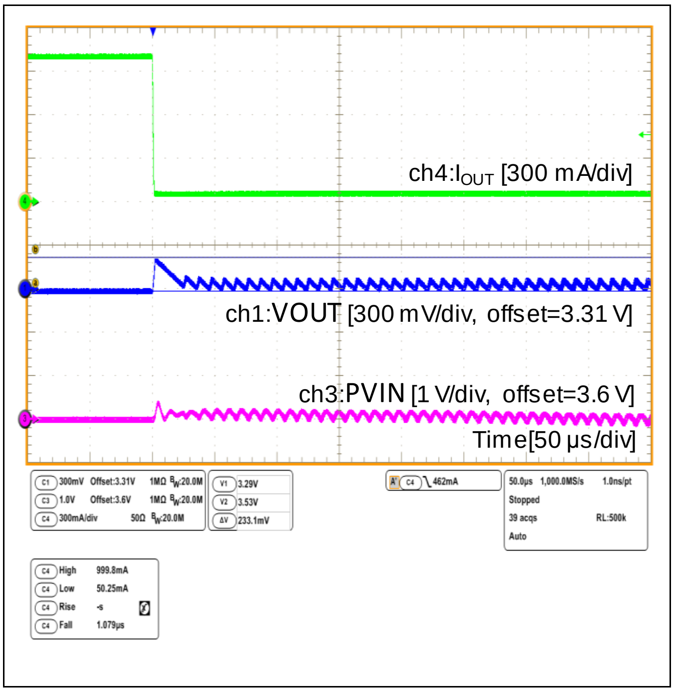


Figure 25. Transient Response
(VIN=3.6 V, VSEL=High, MODE=Low: Auto-PFM/PWM,
Output current 1000 mA->50 mA)

Typical Performance Curves - continued

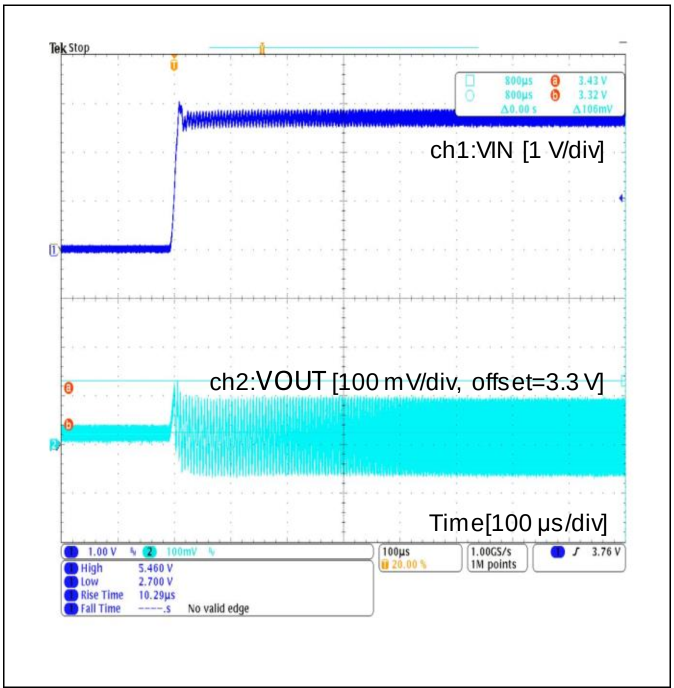


Figure 26. Transient Response
(VIN=2.7 V->5.5 V, VSEL=High, MODE=Low: Auto-PFM/PWM, Output current 300 mA)

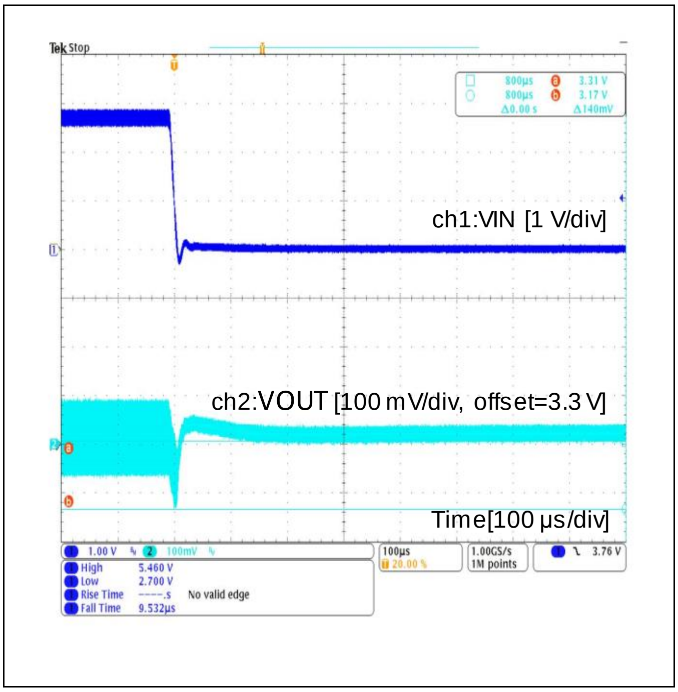


Figure 27. Transient Response
(VIN=5.5 V->2.7 V, VSEL=High, MODE=Low: Auto-PFM/PWM, Output current 300 mA)

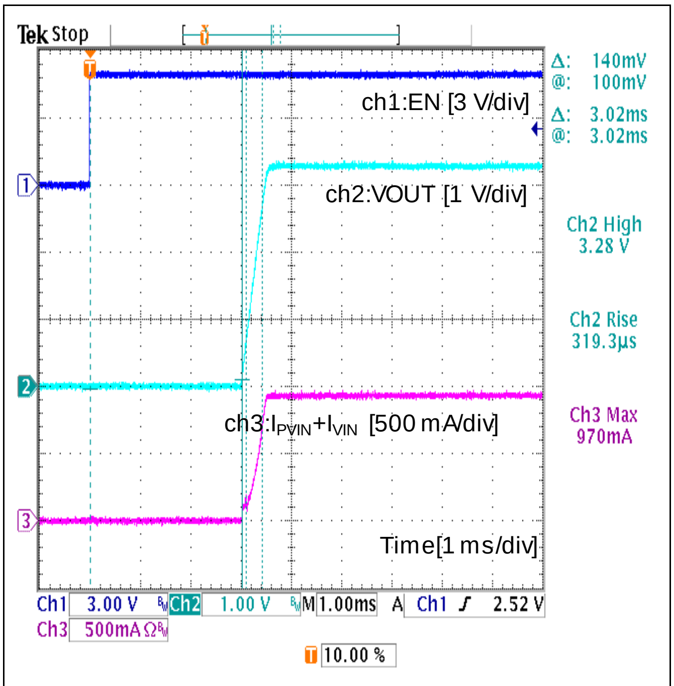


Figure 28. Startup Waveform
(VIN=2.4 V, VSEL=High, MODE=High: Forced-PWM, 5.5 Ω resistive load)

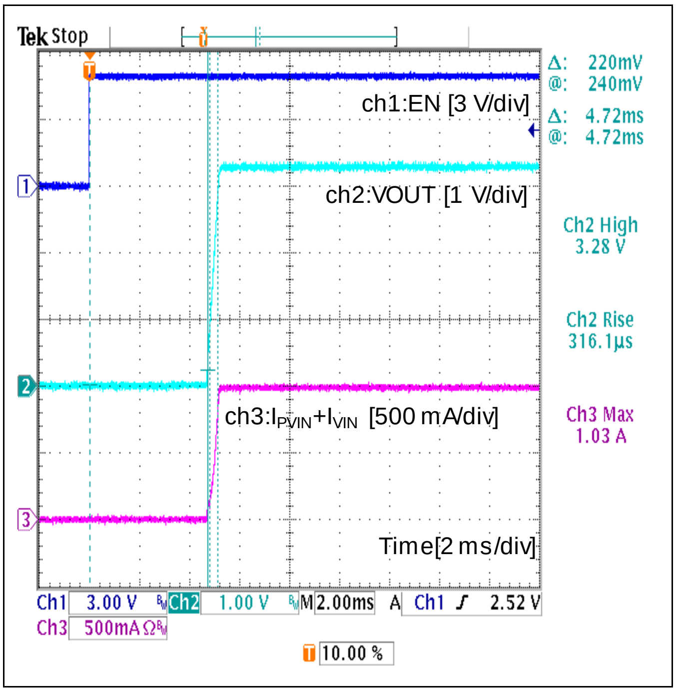


Figure 29. Startup Waveform
(VIN=3.6 V, VSEL=High, MODE=High: Forced-PWM, 3.3 Ω resistive load)

Typical Performance Curves - continued

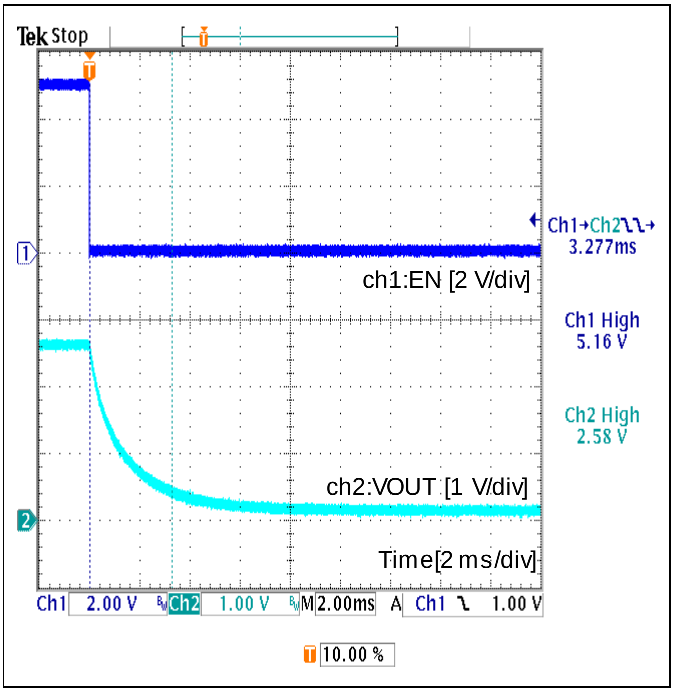


Figure 30. Shutdown Waveform
(VIN=3.6 V, VSEL=Low, MODE=Low: Auto-PFM/PWM, No load)

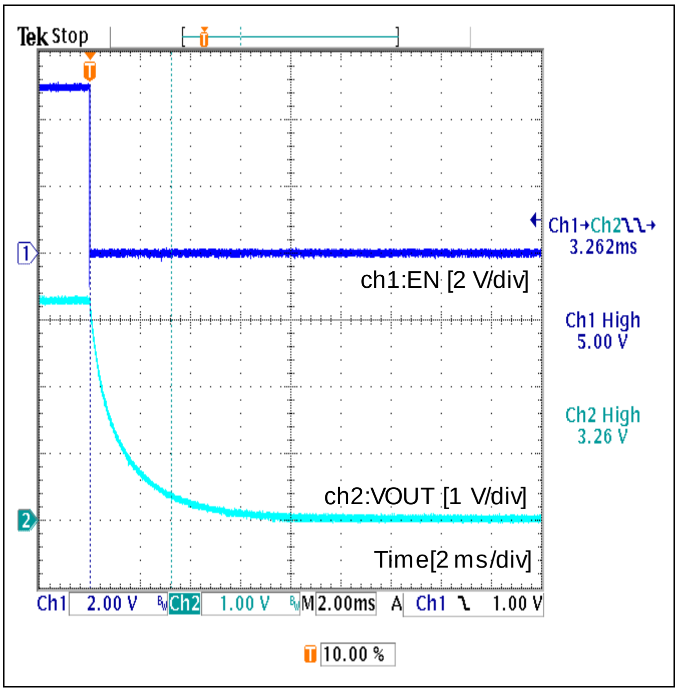


Figure 31. Shutdown Waveform
(VIN=3.6 V, VSEL=High, MODE=Low: Auto-PFM/PWM, No load)

Application Examples

VSEL = V_{IN} (V_{OUT} = 3.3 V setting)

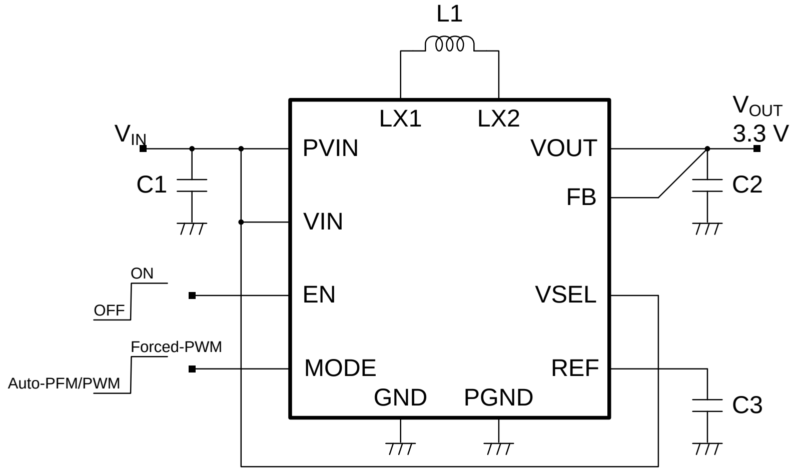


Figure 32. 3.3V Output Application Circuit

VSEL = GND (V_{OUT} = 2.5 V setting)

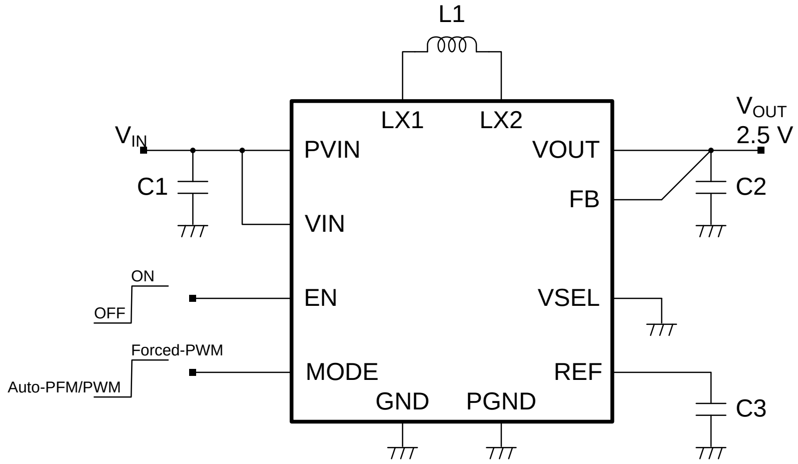
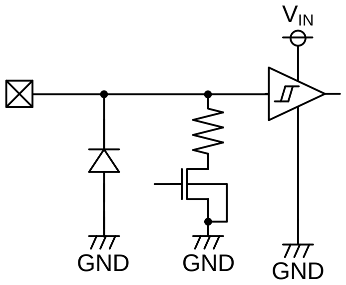
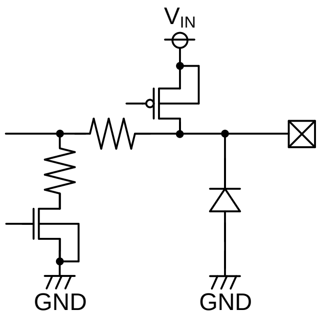
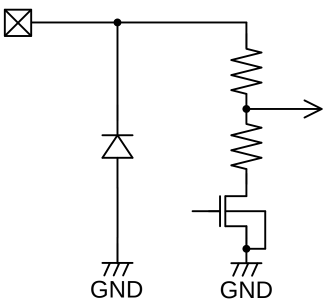
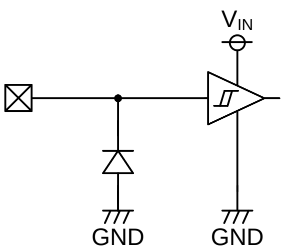
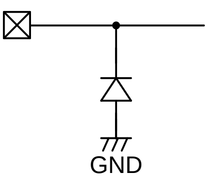


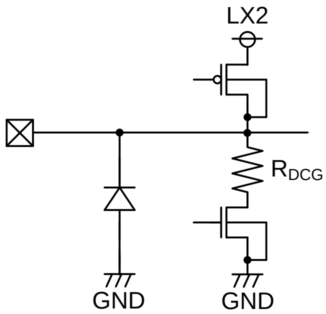
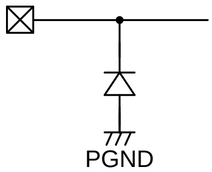
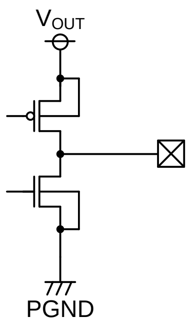
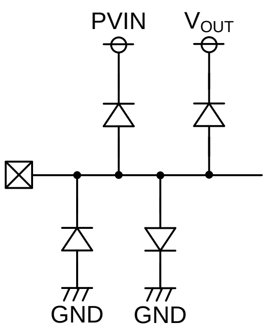
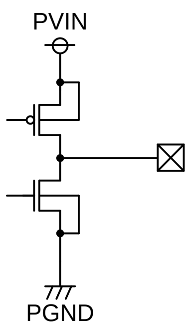
Figure 33. 2.5 V Output Application Circuit

Parts Number	Description	Supplier
L1	1239AS-H-1R5M (1.5 µH, 2.5 mm x 2.0 mm x 1.2 mm)	muRata
C1	EMK212ABJ106KD (10 µF, 16 V, X5R, 0805)	Taiyo Yuden
C2*(Note 1)*	JMK107BBJ226MA (22 µF, 6.3 V, X5R, 0603)	Taiyo Yuden
C3	EMK105ABJ474KV-F (0.47 µF, 16 V, X5R, 0402)	Taiyo Yuden

(Note 1) The effective load capacitance value considering accuracy, temperature characteristic and DC bias characteristic of output capacitors should not be less than 22 µF. The amount of output capacitance will have a significant effect on the output ripple voltage.

I/O Equivalence Circuits

Pin Name	Equivalence circuit
EN	
REF	
FB	
MODE VSEL	
VIN	

Pin Name	Equivalence circuit
VOUT	
PVIN	
LX2	
PGND	
LX1	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

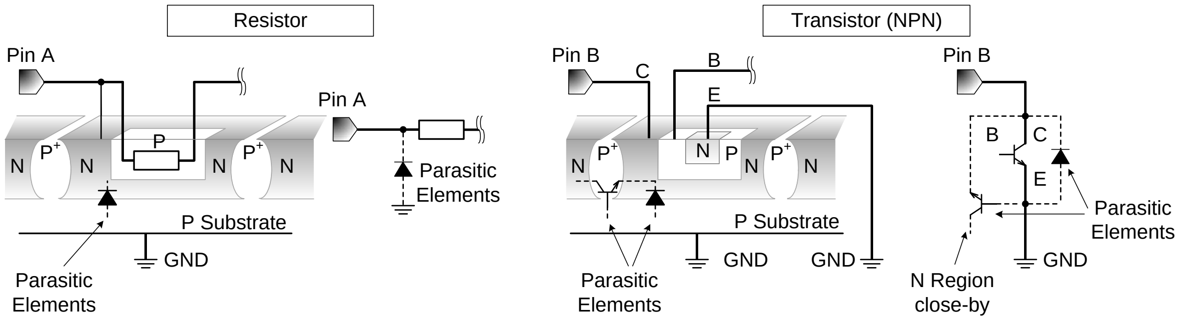


Figure 34. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC’s maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Disturbance Light

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

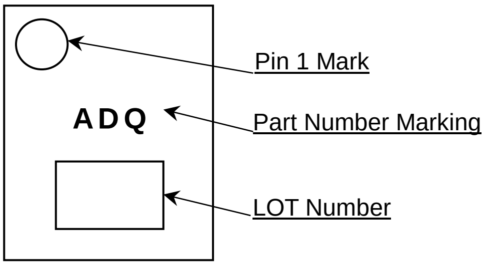
Ordering Information

B	D	8	3	0	7	0	G	W	L		E 2

- Part Number
- Package
  GWL: UCSP50L1C
- Packaging and forming specification
  E2: Embossed tape and reel

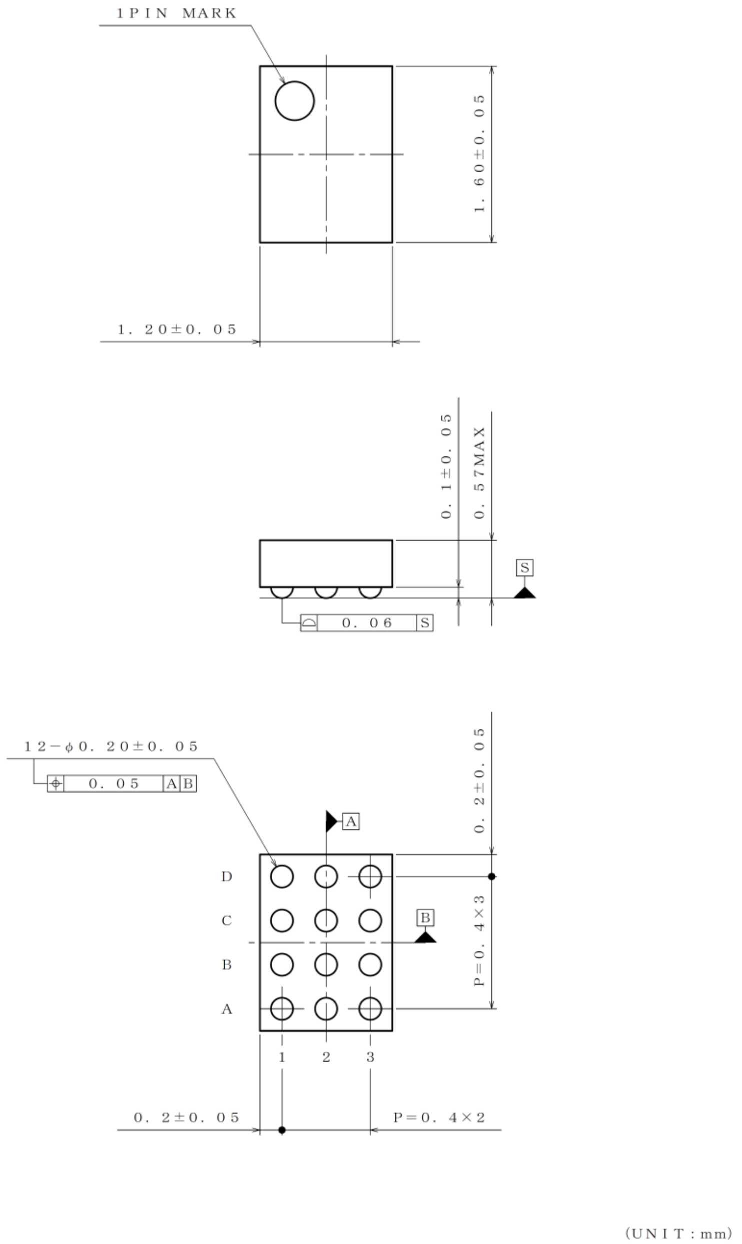
Marking Diagram

TOP VIEW
UCSP50L1C (BD83070GWL)



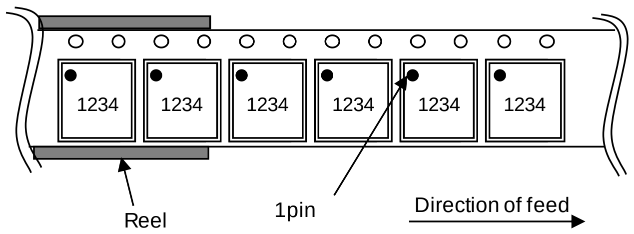
Physical Dimension and Packing Information

Package Name	UCSP50L1C(BD83070GWL)



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3,000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
09.Oct.2018	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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