XL3232 3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver With ±15-kV ESD Protection

1 Features

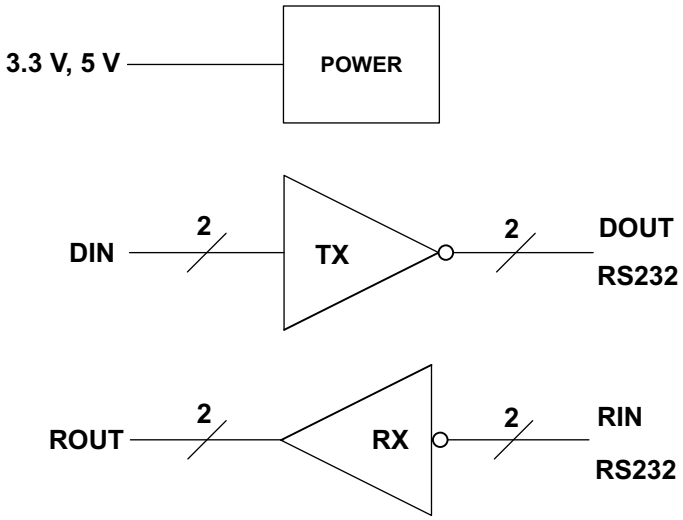
- RS-232 Bus-terminal esd protection exceeds ±15 kV using human-body model (HBM)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU V.28 standards
- Operates with 3-V to 5.5-V V_{CC} supply
- Operates up to 250 kbit/s
- Two drivers and two receivers
- Low supply current: 300 µA Typical
- External capacitors: 4 × 0.1 µF
- Accepts 5-V logic input with 3.3-V supply
- Alternative high-speed terminal-compatible devices (1 Mbit/s)

3 Description

The XL3232 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

2 Applications

- Wired networking
- Data center and enterprise networking
- Battery-powered systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-held equipment spacer



Simplified Schematic

4 Pin Configuration and Functions

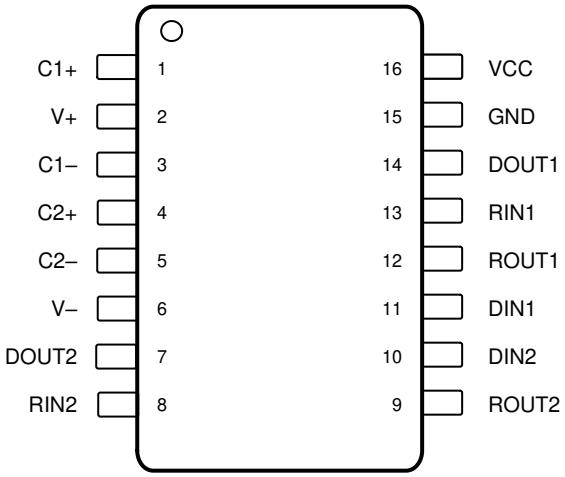


Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
V+	2	O	Positive charge pump output for storage capacitor only
C1–	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2–	5	—	Negative lead of C2 capacitor
V–	6	O	Negative charge pump output for storage capacitor only
DOUT2	7	O	RS232 line data output (to remote RS232 system)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
RIN1	13	I	RS232 line data input (from remote RS232 system)
ROUT2	9	O	Logic data output (to UART)
ROUT1	12	O	Logic data output (to UART)
DIN2	10	I	Logic data input (from UART)
DIN1	11	I	Logic data input (from UART)
GND	15	—	Ground
V_{CC}	16	—	Supply Voltage, Connect to external 3 V to 5.5 V power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive output supply voltage range(2)		–0.3	7	V
V–	Negative output supply voltage range(2)		–7	0.3	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Drivers	–0.3	6	V
		Receivers	–25	25	
V_O	Output voltage range	Drivers	–13.2	13.2	V
		Receivers	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 RIN , DOUT, and GND pins (1)	15000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 All other pins(1)	3000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

(see Typical Operating Circuit and Capacitor Values)(1)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver low-level input voltage	DIN				0.8	V
V_I	Driver input voltage	DIN		0		5.5	V
	Receiver input voltage	RIN		–25		25	
T_A	Operating free-air temperature		3232	–40		85	°C

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

5.4 Electrical Characteristics — Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2) (see Typical Operating Circuit and Capacitor Values)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	No load,	V_{CC} = 3.3 V to 5 V		0.3	1	mA

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

5.5 Electrical Characteristics — Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3) (see Typical Operating Circuit and Capacitor Values)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	D_{OUT} at R_L = 3 kΩ to GND,	D_{IN} = GND	5	5.4		V
V_{OL}	Low-level output voltage	D_{OUT} at R_L = 3 kΩ to GND,	D_{IN} = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	µA
I_{OS} (2)	Short-circuit output current	V_{CC} = 3.6 V	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V	V_O = 0 V				
r_O	Output resistance	V_{CC}, V+, and V– = 0 V	V_O = ±2 V	300	10M		Ω

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
(3) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5

5.6 Electrical Characteristics — Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2) (see Typical Operating Circuit and Capacitor Values)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT–}$)			0.3		V
r_I	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

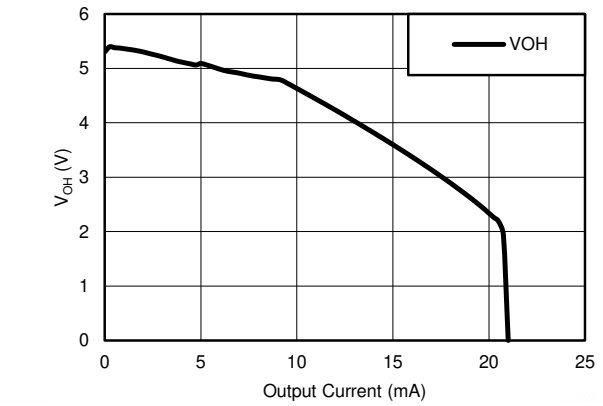
5.7 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3) (see Typical Operating Circuit and Capacitor Values)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
	Maximum data rate	R_L = 3 kΩ, One D_{OUT} switching,	C_L = 1000 pF See Figure 7-1	150	250		kbit/s
$t_{sk(p)}$	Driver Pulse skew(2)	R_L = 3 kΩ to 7 kΩ,	C_L = 150 to 2500 pF See Figure 7-2		300		ns
SR(tr)	Slew rate, transition region (see Figure 7-1)	R_L = 3 kΩ to 7 kΩ, V_{CC} = 5 V	C_L = 150 to 1000 pF	6		30	V/µs
			C_L = 150 to 2500 pF	4		30	
$t_{PLH®)}$	Propagation delay time, low- to high-level output	C_L = 150 pF			300		ns
$t_{PHL®)}$	Propagation delay time, high- to low-level output				300		
$t_{sk(p)}$	Receiver Pulse skew(3)				300		

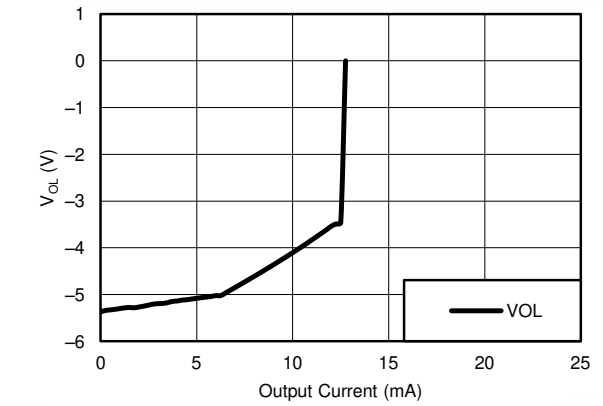
(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

5.8 Typical Characteristics



V_{CC} = 3.3 V

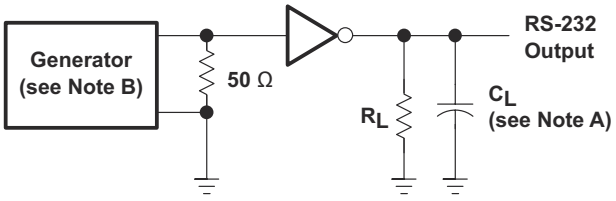
Figure 6-1. DOUT V_{OH} vs Load Current, Both Drivers Loaded



V_{CC} = 3.3 V

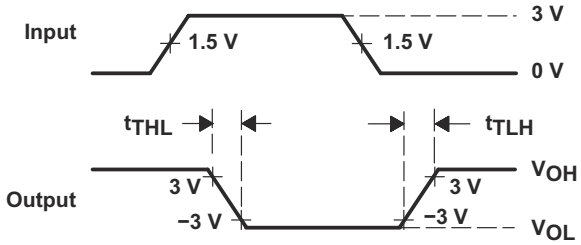
Figure 6-2. DOUT V_{OL} vs Load Current, Both Drivers Loaded

6 Parameter Measurement Information



TEST CIRCUIT

$$SR(tr) = \frac{6\ V}{t_{THL} \text{ or } t_{TLH}}$$

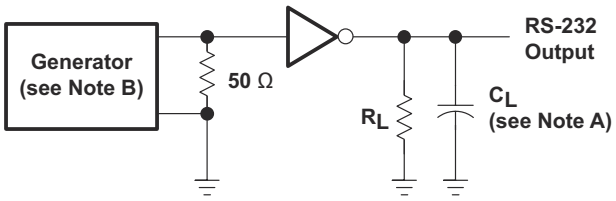


VOLTAGE WAVEFORMS

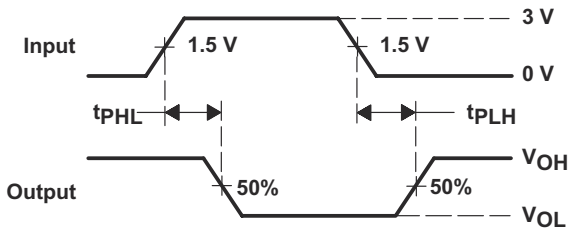
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 6-1. Driver Slew Rate



TEST CIRCUIT

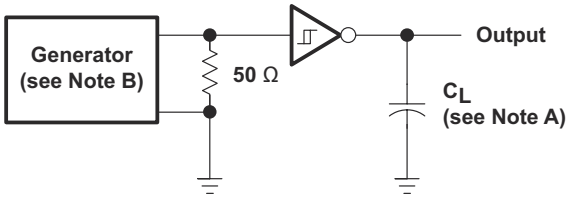


VOLTAGE WAVEFORMS

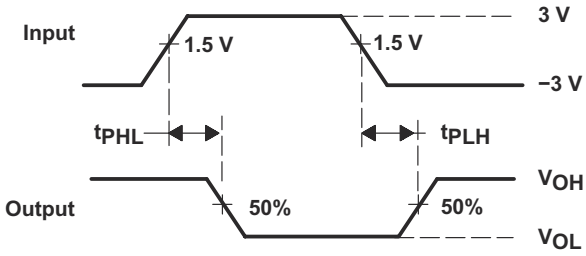
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 6-2. Driver Pulse Skew



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

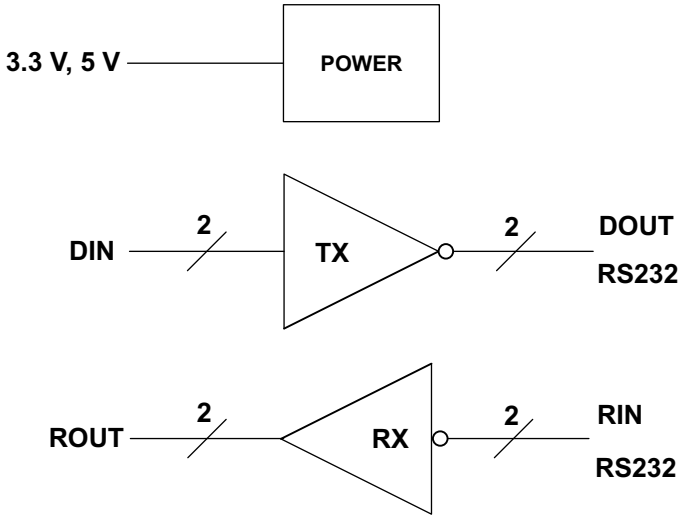
Figure 6-3. Receiver Propagation Delay Times

7 Detailed Description

7.1 Overview

The XL3232 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/μs driver output slew rate. Outputs are protected against shorts to ground.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V- pins using a charge pump that requires four external capacitors.

7.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

7.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

7.4 Device Functional Modes

Table 7-1. Each Driver(1)

INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

Table 7-2. Each Receiver(1)

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off

7.4.1 V_{CC} powered by 3 V to 5.5 V

The device will be in normal operation.

7.4.2 V_{CC} unpowered, V_{CC} = 0 V

When XL3232 is unpowered, it can be safely connected to an active remote RS232 device.

8 Application and Implementation

Note

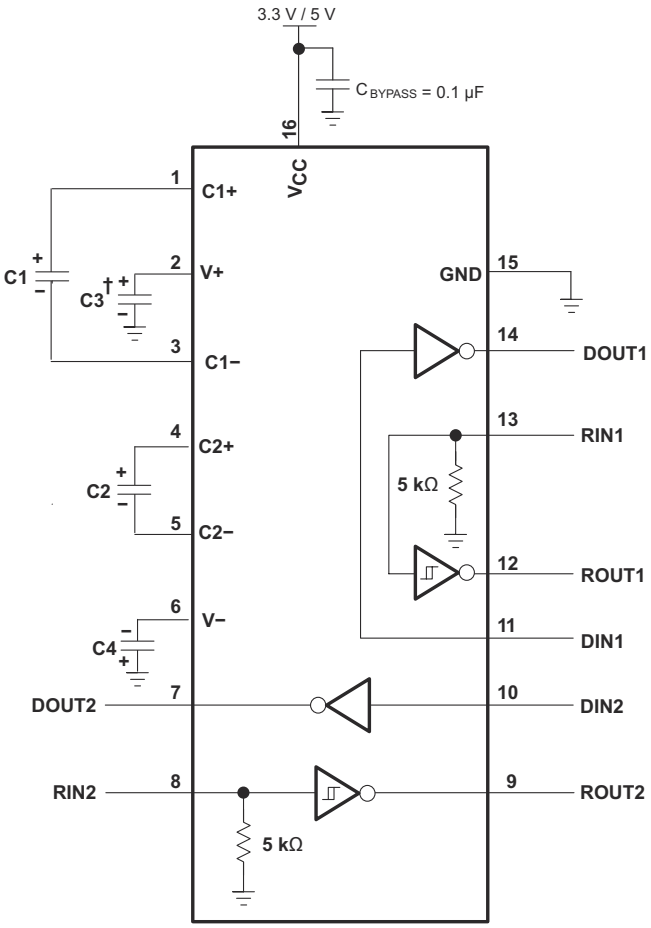
Information in the following applications sections is not part of the XINLUDA component specification, and XINLUDA does not warrant its accuracy or completeness. XINLUDA customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

For proper operation, add capacitors as shown in Typical Operating Circuit and Capacitor Values.

8.2 Standard Application

ROUT and DIN connect to UART or general purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.



† C3 can be connected to V_{CC} or GND.

A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 8-1. Typical Operating Circuit and Capacitor Values

8.2.1 Design Requirements

- Recommended V_{CC} is 3.3 V or 5 V. 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 250 kbit/s.

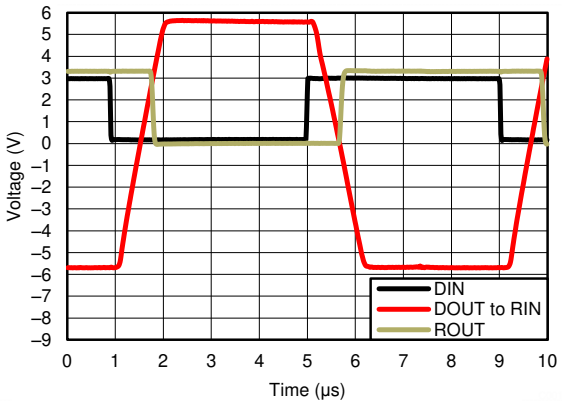
Table 8-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

8.2.2 Detailed Design Procedure

- All DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels.
- Select capacitor values based on VCC level for best performance.

8.2.3 Application Curves



V_{CC} = 3.3 V

Figure 9-2. 250 kbit/s Driver to Receiver Loopback Timing Waveform

9 Power Supply Recommendations

V_{CC} should be between 3 V and 5.5 V. Charge pump capacitors should be chosen using table in Typical Operating Circuit and Capacitor Values.

10 Layout

10.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

10.2 Layout Example

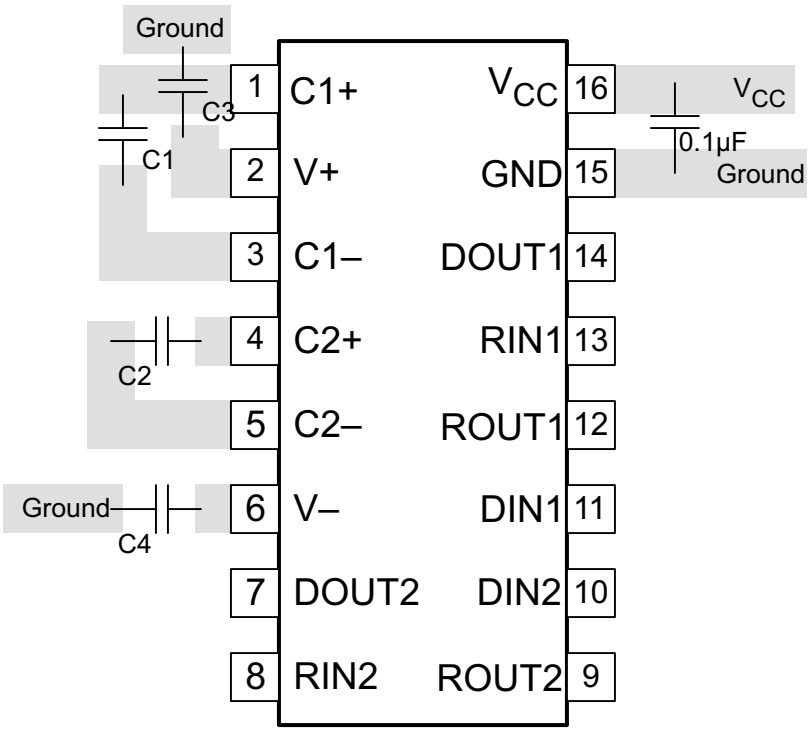
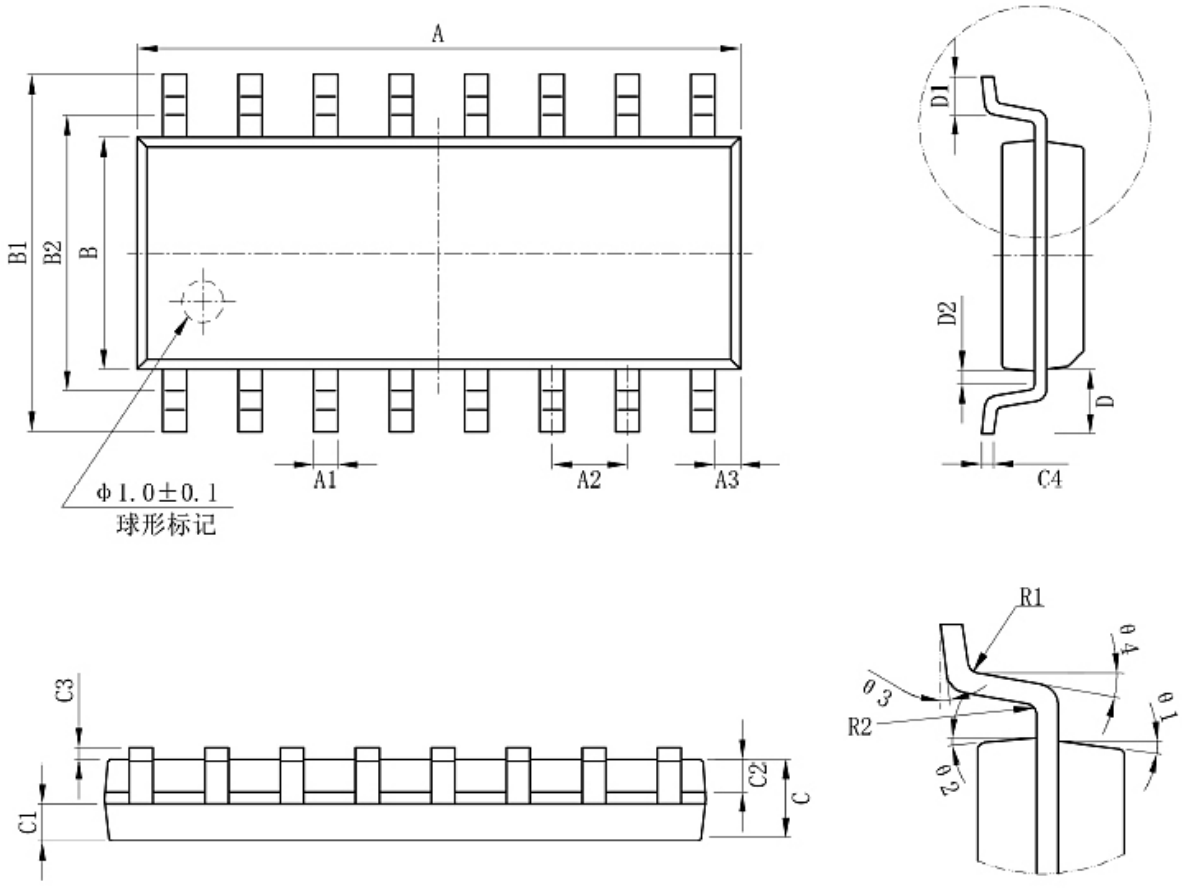


Figure 10-1. Layout Diagram

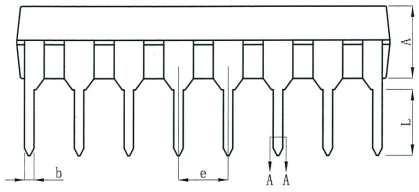
Ordering Information							
part Number	Device Marking	Package type	Body size (mm)	Temperature (℃)	MSL	Transport Media	Package Quantity
XL3232	XL3232	SOP16	9.9*3.9	-40 to +85	MSL3	T&R	2500
XL3232-TS	XL3232-TS	TSSOP16	5.0*3.9	-40 to +85	MSL3	T&R	2500
XD3232	XD3232	DIP16	19.05*6.35	-40 to +85	MSL3	Tube 25	1000

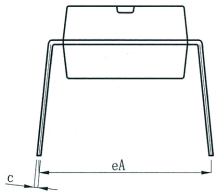
SOP16封装尺寸图

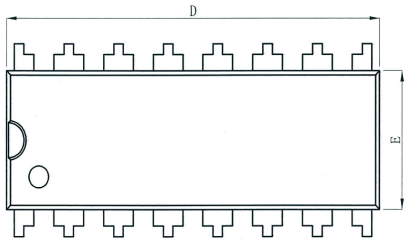
标注 \ 尺寸	最小(mm)	最大(mm)	标注 \ 尺寸	最小(mm)	最大(mm)
A	9.80	10.00	C4	0.203	0.233
A1	0.356	0.456	D	1.05TYP	
A2	1.27TYP		D1	0.40	0.70
A3	0.302TYP		D2	0.15	0.25
B	3.85	3.95	R1	0.20TYP	
B1	5.84	6.24	R2	0.20TYP	
B2	5.00TYP		θ1	8° ~ 12° TYP4	
C	1.40	1.60	θ2	8° ~ 12° TYP4	
C1	0.61	0.71	θ3	0° ~ 8°	
C2	0.54	0.64	θ4	4° ~ 12°	
C3	0.05	0.25			

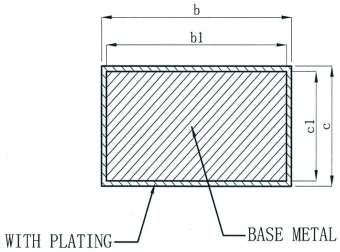


DIP16封装尺寸图



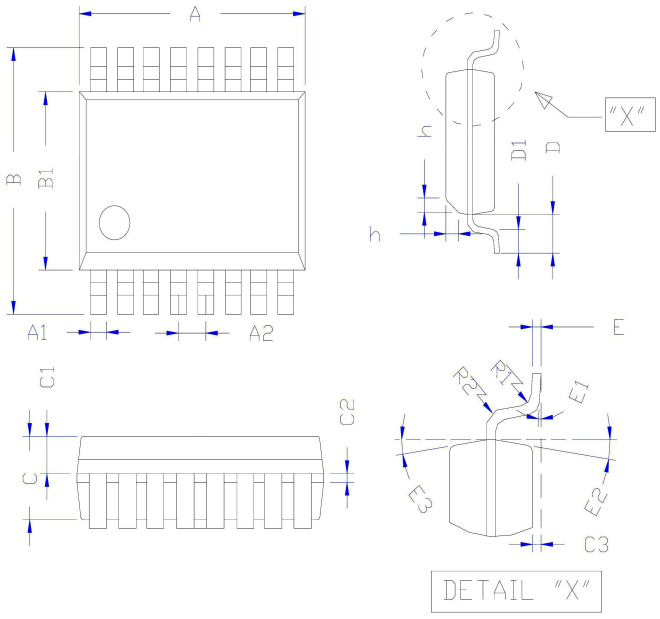






symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---

TSSOP16封装尺寸图



标注	表示	MIN	NOM	MAN
A	总长	4.95	5.00	5.05
A1	脚宽	0.20	0.22	0.24
A2	脚间距	0.60	0.65	0.70
B	跨度	5.70	6.00	6.30
B1	胶体宽度	3.80	3.90	4.00
C	胶体厚度	0.95	1.00	1.05
C1	上胶体厚	0.40	0.41	0.42
C2		0.05	0.15	0.25
C3	站高	0.02	0.08	0.10
D	单边长	0.85	1.05	1.25
D1	脚长	0.40	0.65	0.85
E	脚厚	0.15	0.20	0.25
E1	脚角度	0℃		8℃
h		0.30	0.40	0.50