MORNSUN®

TDA51S485HC
SOIC16 package isolated RS485 Transceiver

Features

- Ultra-small, ultra-thin, chip scale SOIC 16 package
- Compliant with TIA/EIA-485-A standard
- Wide input supply range: 3.15 V to 5.5 V
- Integrated high-efficiency DC-DC converter with on-chip transformer; With overload and short-circuit protection
- I/O power supply range supports 3.3V and 5V microprocessors
- High isolation to 5000Vrms
- Bus-Pin ESD protection up to 6kV(HBM)/15kV(contact)
- Baud rate up to 500kbps
- High CMTI:150kV/μs(typical)
- Nanosecond communication delay
- 1/8 unit load—up to 256 nodes on a bus
- Bus fail-safe
- Bus driver short circuit protection
- Industrial operating ambient temperature range: -40℃ to +105℃

Package

Applications

- Industrial Automation
- Building Automation
- Smart Electricity Meter
- Remote Signal Interaction, Transmission

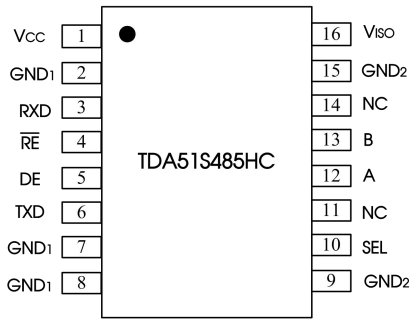
Functional Description

TDA51S485HC is a half-duplex enhanced transceiver designed for RS–485 data bus networks, which is fully compliant with TIA/EIA-485-A standard and is suitable for data transmission of up to 500kbps. Receivers have an exceptionally high input impedance, which places only 1/8 of the standard load on a shared bus and up to 256 transceivers.

The reliability design of A and B pin is emphasized, including driver output over current protection and enhanced ESD design. The ESD protection level of A, B pin can be up to 15kV (Human Body Model).

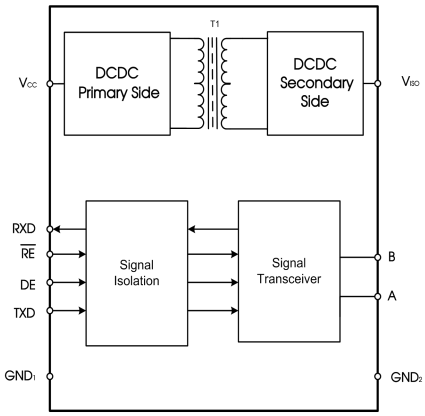
Contents

Pin Connection



Note: All GND_1 pins are internally connected.
All GND_2 pins are internally connected.

Internal Block



Function Table

Letter	Description
H	High-Level
L	Low-Level
X	Unrelated
Z	High Impedance

Table 1. Driver Function table

TXD	DE	Output	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
X	Open	Z	Z
Open	H	H	L
X	X	Z	Z

Table 2. Receiver Function table

Difference input $V_{ID} = (V_A - V_B)$	$\overline{RE}$	RXD
$-0.02\ V \leqslant V_{ID}$	L	H
$-0.2\ V < V_{ID} < -0.02V$	L	Uncertain
$V_{ID} \leqslant -0.2\ V$	L	L
X	H	Z
X	Open	Z

Open	L	H
Short	L	H
Idle(terminYted) bus	L	H

Note:

①$\overline{RE}$ =High when driving.

②DE=Low when receiving.

Pin Descriptions

Pin Number	Pin Name	Pin Functions
1	V_{CC}	Power supply. By using 0.1uF and 10uF ceramic capacitance ground(GND_1).
2	GND_1	Ground(Logic side).
3	RXD	Receiver output pin.
4	$\overline{RE}$	Receiver enable input. When $\overline{RE}$ is low, if (A − B) ≥ −20 mV, then RXD = high. if (A − B) ≤ −200 mV, then RXD = low.
5	DE	Driver enable input. When DE is high, outputs are enabled. When DE is low, outputs are high impedance. Drive DE low and $\overline{RE}$ high to enter shutdown mode.
6	TXD	Driver input pin.
7	GND_1	Ground(Logic side).
8	GND_1	Ground(Logic side).
9	GND_2	Ground (Bus Side).
10	SEL^1	V_{ISO} selection pin.
11	NC	No Connect.
12	A	RS485 Bus A Line.
13	B	RS485 Bus B Line.
14	NC	No Connect.
15	GND_2	Ground (Bus Side).
16	V_{ISO}	Insulation power output. By using 0.1uF and 10uF ceramic capacitance ground(GND_2).

Note: When SEL at V_{ISO}, V_{ISO}=5V; When SEL at GND_2 or floating, V_{ISO}=3.3V; When V_{CC}=3.3V, SEL must at GND_2 or floating; When V_{CC}=5V, SEL is not restricted.

Absolute Maximum Ratings

General test conditions: Free-air, normal operating temperature range (Unless otherwise specified).

Parameters	Unit
Supply voltage V_{CC}	-0.5V to +6V
Input voltage V_{in}	-0.5V to V_{CC}+0.5V
Output current I_O	-20mA to +20mA
Junction temperature T_J	< 150℃
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	−65°C to +150°C

Important: Exposure to absolute maximum rated conditions for an extended period may severely affect the device reliability, and stress levels exceeding the “Absolute Maximum Ratings” may result in permanent damage. Maximum voltage must not exceed 6 V.

Recommended Operating Conditions

Symbol	Recommended Operating Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3.15	3.3	5.5	V
V_I	A, B pin Voltage	-7		12	
V_{ID}	A, B Differential input voltage	-12		12	
V_{IH}	High-level input voltage	2			
V_{IL}	Low-level input voltage			0.8	
T_A	Operating temperature range	-40	25	105	℃
DR	Signaling rate			500	kbps

Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver						
V_{OD}	Differential drive output	No load, SEL at low or floating.	3.09	3.35	3.62	V
		No load, SEL at high	4.50	5.07	5.43	
		R_L=54Ω, Figure 7, SEL at low or floating.	1.17	1.4		
		R_L=54Ω, Figure 7, SEL at high	1.9	2.5		
$\|V_{OD3}\|$	Differential driver(With load) output	V_{test}= -7V to 12V, Figure6	1	1.4		
ΔV_{OD}	$\Delta\|V_{OD}\|$ for complementary output states	R_L=54Ω, Figure 7	-0.2		0.2	
V_{OC}	Common-Mode output voltage	R_L=54Ω, or R_L=100Ω Figure 7	1		3	
ΔV_{OC}	$\Delta\|V_{OC}\|$ for complementary output states	R_L=54Ω, or R_L=100Ω Figure 7			0.2	
V_{IH}	High input threshold voltage	TXD, DE, RE	2			
V_{IL}	Low input threshold voltage	TXD, DE, RE			0.8	
I_{IL}	Input leakage current	TXD, DE, RE=0 or 1	-20		20	uA
I_{OZ}	High-impedance output leakage current	DE=0, RE=0,V_{CC}=0 or 5V,V_{IN}=12V		60	100	uA
		DE=0, RE=0,V_{CC}=0 or 5V,V_{IN}=-7V	-100	-60		
I_{OS1}	Output short-circuit current(V_O=HIGH)	DE= RE=1, TXD=1, V_A=-7 V, V_B=12 V	29	44	62	mA
I_{OS2}	Output short-circuit current(V_O=LOW)	DE= RE=1, TXD=0, V_A=-7 V, V_B=12 V	29	44	62	mA
CMTI	Common mode transient immunity	V_{CM} = 1200V; Figure 12	100	150		kV/μS
C_I	Input capacitance	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF
Receiver						
$V_{IT(+)}$	Positive differential input threshold voltage	−7 V ≤ V_{CM} ≤ +12 V		-100	-20	mV
$V_{IT(-)}$	Negative differential input threshold voltage	−7 V ≤ V_{CM} ≤ +12 V	–200	-130		mV
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})	−7 V ≤ V_{CM} ≤ +12 V		30		mV
V_{OH}	RXD output high voltage	I_{OUT} = 4 mA, V_A − V_B = 0.2 V	Vcc − 0.4	Vcc − 0.2		V
V_{OL}	RXD output low voltage	I_{OUT} = −4 mA, V_A − V_B = −0.2 V		0.2	0.4	V
I_I	Bus input current	V_A or V_B =12V, other pins connect to 0V		0.04	0.1	mA
		V_A or V_B =12V, power off , other pins connect to 0V		0.06	0.13	
		V_A or V_B =–7V, other pins connect to 0V	-0.1	-0.04		
		V_A or V_B =–7V, power off , other pins connect to 0V	-0.1	-0.03		
I_{IH}	Input high voltage leakage current (RE)	V_{IH}=2V			20	uA
I_{IL}	Input low voltage leakage current (RE)	V_{IH}=0.8V	-20			
R_{ID}	Differential input resistance(A, B)	−7 V ≤ V_{CM} ≤ +12 V	384	430	478	kΩ
C_D	Differential input capacitance	f = 1.5 MHz, Vpp=1V Sin Signal, measure C_D		7		pF
C_I	Input to ground capacitance	V_I = 0.4 × sin (2πft), f = 1MHz		2		pF
Power supply and safeguard characteristic						
V_{ISO}	Isolated power supply output voltage	V_{CC}=5V, no load, SEL=0 or floating	3.17	3.35	3.53	V
		V_{CC}=5V, no load, SEL=1	4.50	5.07	5.43	V
I_{CC}	Logic side supply current	No load, V_{CC}=3.3V, RE=0, DE=1, DI=0, SEL=0	10	15	19	mA
		No load, V_{CC}=5.0V, RE=0, DE=1, DI=0, SEL=0	9	13	17	
		No load, V_{CC}=5.0V, RE=0, DE=1, DI=0, SEL=1	13	17	21	

		A, B with 54Ω load, V_{CC}=3.3V, RE=0, DE=1, DI=0, SEL=0	62	69	76	
		A, B with 54Ω load, V_{CC}=5V, RE=0, DE=1, DI=0, SEL=0	45	49	53	
		A, B with 54Ω load, V_{CC}=5V, RE=0, DE=1, DI=0, SEL=1	90	96	102	
		A, B with 100Ω load, V_{CC}=3.3V, RE=0, DE=1, DI=0, SEL=0	50	55	60	
		A, B with 100Ω load, V_{CC}=5V, RE=0, DE=1, DI=0, SEL=0	43	48	53	
		A, B with 100Ω load, V_{CC}=5V, RE=0, DE=1, DI=0, SEL=1	69	74	79	
		A, B with 120Ω load, V_{CC}=3.3V, RE=0, DE=1, DI=0, SEL=0	45	50	55	
		A, B with 120Ω load, V_{CC}=5V, RE=0, DE=1, DI=0, SEL=0	32	36	40	
		A, B with 120Ω load, V_{CC}=5V, RE=0, DE=1, DI=0, SEL=1	69	68	72	
ESD	HBM	A, B to GND_1			±6	kV
		A, B to GND_2			±8	kV
		Other pin			±6	kV
	Contact	A, B to GND_2			±15	kV
V_{IO}	Insulate voltage				5000	Vrms
R_{IO}	Insulate impedance		1			GΩ

Note:ESD indicators refer to the specifications for non electrified testing.

Transmission Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
-	Maximum data rate	Duty 40% ~ 60%			500	kbps
T_{PHL}, T_{PLH}	Driver propagation delay	R_{Diff}=54Ω , C_{L1}=C_{L2}=50pF Figure 8 Figure 11		16	48	ns
$\|T_{PHL}-T_{PLH}\|$	Driver skew ($\|T_{PHL}-T_{PLH}\|$)			3	12.5	ns
T_R, T_F	Driver rise/fall time			12	25	ns
t_{PZH}/ t_{PZL}	Driver off enable propagation delay			28	90	ns
t_{PZH}/ t_{PZL}	Driver on enable propagation delay			28	90	ns
T_{PHL}, T_{PLH}	Receiver propagation delay	C_L = 15pF Figure 9		80	165	ns
$\|T_{PHL}-T_{PLH}\|$	Receiver skew ($\|T_{PLH}-T_{PHL}\|$)			15	30	ns
T_R, T_F	Bus rise/fall time	R_{Diff}=54Ω , C_{L1}=C_{L2}=50pF Figure 9 Figure 10		2.5	4	ns
t_{PLH}	Receiver off enable propagation delay			28	90	us
t_{PHL}	Receiver enable propagation delay			43	52	us

Physical Specifications

Parameters	Value	Unit
Weight	0.4(Typ.)	g

Test Circuits

Note:Testing the condition burden capacitance including test to stretch forward and testing fixture parasitic capacitance. Testing semaphore upswing and droop to follow < 6ns, frequency100kHz, duty50%. resistance ZO = 54Ω.

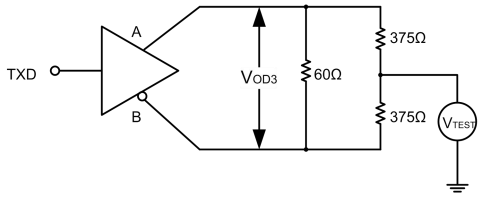


Figure 6. Driver test circuit, VOD with common-mode loading

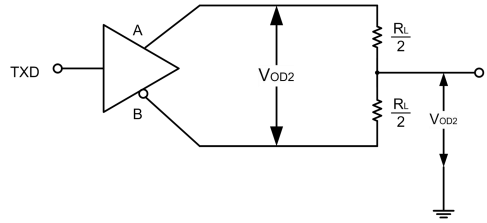
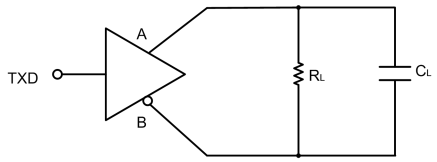
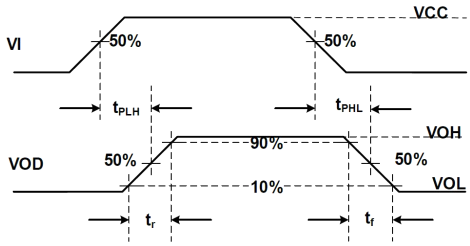


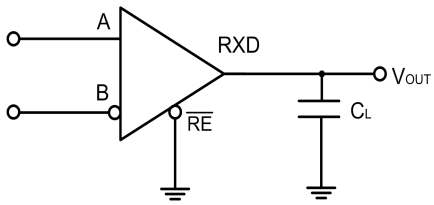
Figure 7. Driver test circuit

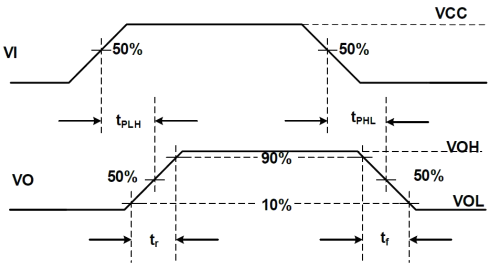




Note:C_L includes fixtures and a parasitic capacitor

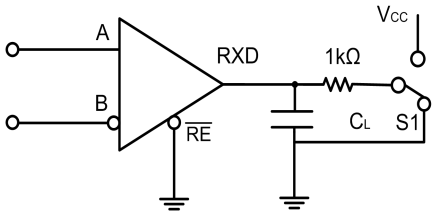
Figure 8. Drive propagation delay test circuit and wave forms





Note:C_L includes fixtures and a parasitic capacitor

Figure 9. Receiver propagation delay test circuit and wave forms



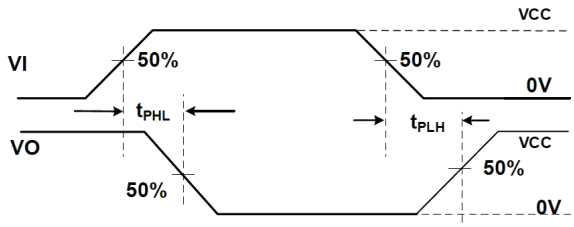
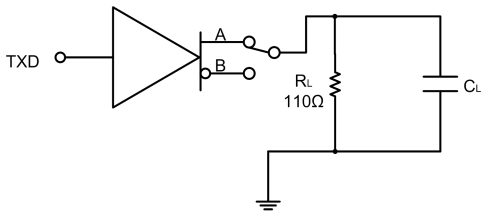
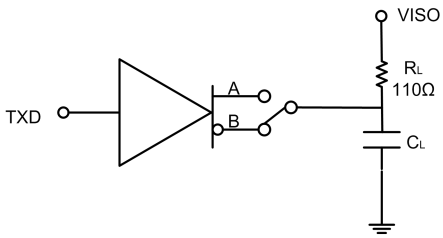
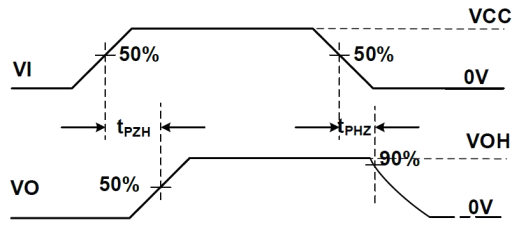
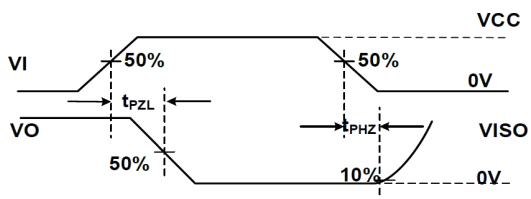


Figure 10. Receiver enable and off time test circuit









Note:C_L includes fixtures and a parasitic capacitor

Figure 11. Driver enable and off time test circuit

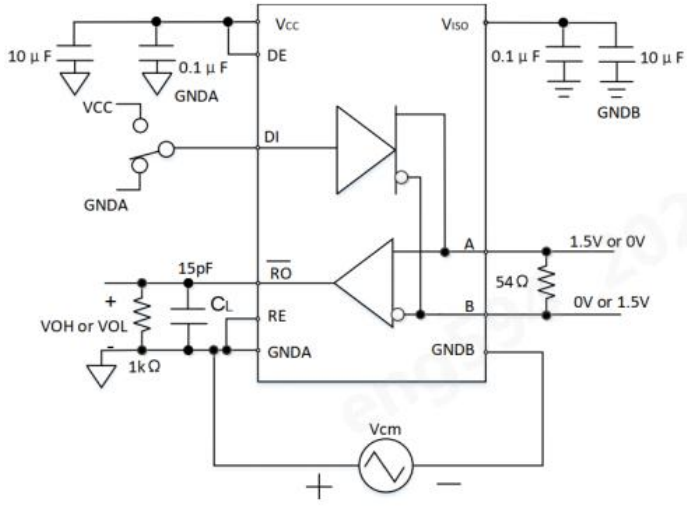


Figure 12. CMTI test circuit

Detailed Description

TDA51S485HC is a semi-duplex enhanced RS485 isolated transceiver with isolated power supply. In addition to an isolated power supply, each transceiver contains a drive and a receiver. The transceiver has a standby bus failure protection function to ensure that the receiver output is high when the receiver input is open, short, or when the bus is idle. The whole machine can monitor the overall working state of the module and limit the output high current, so as to prevent the bus overload or short circuit from causing non-recoverable damage to the transceiver.

Bus failure protection: In general, when -200mV < A - B < +50mV, the bus receiver will be in an indeterminate state.This phenomenon occurs when the bus is idle. Bus failure protection ensures that the receiver outputs a high level when the receiver input is open, short, or when the bus access port matches the resistance. TDA51S485HC receiver threshold voltage is relatively accurate, and the threshold voltage to the reference ground has a margin of at least +50mV, which can ensure that even if the bus differential voltage is 0V, the receiver output level is high, and meets the requirements of EIA/TIA-485 standard -200mV to +50mV.

The bus load capacity (256 point) : standard RS485 receiver input impedance is defined as 12 kΩ (unit load). A standard RS485 driver can drive at least 32 load units. TDA51S485HC bus receiver designed by 1/8 unit load, the input impedance is greater than 96 kΩ. As a result, the bus allows access to more transceivers (up to 256). TDA51S485HC can also be mixed with the standard RS485 transceiver with 32 unit loads (cumulative receiver load cannot exceed 32 units).

Drive output protection: TDA51S485HC avoids high output current and power consumption due to failures or bus collisions by two mechanisms,First overcurrent protection which provides fast short circuit protection throughout the common die range Second the thermal turn-off circuit forces the driver output into a low level when the core temperature exceeds the overtemperature reading value (typical value of 160℃).

Application Circuit

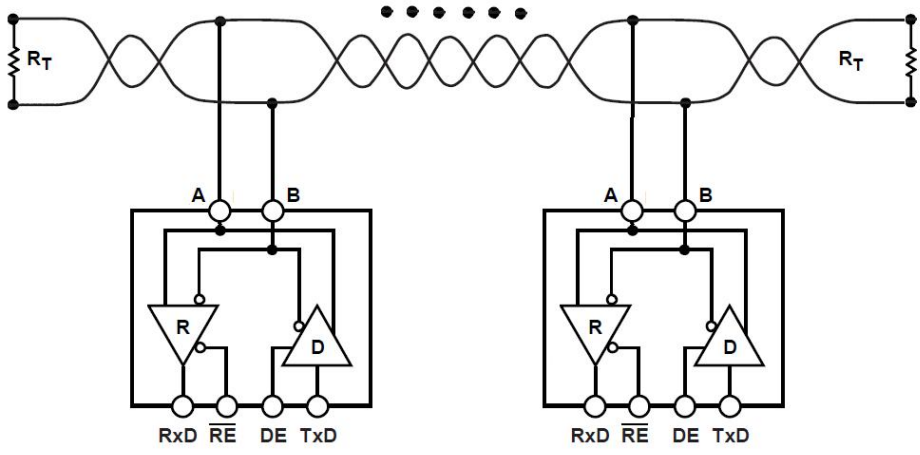


Figure13. Typical Application Circuit(Half-Duplex Network Topology)

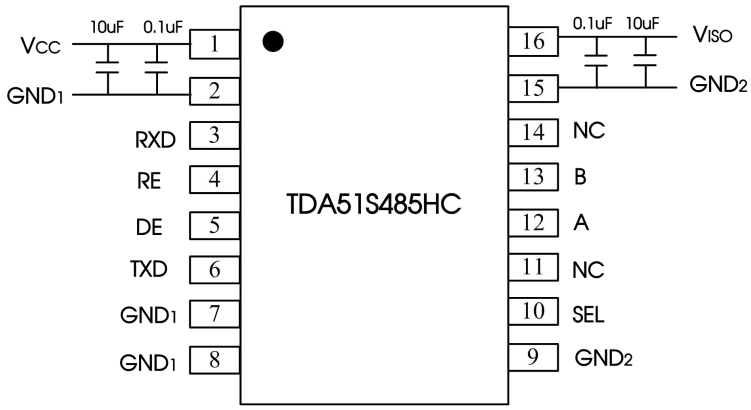
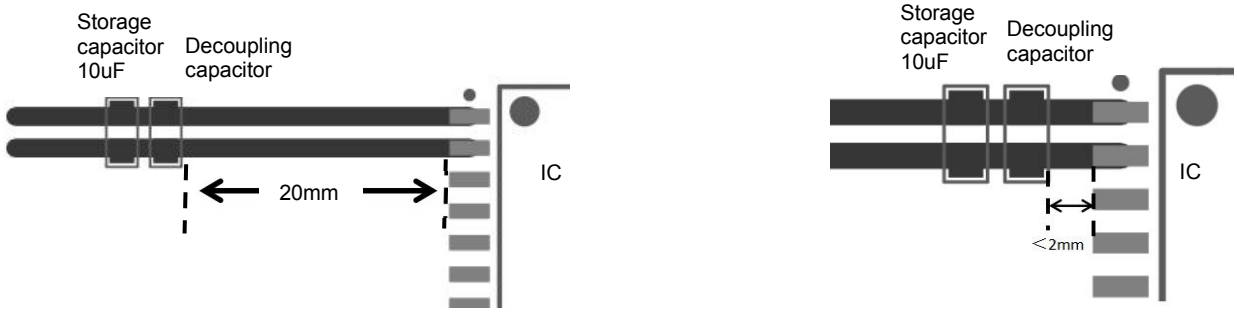


Figure14. Type PCB layout

PCB Design Instructions

1. The decoupling capacitors and energy storage capacitor of VCC and GND1, VISO and GND2 should be placed as close the chip pins as possible to the chip pins to reduce loop area and parasitic inductance of PCB traces. General control should be within 2mm. The decoupling capacitor is placed close the chip, and the energy storage capacitor is placed outside. As shown in Figre14-1.



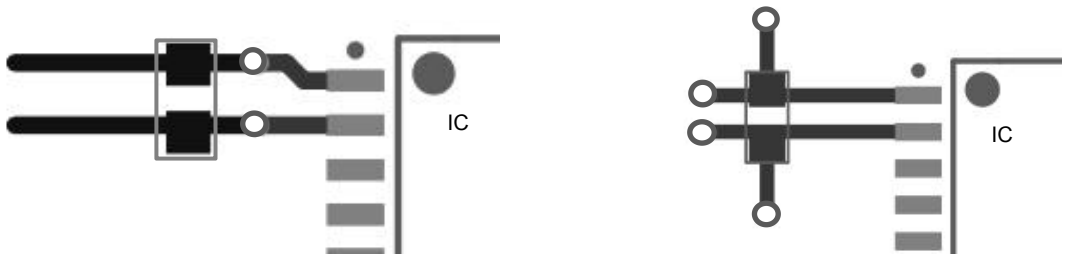
Not recommended

Recommend

Figure14-1

2. The power line width should be designed at least 0.5mm when wiring.

3. When it is necessary to place vias in the power supply line and the ground wire, the position of the vias should be placed on the outside of the capacitor relative to the chip pins ,rather than between the capacitor and the chip, as shown in the figure14-2 below to reduce the number of vias effect of parasitic inductance.



Not recommended

Recommend

Figure14-2

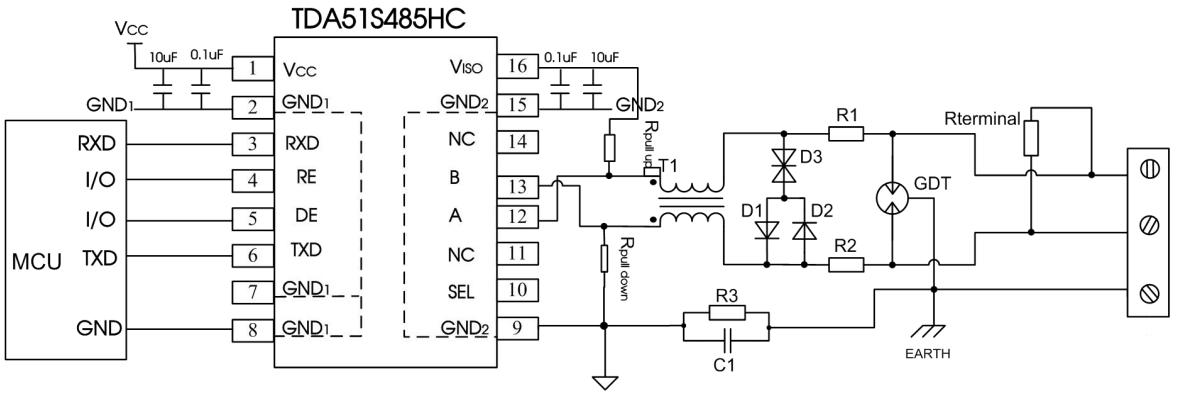


Figure15. Port protection circuit for harsh environments

Recommended components and values:

Component	Recommended part, value	Component	Recommended part, value
R3	1MΩ	R1, R2	2.7Ω/2W
C1	1nF, 2kV	D1, D2	1N4007
T1	ACM2520-301-2P	D3	SMBJ8.5CA
GDT	B3D090L	$R_{terminal}$	120Ω

As the modules internal A / B lines come with its own ESD protection, which generally satisfy most application environments without the need for additional ESD protection devices. For harsh and noisy application environments such as motors, high voltage/current switches, lightning and similar however, we recommended that the user protects the module' s A / B lines with additional measures and external components such as TVS tube, common mode inductors, Gas discharge tube, shielded twisted pair of wires with the same single network Earth point. Figure 15 shows our recommended circuit diagram for such type of applications with components and values given in the table above. This recommendation is for reference only and may have to be adapted accordingly with appropriate component values in order to match the actual situation and application.

Note: Select the $R_{terminal}$ according to the actual application.

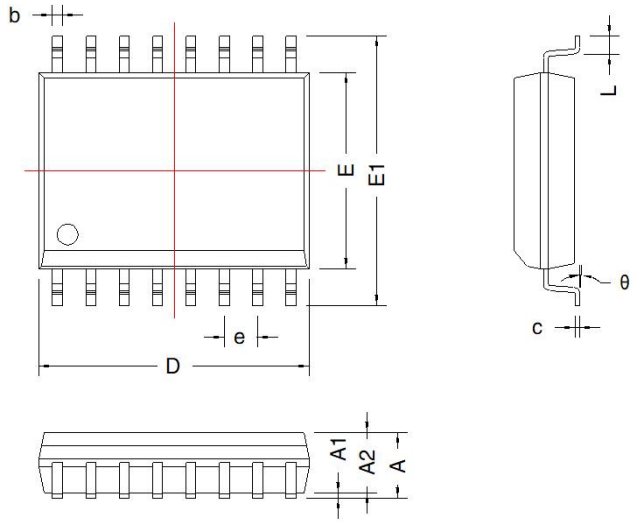
Using Suggests

To maintain A - B bus idle stability, we need at least one node will pull up A to V_{ISOIN} and drop down B to GND2 on the bus. Overall network at the same time pull up and drop down resistance of the parallel value must around 380Ω to 420Ω(0.2W).

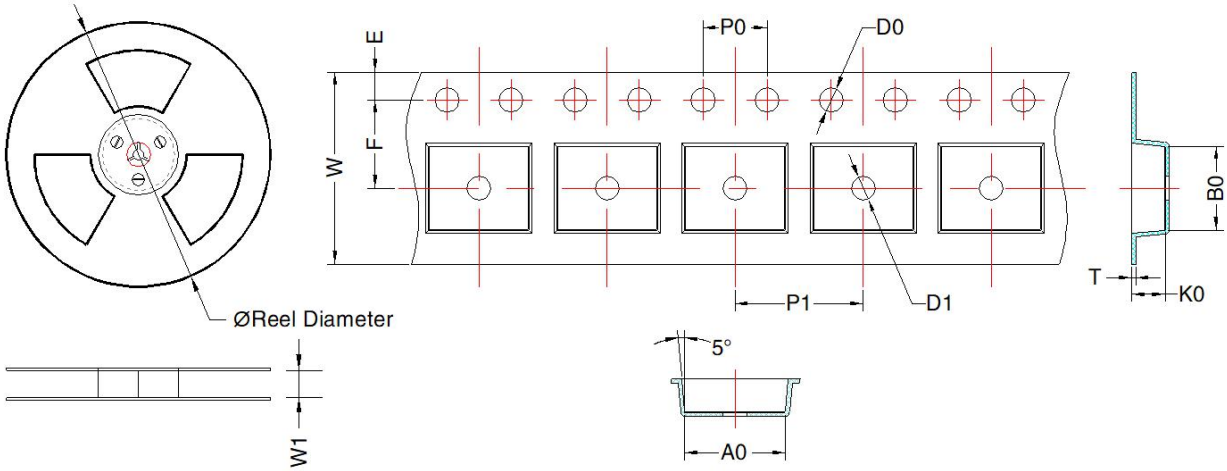
Ordering Information

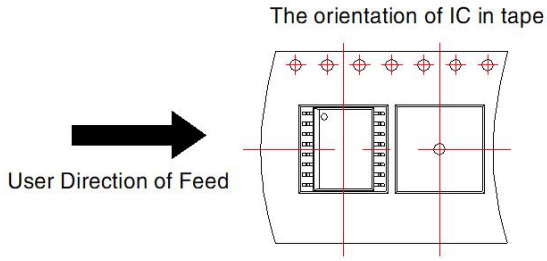
Part number	Package	Number of pins	Product marking	Tape & Reel
TDA51S485HC	SOIC	16	TDA51S485HC	1k/REEL

THIRD ANGLE PROJECTION



SOIC–16				
Mark	Dimension(mm)		Dimension(inch)	
	Min	Max	Min	Max
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
A2	2.25	2.35	0.089	0.093
D	10.2	10.4	0.402	0.409
E	7.4	7.6	0.291	0.299
E1	10.1	10.5	0.340	0.413
L	0.55	0.85	0.022	0.033
b	0.35	0.43	0.014	0.017
e	1.27TYP		0.05TYP	
c	0.15	0.30	0.006	0.012
θ	0°	8°	0°	8°





Device	Package Type	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	T (mm)	W (mm)	E (mm)	F (mm)	P1 (mm)	P0 (mm)	D0 (mm)	D1 (mm)
TDA51S485HC	SOIC-16	1000	330.0	16.4	10.9 ± 0.2	10.7 ± 0.2	3.2 ± 0.2	0.3 ± 0.05	16.0 ± 0.3	1.75 ± 0.1	10.5 ± 0.1	12.0 ± 0.1	4.0 ± 0.1	1.5 ± 0.1	1.5 ± 0.1

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