

## NS4251 3.0W/Channel Stereo Class AB/D Audio Amplifier With Headphone Amplifier

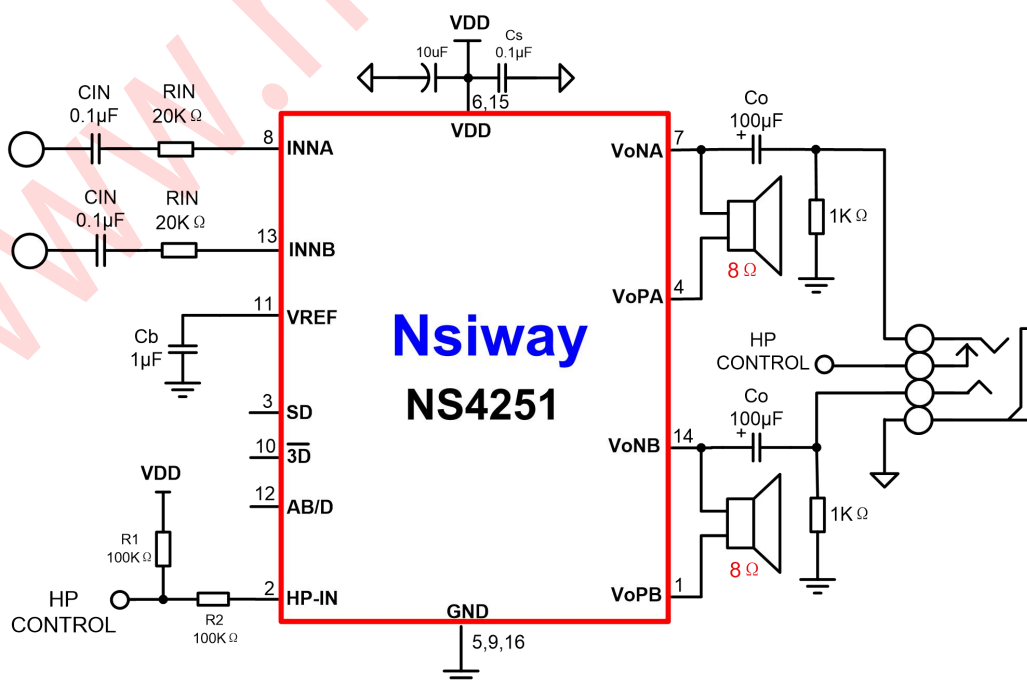
### 1 Features

- 3.0V to 5.25V Single-supply Operation.
- Class AB /Class D Mode Selectable.
- 3D Surround Sound Simulation Function.
- Stereo Headphone Amplifier .
- 3W per Channel Output Power at 10% THD+N with a 4ohm Load And 5V Power supply in Class D Mode.
- THD+N=0.1%@VDD=5V/Po=1W
- Independent Shutdown for Class AB/D and Headphone Amplifiers.
- Integrated Click and Pop Suppression.
- Over-Current and Input UVLO Protection, etc.
- Available QFN3×3-16 package.

### 2 Applications

- Laptops.
- Desktop PCs.
- Low sound systems.

### 4 Typical Application Circuit



### 3 General Description

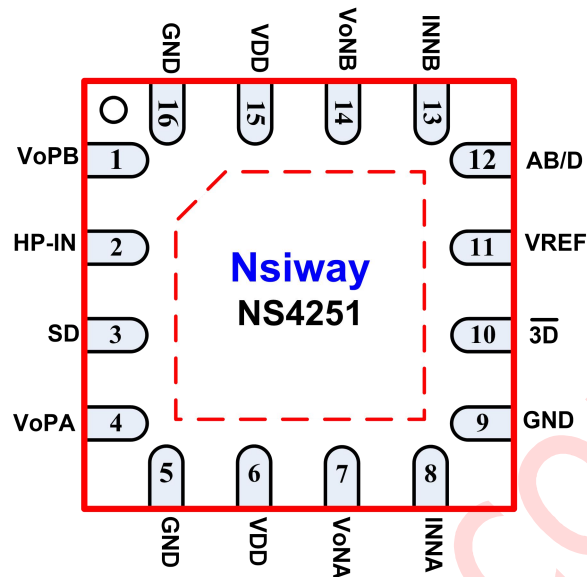
NS4251 is a stereo Class AB/D audio amplifier with headphone amplifier in single-ended mode. The headphone amplifier require a bulky DC-blocking capacitor between the headphone and the amplifier.

AB/D Control pin enables the chip to operate in either class AB or class D operating mode. NS4251 uses advanced technology to greatly reduce EMI interference in the full bandwidth range, minimizing the impact on other components. In order to simplify the audio system design, the bridge connected speaker amplification mode and the single-end stereo headphone amplifier are implemented on the same chip. The PWM modulation structure of NS4251 with Free-filters and built-in feedback resistor reduce external components, PCB area and system cost. With the internal protection of Over-current and Under-Voltage, it can effectively protect the chip from being damaged under abnormal working conditions.

NS4251 is available in QFN3×3-16 package.

## 5 Pin Configuration

QFN3×3-16 Diagram of NS4251 is shown :



Pin Description of NS4251:

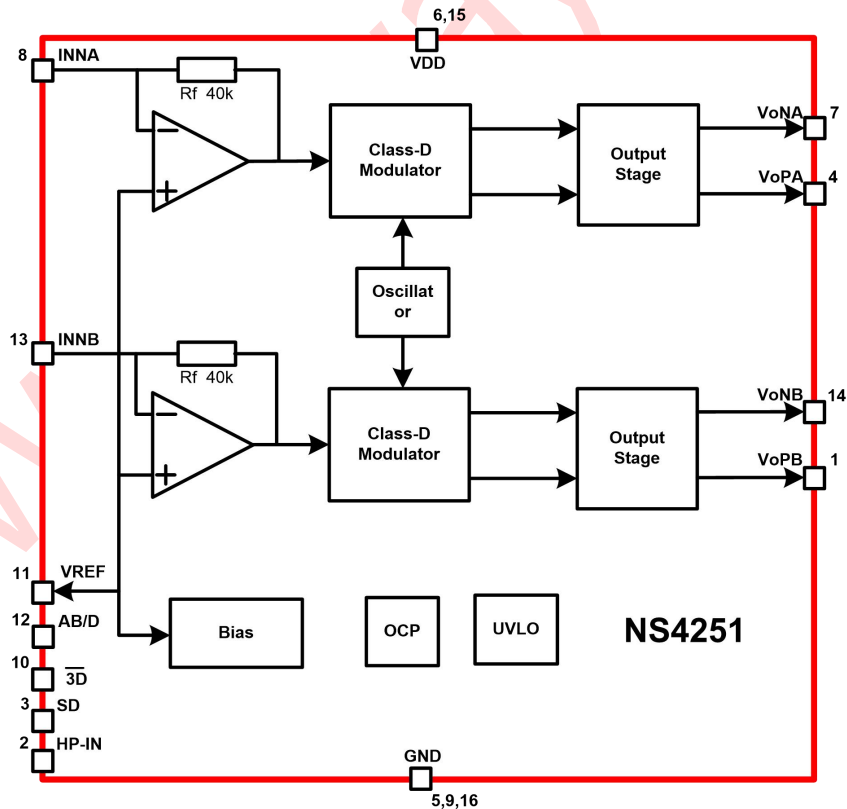
No.	Pin Name	Description
1	VoPB	Channel B positive output pin
2	HP-IN	headphone amplifier mode controller
3	SD	Shutdown Mode control pin
4	VoPA	Channel A positive output pin
5	GND	Power ground
6	VDD	Positive power input
7	VoNA	Channel A negative output pin
8	INNA	Input channel A negative input
9	GND	Power ground
10	$\overline{3D}$	3D function control pin
11	VREF	Bypass capacitor positive pin
12	AB/D	Class AB/D Mode select pin
13	INNB	Input channel B negative input
14	VoNB	Channel B negative output pin
15	VDD	Positive power input
16	GND	Power ground

## 6 Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply Voltage VDD	-0.3	5.5	V
Storage Temperature	-65	150	oC
ESD Rating(HM)		4000	V
Junction Temperature		150	oC
Operating Temperature	-40	85	oC
thermal resistance			
JC		20	°C/W
JA		80	°C/W
Welding temperature		260	°C

Notes: Over these operating parameters above, the chip may be permanently damaged. The above parameters are only the limits of the operating conditions. It is not recommended that the device work beyond the recommended conditions. Exposure over time at any limit operating conditions, the reliability and lifetime of the chip may be affected.

## 7 Block Diagram

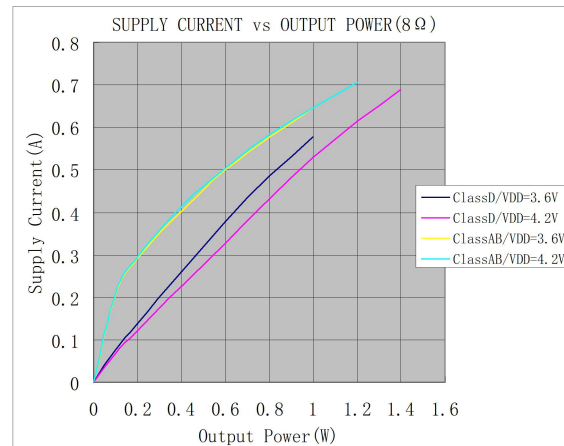
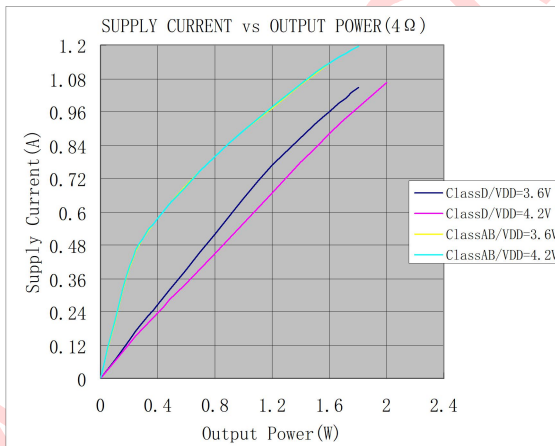
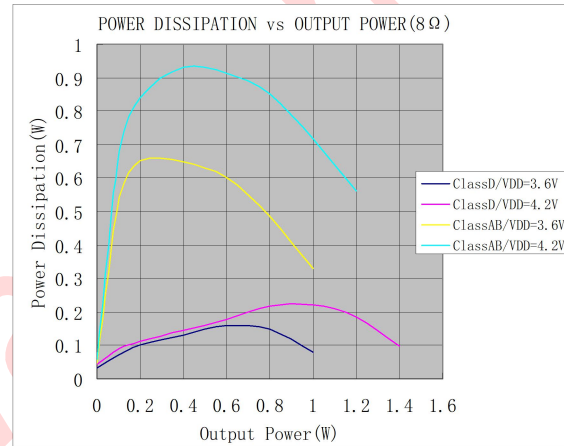
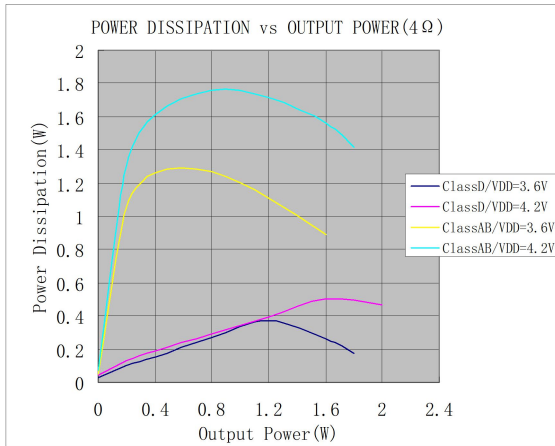
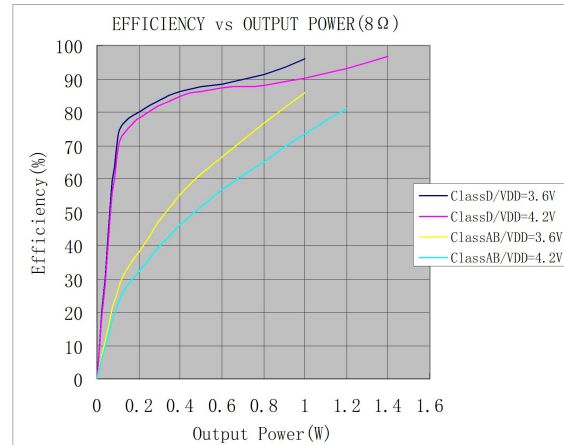
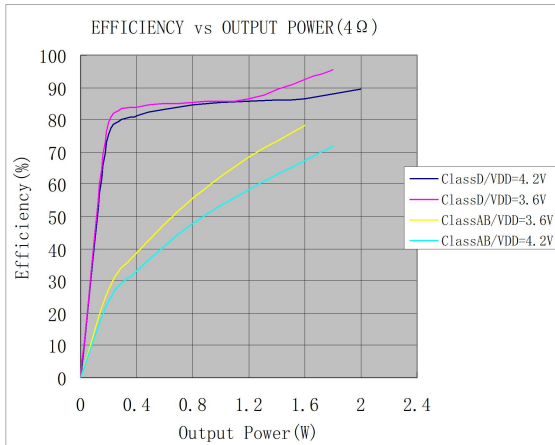


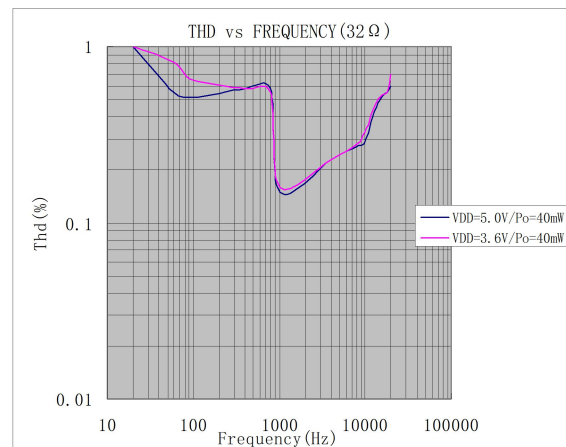
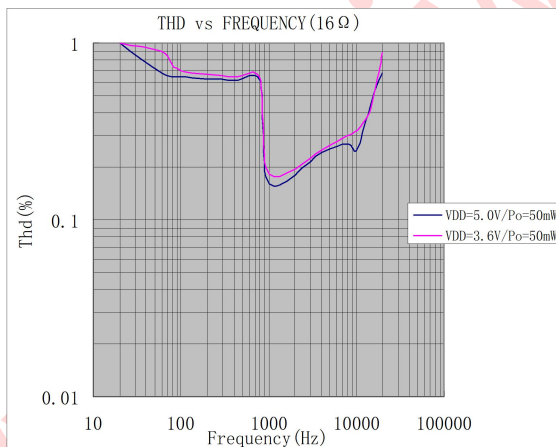
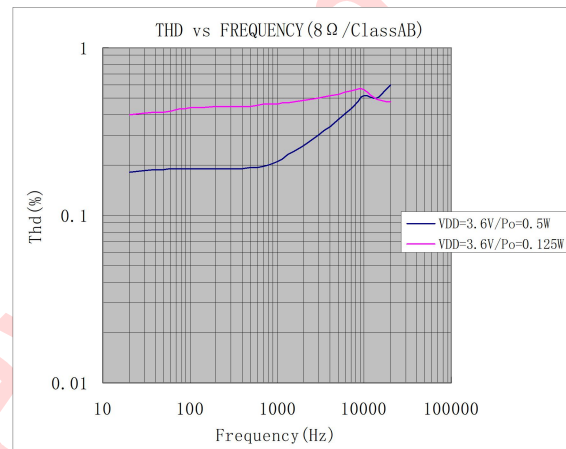
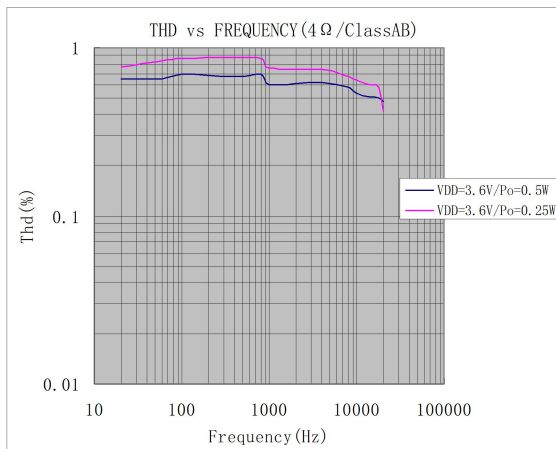
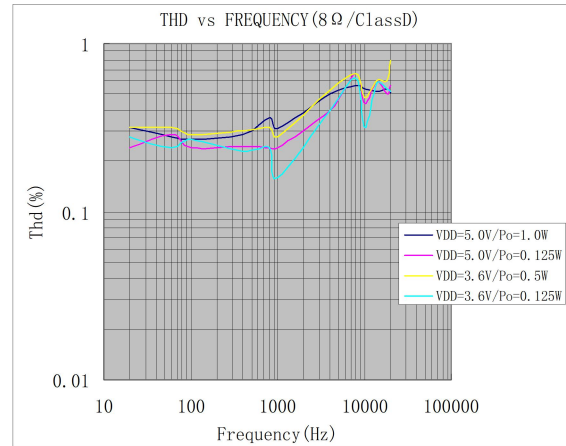
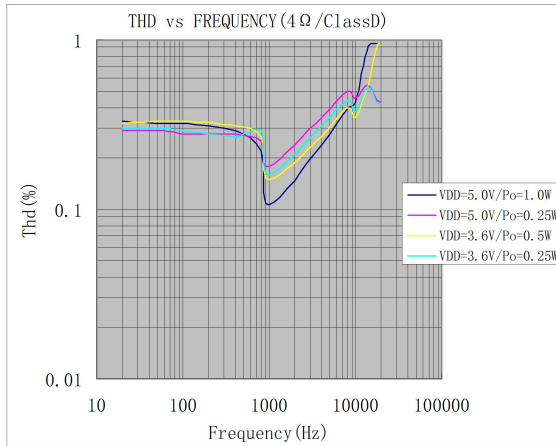
## 8 Electrical Characteristics

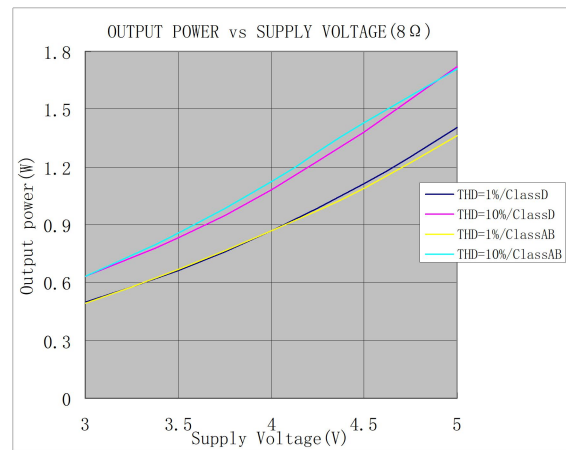
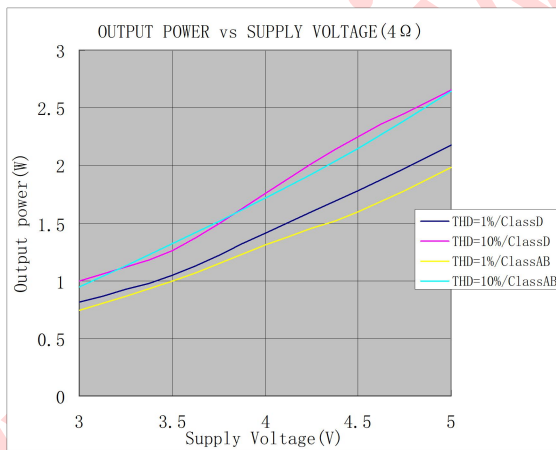
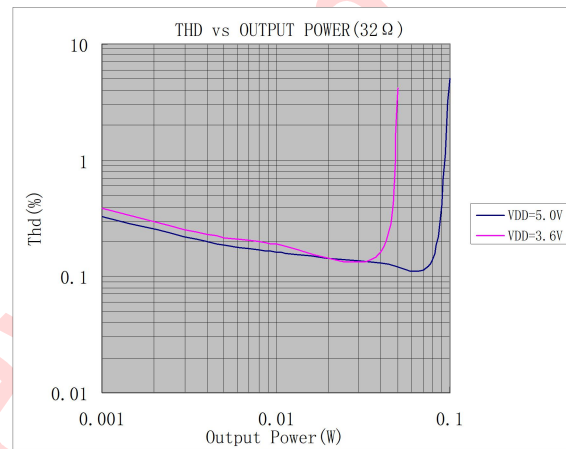
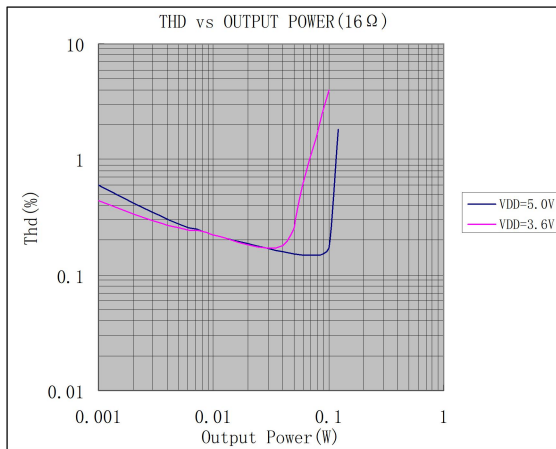
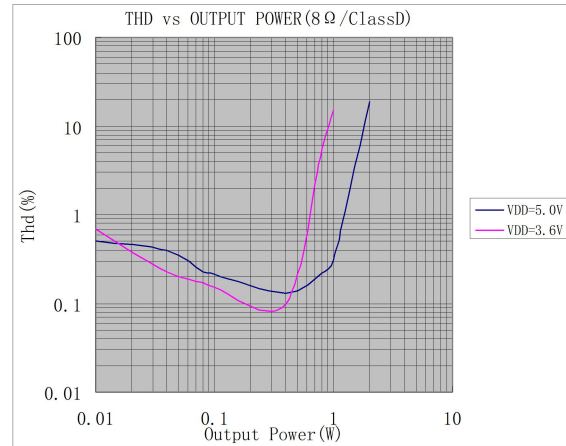
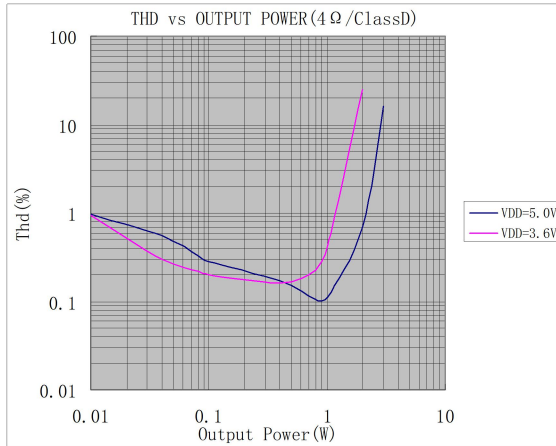
Operating conditions(unless otherwise stated) :  $T_A=25^{\circ}\text{C}$ .

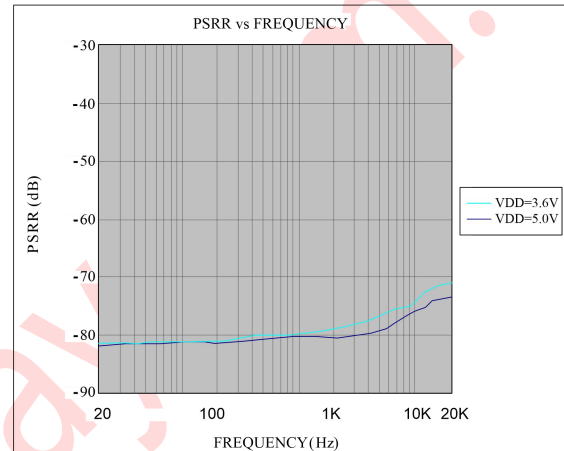
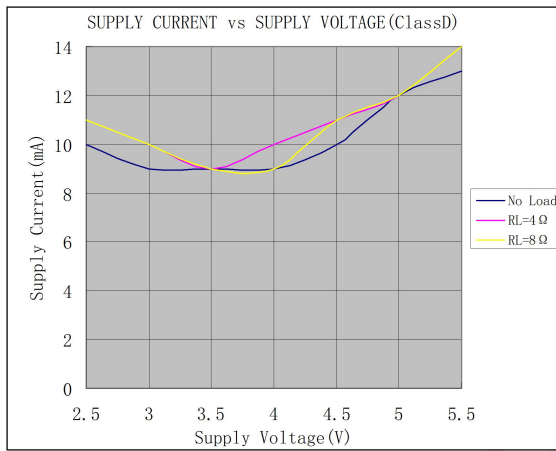
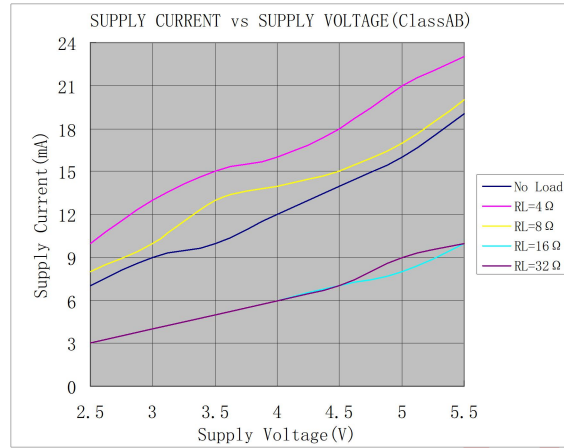
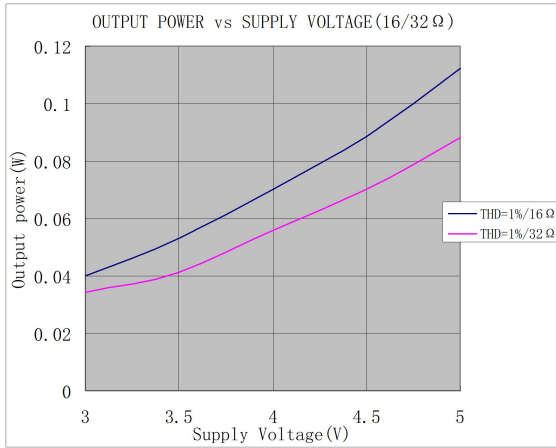
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply Voltage		3.0		5.25	V
$I_{DD}$	Quiescent Current	$V_{DD}=3.6\text{V}, V_{IN}=0\text{V}, \text{No load}$		11		mA
		$V_{DD}=5.0\text{V}, V_{IN}=0\text{V}, \text{No load}$		20		mA
$I_{SD}$	Shutdown Current	$V_{SD}=3.3\text{V}$		1	10	$\mu\text{A}$
$V_{OS}$	Output offset voltage			10	40	mV
$R_O$	Output resistance			3		K
PSRR	Power supply rejection ratio	217Hz			-80	dB
		20KHz			-72	dB
CMRR	Common mode rejection ratio			-70		dB
$f_{SW}$	Carrier clock frequency	$V_{DD}=3.0\text{V to }5.25\text{V}$		450		kHz
$V_{IH}$	CTRL High voltage		1.4			V
$V_{IL}$	CTRL Low voltage				0.4	V
Headphone Amplifier Output mode( $V_{DD}=5.0\text{V}$ )						
$P_O$	Output power	THD = 1%, $f=1\text{KHz}, R_L=16\Omega$		110		mW
		THD = 1%, $f=1\text{KHz}, R_L=32\Omega$		80		mW
$X_{TALK}$	Stereo separation	$R_L=32\Omega, P_o=10\text{mW}$		-85		dB
THD	Harmonic Distortion&Noise	$R_L=16\Omega/32\Omega, f=1\text{KHz}, P_o=10\text{mW}$		0.2		%
SNR	Signal-to-Noise Ratio	$R_L=32\Omega, P_o=10\text{mW}$		75		dB
Speaker Output Mode ( $V_{DD}=5.0\text{V}$ )						
$P_O$	Output power	THD = 1%, $f=1\text{KHz}, \text{ClassAB}, R_L=8\Omega$		1.3		W
		THD = 10%, $f=1\text{KHz}, \text{ClassAB}, R_L=8\Omega$		1.7		W
		THD = 1%, $f=1\text{KHz}, \text{ClassD}, R_L=4\Omega$		2.1		W
		THD = 1%, $f=1\text{KHz}, \text{ClassD}, R_L=8\Omega$		1.4		W
$P_O$	Output power	THD = 10%, $f=1\text{KHz}, \text{ClassD}, R_L=4\Omega$		3.0		W
		THD = 10%, $f=1\text{KHz}, \text{ClassD}, R_L=8\Omega$		1.7		W
THD+N	Harmonic Distortion&Noise	$f=1\text{KHz}, \text{ClassD}, P_o=0.5\text{W}, R_L=4\Omega/8\Omega$		0.2		%
Stereo Isolation	Stereo separation	$R_L=4\Omega, P_o=0.5\text{W}$		-80		dB
SNR	signal-to-noise ratio	$R_L=4\Omega, P_o=0.5\text{W}$		75		dB

## 9 Typical Characteristic









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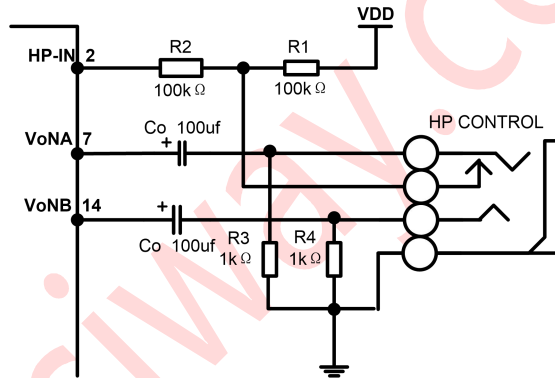
## 10 Application Information

### 10.1 Operating Mode Selection

The operating mode of NS4251 is set by pin SD, AB/D and HP-IN, as shown in the following table.

SD	AB/D	HP-IN	Operating
low	low	Logic low	Class AB Mode
low	high	Logic low	Class D Mode
low	low/high	Logic high	Headphone Amplifier Mode (class AB single-ended output)
high	low/high	Logic low /high	Low power shutdown mode

The output mode can be selected automatically through the output headphone amplifier plug. Typical application is shown in the following figure. The control part of headphone amplifier is as follows.



When there is no headphone amplifier plug to access the plug, the divider resistance R1-R3 make the voltage supplied to the HP-IN pin (Pin2) approximately 50mV (low level), enabling the NS4251 to operate in bridge output mode. When the headphone amplifier plug is inserted into the headphone amplifier plug to separate the headphone amplifier plug from R3, the HP-IN pin is pulled up to high level. NS4251 works in single-ended output mode (headphone amplifier application).

#### Gain of Output Mode

When NS4251 is working in class D Mode, the gain of each channel is:  $A_{VD} = \frac{260k}{R_{IN}} (\text{Class\_D})$

When NS4251 is working in class AB Mode, the gain of each channel is:  $A_{VD} = \frac{240k}{R_{IN}} (\text{Class\_AB})$

When NS4251 is working in Headphone Amplifier Mode, the gain of each channel is:  $A_{VD} = \frac{240k}{2 \cdot R_{IN}}$

### Selection of input $C_{IN}$ and $R_{IN}$

The input capacitance and the input resistance form a high-pass filter, the cut-off frequency is:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_I}$$

In many applications, speakers cannot reproduce low frequency speech below 100Hz, so large capacitors can not improve the system performance. In addition to considering the system performance, the suppression performance of on/off switching noise is affected by capacitance. The larger the coupling capacitance is, the larger the delay of the feedback network will be and the POP noise will be caused. Therefore, a small coupling capacitance can reduce the noise. If  $C_i$  is 0.1uF~0.39uF, the system performance can be satisfied.

### Selection of bypass capacitor

$C_b$  determines the stability of NS4251's static operating point, so its value is critical when turning on a burst input signal. The larger the  $C_b$  is, the slower the chip output tilts to the static DC voltage ( $V_{DD}/2$ ), the smaller the popping sound.  $C_b$  is set to 1uF to obtain a turn-off function with less "ticking" and "popping".

### Selection of power filter capacitance

In the amplifier application, the power supply bypass design is very important, especially for the noise performance and power supply voltage suppression performance. The filter capacitor is required to be close to the chip power supply pin. Typical capacitance is an electrolytic capacitor of 10uF with a ceramic capacitor of 0.1uF.

### Shutdown Mode

When the SD pin level is high, the chip is in the state of low power off. In practice, it is recommended that SD pins be connected to a pull resistor. This ensures that the chip is in off state when connected with SD pin hanging in the air or high resistance.

### Class AB/D switching function

When the AB/D pin is high, the chip works in class D. When the pin is low, the chip works in class AB. The AB/D pin should not be hanging in the air.

### 3D surround sound simulation function

3D surround sound simulation function is controlled by the /3D pin. 3D function is turn on at low power level, and it is turn off at high level.

### 10.2 Pop noise reduction function

The Pop Noise Reduction Function works in the cases of Power-on, Power-off, Power-down on, and Power-down off. And, the pop-noise can be suppressed according to control the power down by the following procedure.

- 1) Power down mode is cancelled after power-on and the power supply is stabilized enough.
- 2) Power down mode is set before Power-off.

### 10.3 Efficiency

NS4251 uses extended spectrum technology to fully optimize the circuit design of the new Class D amplifier to improve the efficiency. When the chip works in class D, up to 90% efficiency is more suitable for portable audio products.

## 11 Application Notes

### 11.1 EMI interference source of class D audio amplifier

EMI interference of class D audio amplifier mainly comes from two places. One is the jump of current in the power cord, the other is the edge of the output pulse signal. EMI mainly radiates out through the wiring of the PCB, through the hole, and the wiring of the speaker, interfering with other components.

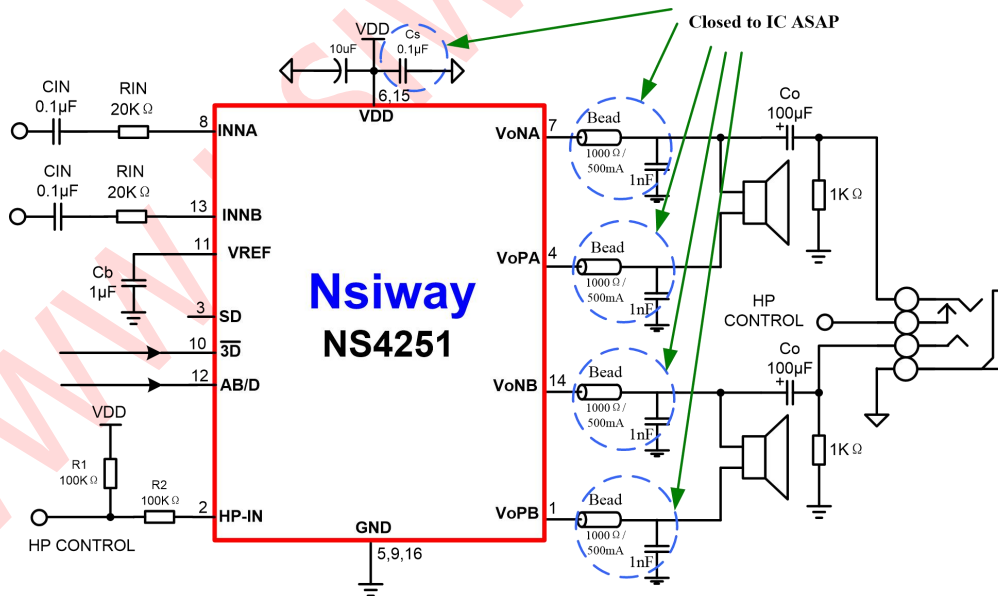
### 11.2 Low EMI

The battery life of portable audio devices is directly related to the efficiency of audio amplifiers. The efficiency of class D audio amplifiers is great important in extending battery life. However, the EMI interference of traditional Class D audio power amplifier directly limits the use of amplifier with radio module, this causes problems for many design engineers. NS4251 uses advanced EMI enhancement technology to effectively reduce EMI interference.

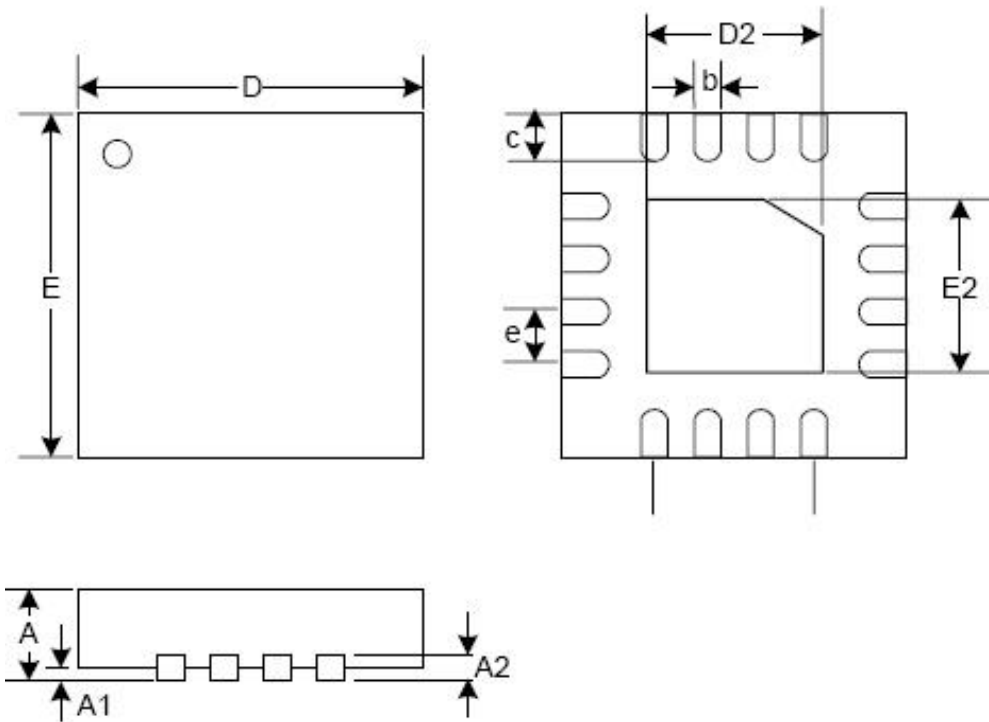
### 11.3 Application design reference

To Maximize the performance of class D power amplifier, the EMI interference of class D audio amplifier can be minimized from the following aspects:

1. Between the output to the speaker, the line should be short as possible, as wide as possible, and as far as possible away from sensitive signal lines and circuits.
2. The decoupling capacitor of the power pin should be as close to the chip pin as possible. The power cord and ground wire are best connected by star.
3. When EMI interference is serious due to space limitation, adding magnetic beads and capacitors at the output can effectively suppress EMI interference. Magnetic beads and capacitance should be as close to the chip pin as possible. The following is the application design reference circuit of NS4251 with magnetic beads:



## 12 Packaging information



QFN-16L-3x3				
Sy mbol	Min	Typ	Max	U nit
A	0.800	0.850	0.900	mm
A1	0.000		0.050	
A2	0.203(BSC)			
b	0.200	0.250	0.300	
c	0.300	0.350	0.450	
D	2.950	3.000	3.050	
D2	1.600	1.650	1.700	
e	0.500(BSC)			
E	2.950	3.000	3.050	
E2	1.600	1.650	1.700	

## 13 Revision History

Notice: Shenzhen Nsiway Co. LTD. Reserve the right to modify the datasheet at anytime, and without notice, Only Shenzhen Nsiway Co. LTD. have the right to explain the content in this datasheet.