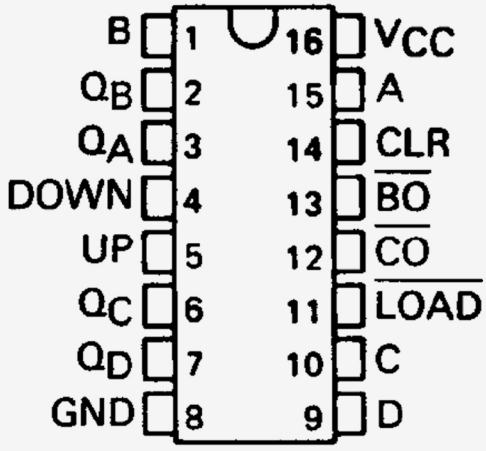
XD74LS192 DIP-16 XD74LS193 DIP-16

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
74LS192,74LS193	32 MHz	95 mW

74LS192 74LS193
(TOP VIEW)



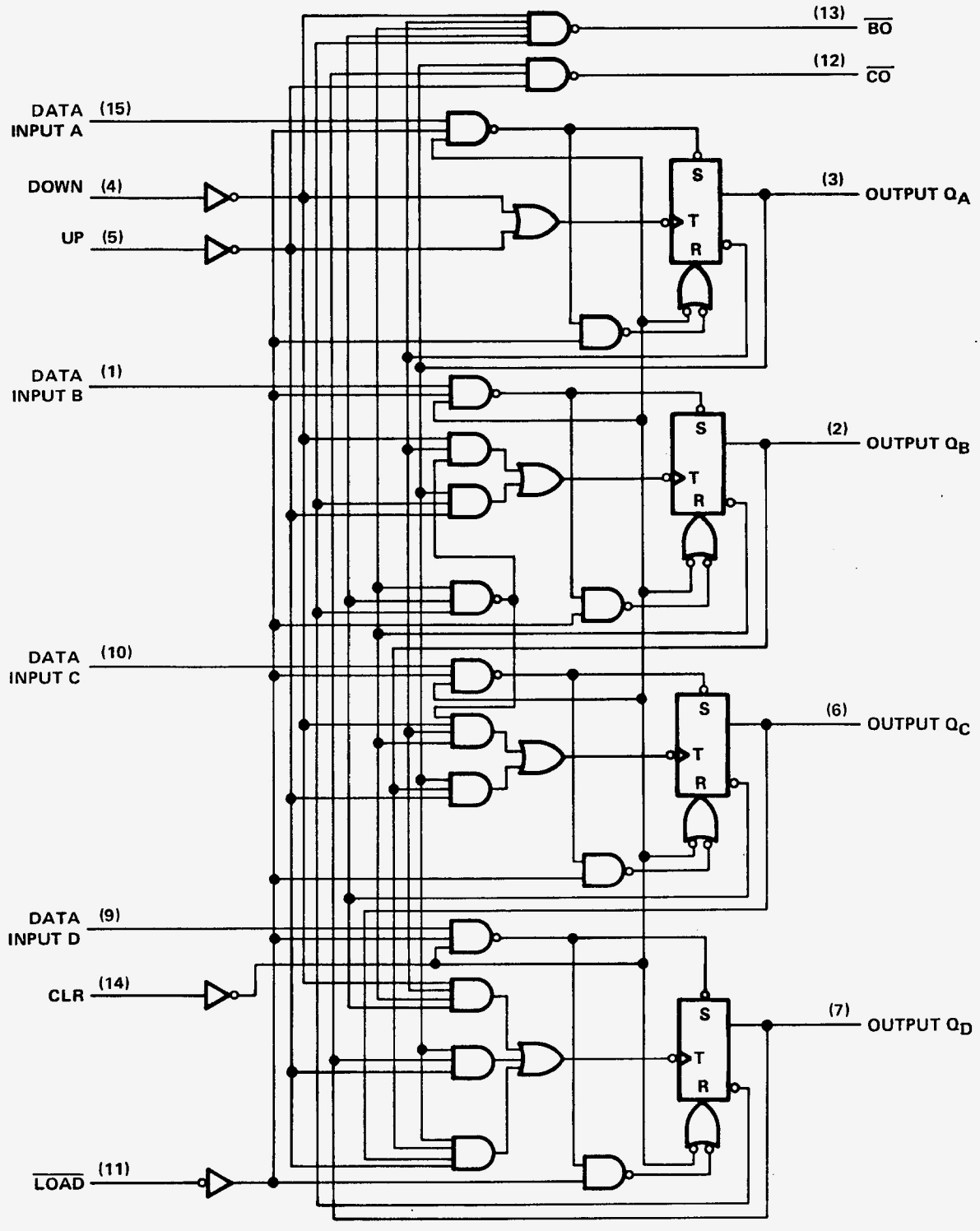
description

These monolithic circuit, synchronous reversible (up/down) counters having • complexity of 55 equivafont gates. 74LS192 circuits are BCD counter* 74LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentty with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-dockl counters.

The outputs of the four matter-tlave flip-flops are triggered by a low-to-high-l«vel trantition of either count (dock) input. The direction of counting is determined by which count input it pulsed white the other count input to high.

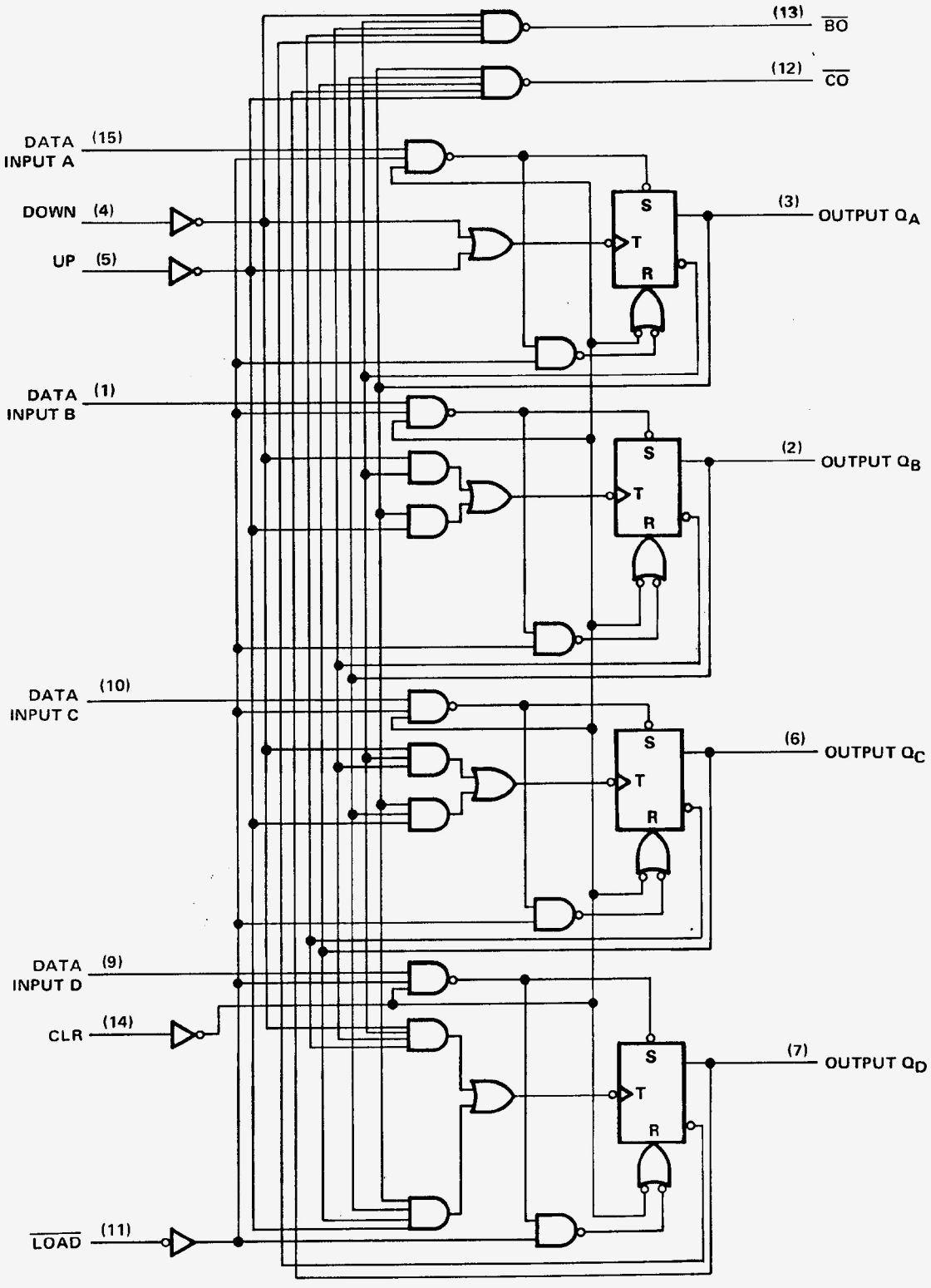
AM four counters are futty programmable; that b, each output may be preset to either lovel by entering the desired data at the data inputs while the load input M low. The output wil change to agree with the data inputs independently of tho count pulm. This featureallows the counters to be used as moduto-N dividefs by simply modifying the count length with the preset inputs.A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements.This reduces the number of dock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down-counting functions. The borrow output produces a pcjtse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and cany outputs to the count-down and count-up inputs respectively of the succeeding counter.



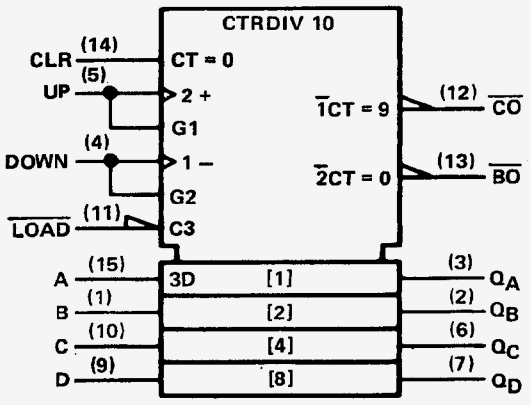
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

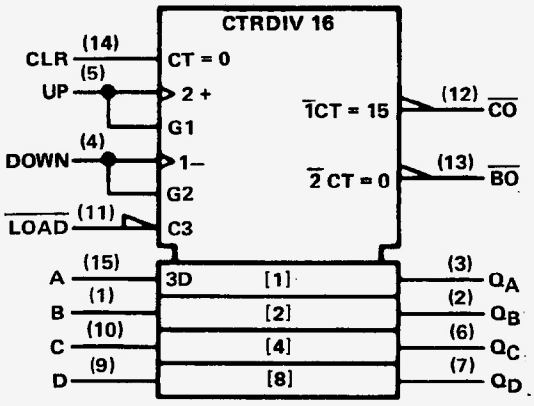


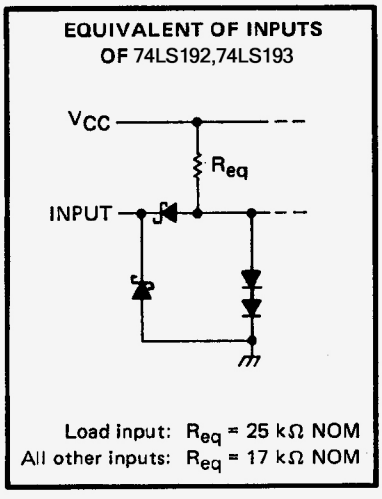
logic symbols†

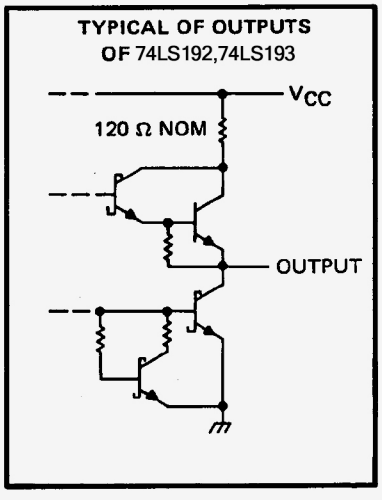
74LS192



74LS193





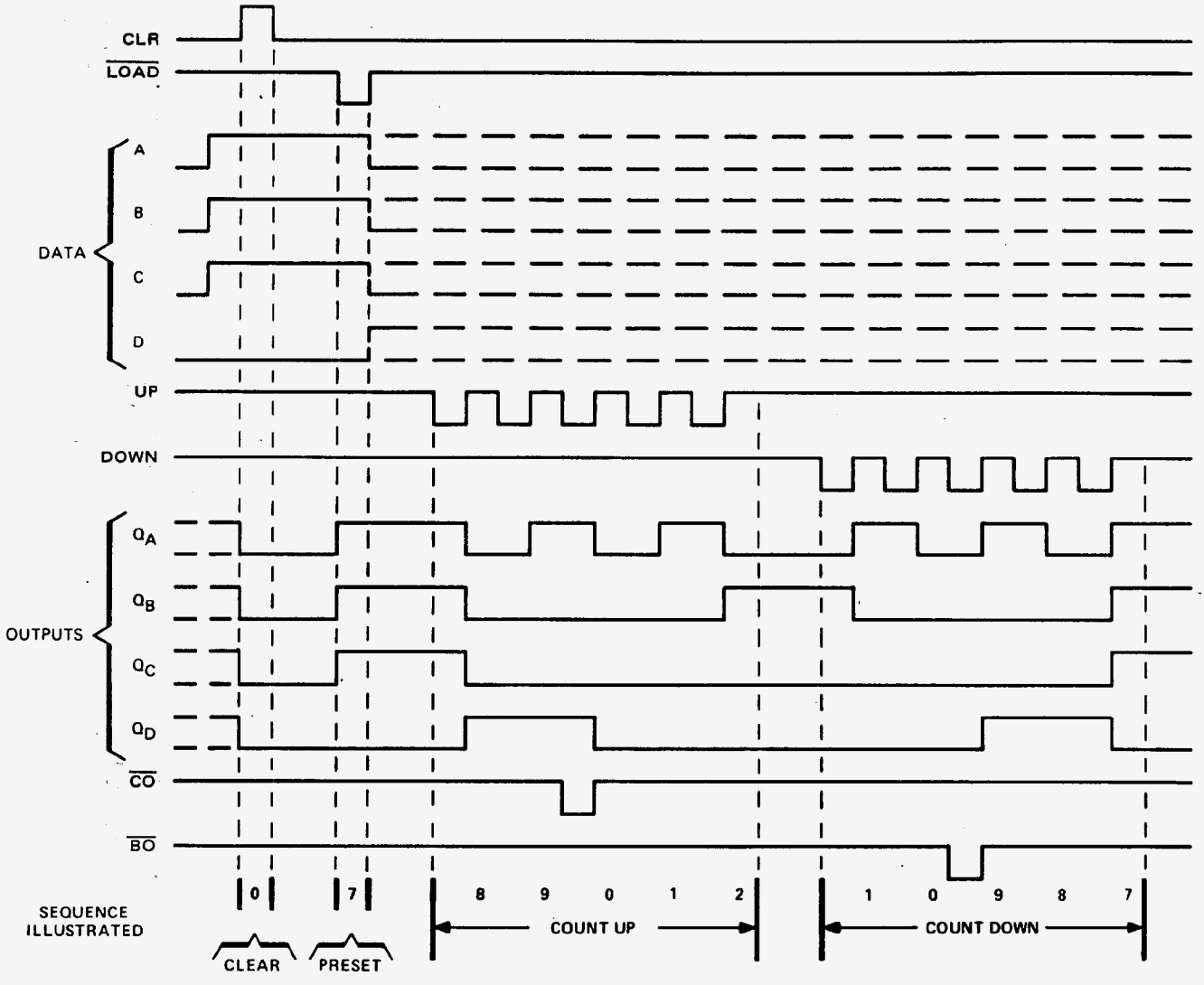


74LS192 DECADE COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



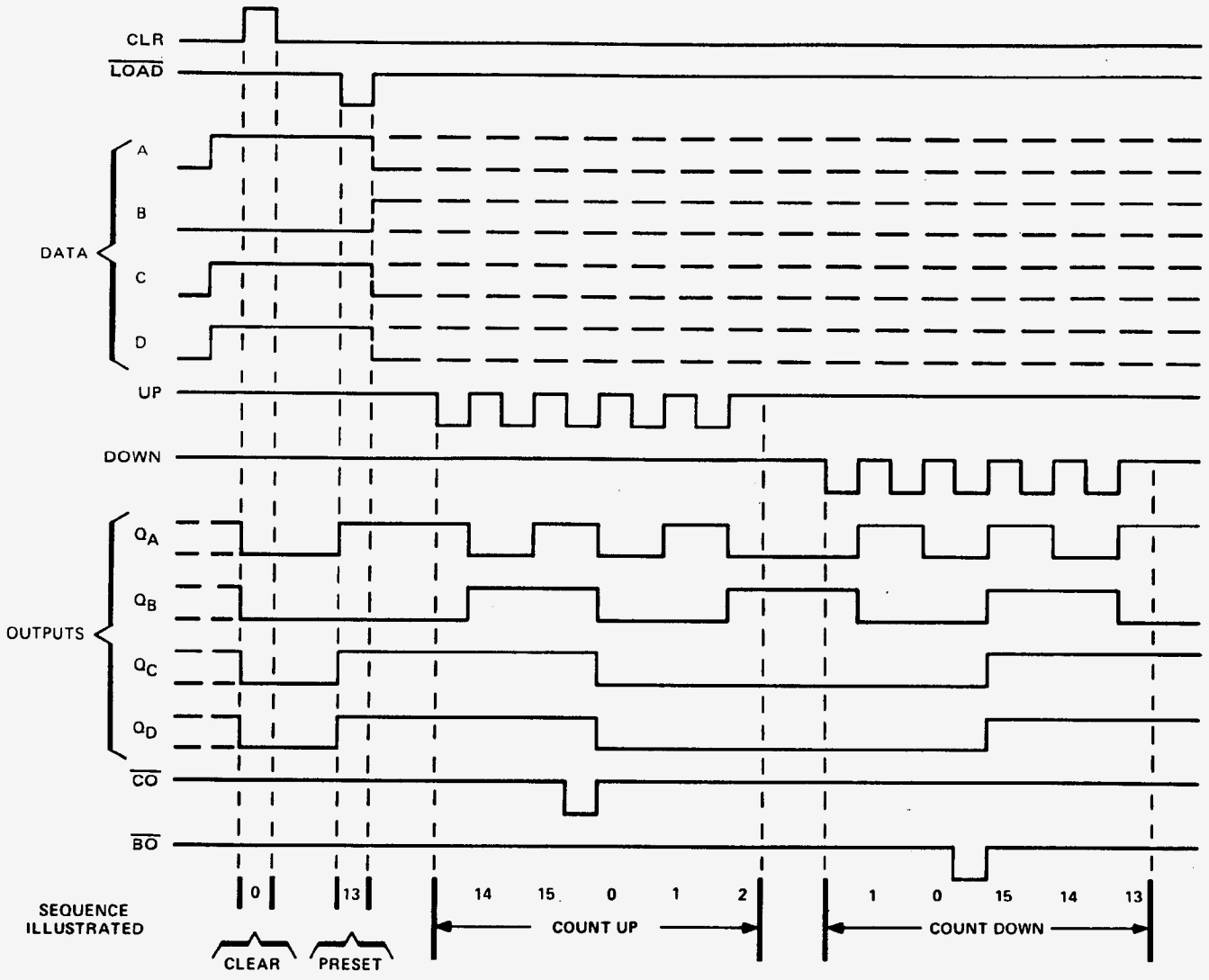
NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

74LS193 BINARY COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

recommended operating conditions

		74LS192 74LS193			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High-level output current			−400	μA
I_{OL}	Low-level output current			8	mA
f_{clock}	Clock frequency	0		25	MHz
t_w	Width of any input pulse	20			ns
t_{su}	Clear inactive-state setup time	15			ns
	Load inactive-state setup time	15			ns
	Data setup time (see Figure 1)	20			ns
t_h	Data hold time	5			ns
T_A	Operating free-air temperature range	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

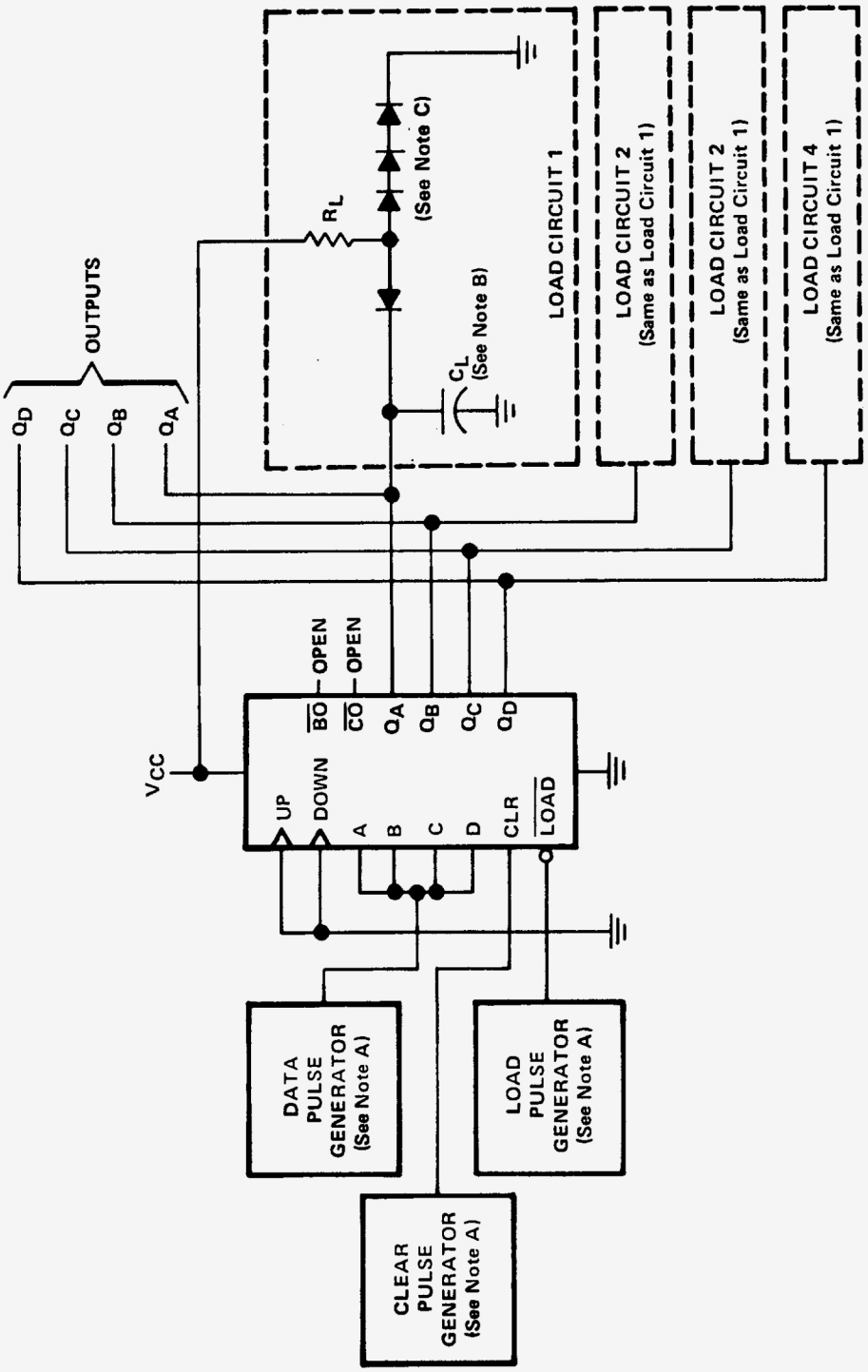
PARAMETER		TEST CONDITIONS†		74LS192 74LS193			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.15	0.4	V
			I_{OL} = 8 mA		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			19	34	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 2	25	32		MHz
t_{PLH}	UP	$\overline{CO}$			17	26	ns
t_{PHL}					18	24	
t_{PLH}	DOWN	$\overline{BO}$			16	24	ns
t_{PHL}					15	24	
t_{PLH}	UP OR DOWN	Q			27	38	ns
t_{PHL}					30	47	
t_{PLH}	$\overline{LOAD}$	Q			24	40	ns
t_{PHL}					25	40	
t_{PHL}	CLR	Q			23	35	ns

PARAMETER MEASUREMENT INFORMATION

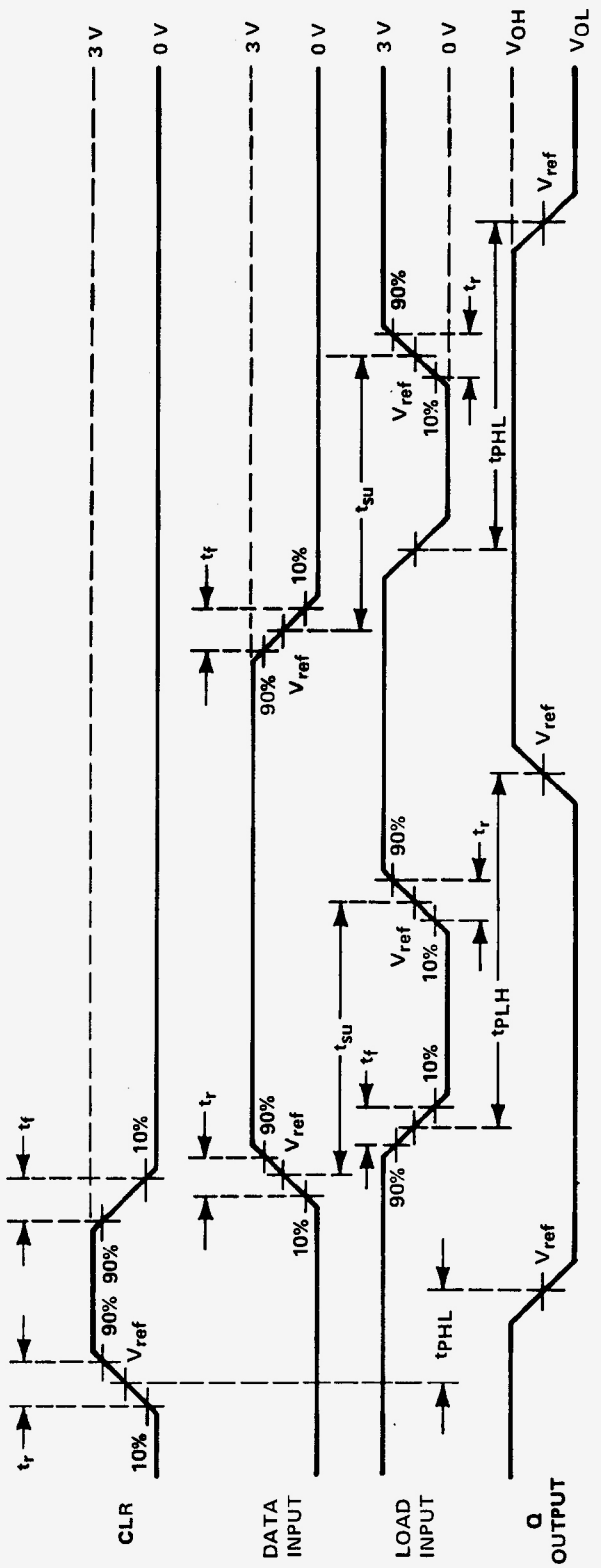


TEST CIRCUIT

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$ and for the data pulse generator PRR $\leq$ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064 or equivalent.
D. t_r and $t_f \leq 7$ ns.
E. V_{ref} is 1.5 V for '192 and '193, 1.3 V for 74LS192,74LS193.

FIGURE 1A – CLEAR, SETUP AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

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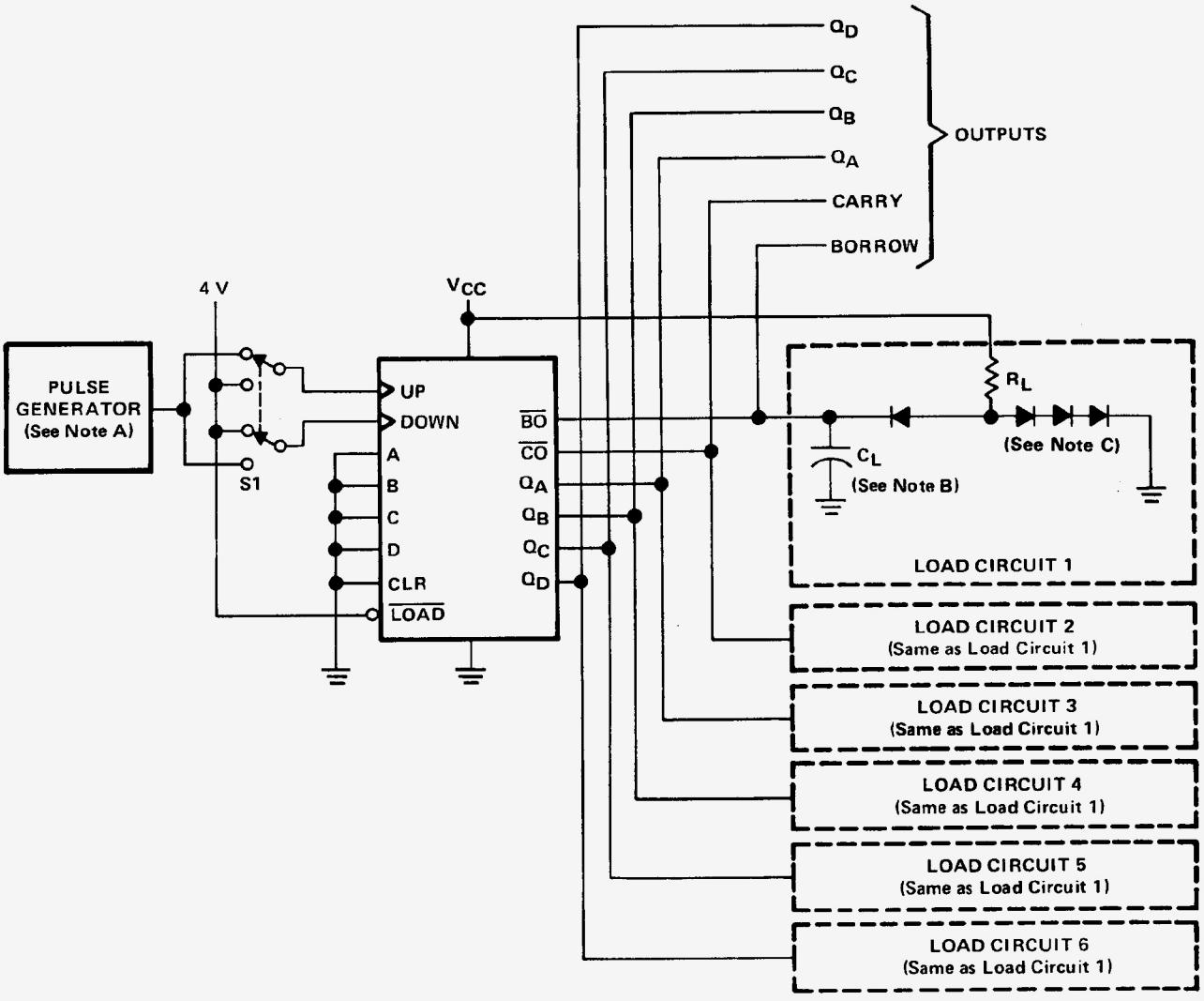
D. t_r and $t_f \leq 7$ ns.
E. V_{ref} is 1.5 V for '192 and '193, 1.3 V for 74LS192,74LS193.

FIGURE 1B – CLEAR, SETUP, AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION

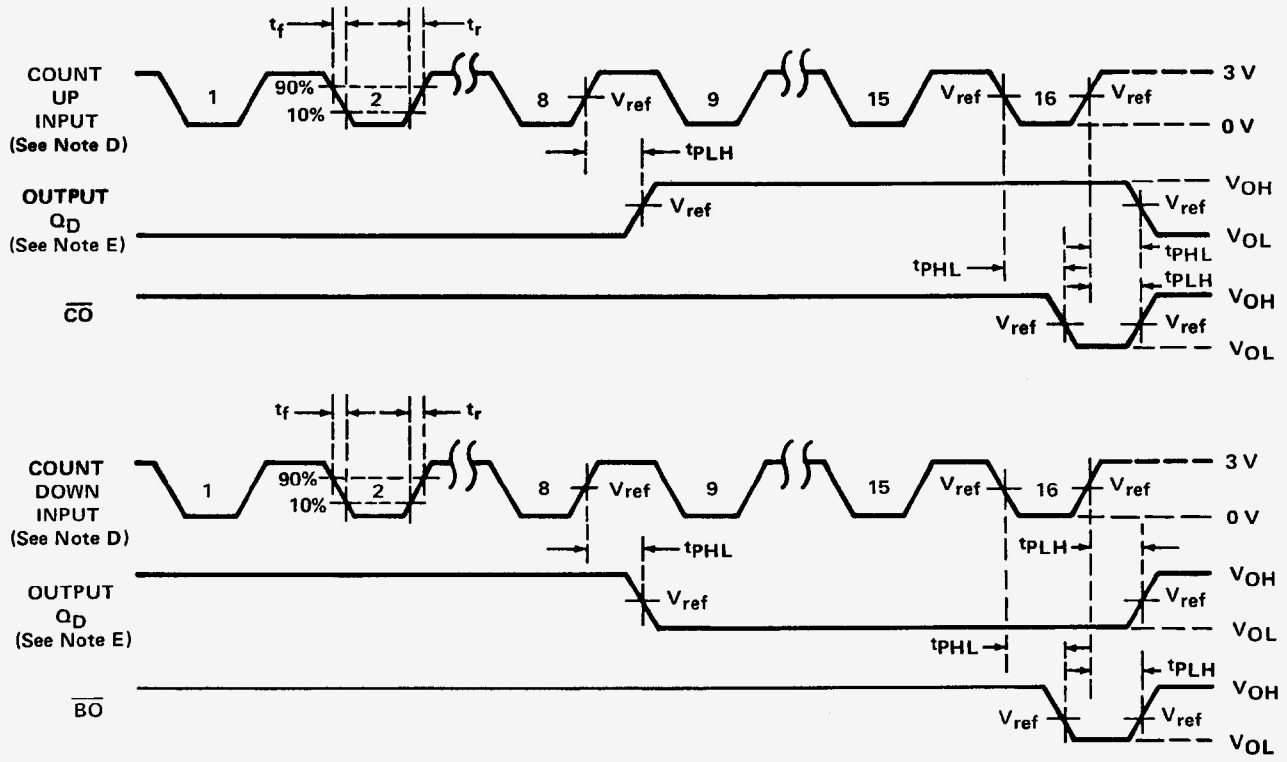


TEST CIRCUIT

NOTES: A. TM pulse gonerators have the foMowkifl chartcteristics: PRR ■ 1 MHz, Zg 50 0, duty cycle - 50%.
B. CI includes probe and jig cep^ciunct.
C. Diodss are 1N3064 or equivatent.
D. Cout-up and dount-down pulse «bown are for 74LS193 Nnary counters. Count cycle for 74LS192 decade counters is 1 through 10.
E. Waveforms for outputs Qa, Qfl, and Qc 斯 omitted to simplify the drawing.
F.tf and tf M 7 ns.
G. .3 V for 74LS192 and 74LS193.

FIGURE 2A — PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

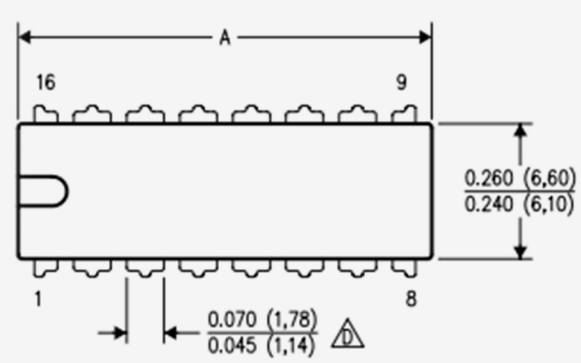


VOLTAGE WAVEFORMS

NOTES:
A. The pulse generators have the following chacactariitict: PRR ■ 1 MHz, Zg ■ 50 Q duty cycle - 50%.
B. CI includes probe and jig capacitance.
C. Diodes are 1N3064 or equivalent.
D. Cout-up and dount-down pulse shown ar* for th«' 74LS193 binary counters. Count cycle for 74LS192 decade counters is 1 through 10.
E. WavBforws for outputs Qa, Qb, and Qc 9t9 omitted to ilmplify the drawing.
F.tr and tf s 7 ns.
G. 1.3 V for 74LS192 and 74LS193.

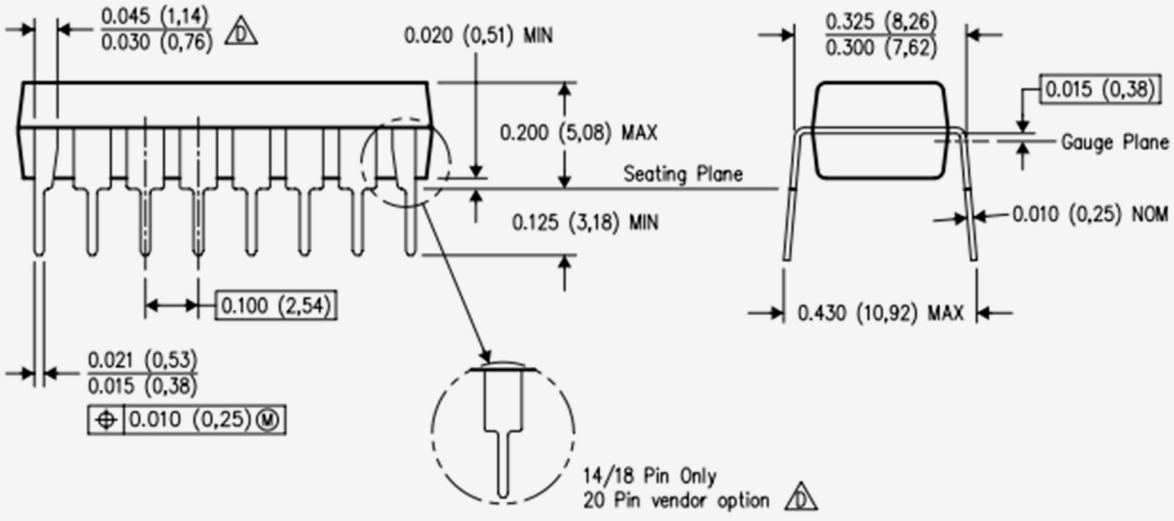
FIGURE 2B – PROPAGATION DELAY TIMES

DIP



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

C



以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA