BROADCOM®

Data Sheet

ACPL-C740

Optically Isolated Sigma-Delta Modulator

Description

The Broadcom® ACPL-C740 is a 1-bit, second-order sigma-delta (Σ-Δ) modulator that converts an analog input signal into a high-speed data stream with galvanic isolation based on optical coupling technology. The ACPL-C740 operates from a 5V power supply with dynamic range of 86 dB with an appropriate digital filter. The differential inputs of ±200 mV (full scale ±320 mV) are ideal for direct connection to shunt resistors or other low-level signal sources in applications, such as motor phase current measurement.

The analog input is continuously sampled by a means of sigma-delta over-sampling using an onboard clock. The signal information is contained in the modulator data, as a density of ones with data rate of 20 MHz, and the data are encoded and transmitted across the isolation boundary where they are recovered and decoded into high-speed data stream of digital ones and zeros. The original signal information can be reconstructed with a digital filter. The serial interface for data and clock has a wide supply range of 3V to 5.5V.

Combined with superior optical-coupling technology, the modulator delivers high noise margins and excellent immunity against isolation-mode transients. With 0.5-mm minimum distance through insulation (DTI), the ACPL-C740 provides reliable reinforced insulation and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives, including devices based on capacitive- or magnetic-coupling with DTI in micro-meter range. Offered in a Stretched SO-8 (SSO-8) package, the isolated ADC delivers the reliability, small size, superior isolation, and over-temperature performance that motor drive designers need to accurately measure current at a much lower price compared to traditional current transducers.

Features

- Superior optical isolation and insulation
- 20-MHz internal clock
- 1-bit, second-order sigma-delta modulator
- 16 bits resolution no missing codes (12 bits ENOB)
- 86 dB SNR
- 1 µV/°C maximum offset drift
- ±1% gain error
- Internal reference voltage
- ±200-mV linear range with single 5V supply (±320 mV full scale)
- 3V to 5.5V wide supply range for digital interface
- –40°C to +110°C operating temperature range
- SSO-8 package
- 25-kV/µs common-mode transient immunity
- Safety and regulatory approval:
  - IEC/EN/DIN EN 60747-5-5: 1414 Vpeak working insulation voltage
  - UL 1577: 5000 V_{rms}/1 min isolation voltage
  - CSA: Component Acceptance Notice #5

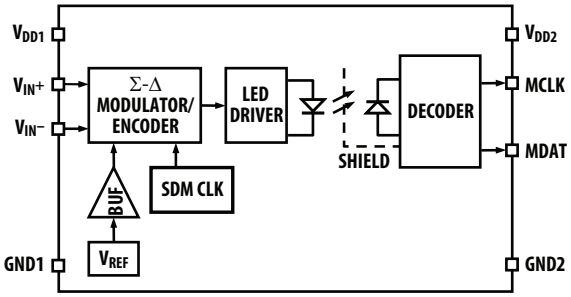
Applications

- Motor phase and rail current sensing
- Power inverter current and voltage sensing
- Industrial process control
- Data acquisition systems
- General-purpose current and voltage sensing
- Traditional current transducer replacements

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Functional Block Diagram

Figure 1: Functional Block Diagram



Pin Configurations and Descriptions

Figure 2: Pin Configuration

Table 1: Pin Descriptions

Pin No.	Symbol	Description
1	V_{DD1}	Supply voltage for signal input side (analog side), relative to GND1.
2	V_{IN+}	Positive analog input, recommended input range ±200 mV.
3	V_{IN-}	Negative analog input, recommended input range ±200 mV (normally connected to GND1).
4	GND1	Supply ground for signal input side.
5	GND2	Supply ground for data/clock output side (digital side).
6	MDAT	Modulator data output.
7	MCLK	Modulator clock output.
8	V_{DD2}	Supply voltage for data output side, relative to GND2.

Ordering Information

The ACPL-C740 is UL recognized with 5000 V_{rms}/1 minute rating per UL 1577.

Table 2: Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-C740	-000E	Stretched SO-8	X		X	80 per tube
	-500E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example:

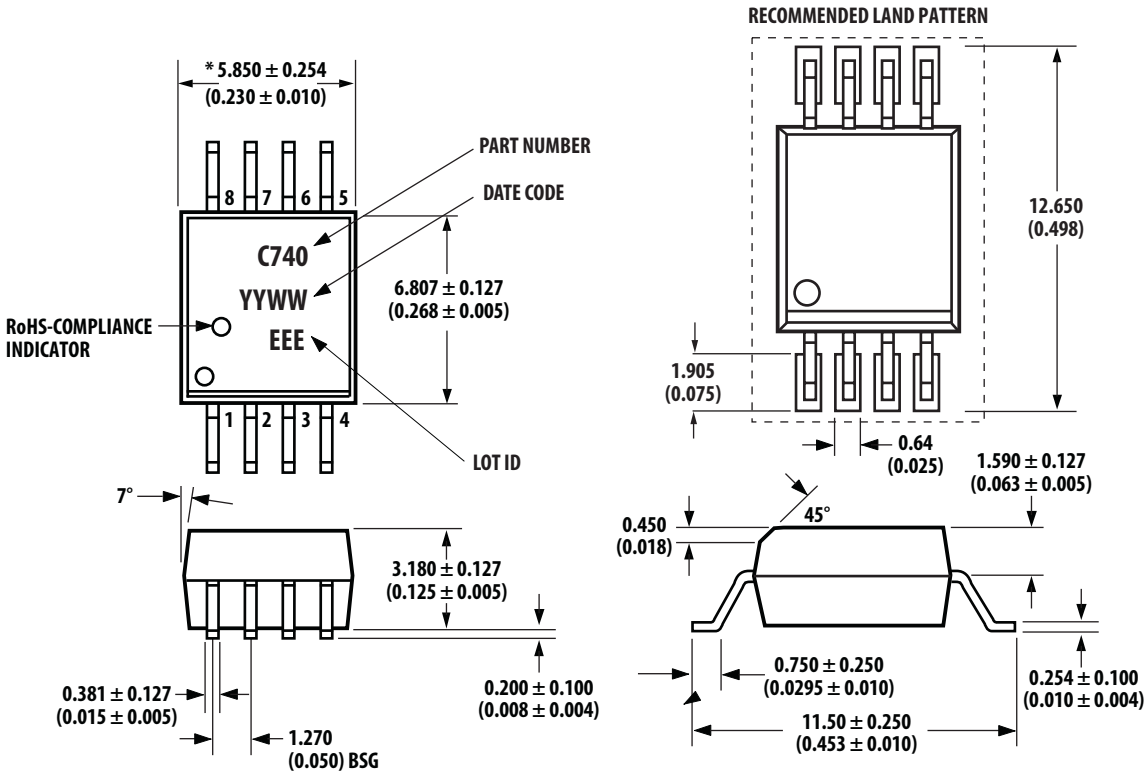
ACPL-C740-500E to order product of Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawings

Stretched SO-8 Package (SSO-8)

Figure 3: Package Dimensions



* Total package width (inclusive of mold flash)
6.100 mm ± 0.250 mm

Dimensions in millimeters and (inches).

Note:
Lead coplanarity = 0.1 mm (0.004 inches).
Floating lead protrusion = 0.25 mm (10 mils) max.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Use non-halide flux.

Regulatory Information

The ACPL-C740 is approved by the following organizations.

Table 3: Regulatory Information

IEC/EN/DIN EN 60747-5-5	Maximum working insulation voltage V_{IORM} = 1414 V_{PEAK}.
UL	Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{rms}/1 min. File E55361.
CSA	Approval under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Table 4: IEC/EN/DIN EN 60747-5-5 Insulation Characteristics[a]

Description	Symbol	Value	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
For rated mains voltage ≤ 150 V_{rms}		I-IV	
For rated mains voltage ≤ 300 V_{rms}		I-IV	
For rated mains voltage ≤ 450 V_{rms}		I-IV	
For rated mains voltage ≤ 600 V_{rms}		I-IV	
For rated mains voltage ≤ 1000 V_{rms}		I-III	
Climatic Classification		55/110/21	°C
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method b V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1s, Partial Discharge < 5 pC	V_{PR}	2652	V_{peak}
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10s, Partial Discharge < 5 pC	V_{PR}	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage, tini = 60 sec)	V_{IOTM}	8000	V_{peak}
Safety-limiting Values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current[b]	$I_{S,INPUT}$	230	mA
Output Power[b]	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	≥ 10^9	Ω

a. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.

b. Safety-limiting parameters are dependent on ambient temperature. The Input Current, $I_{S,INPUT}$, derates linearly above 25°C free-air temperature at a rate of 2.53 mA/°C; the Output Power, $P_{S,OUTPUT}$, derates linearly above 25°C free-air temperature at a rate of 4 mW/°C.

Insulation and Safety Related Specifications

Table 5: Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN EN 60112 (2010-05).
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1).

Absolute Maximum Ratings

Table 6: Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	+125	°C
Ambient Operating Temperature	T_A	–40	+110	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	6.0	V
Steady-State Input Voltage[a, b]	V_{IN+}, $V_{IN–}$	–2	V_{DD1} + 0.5	V
Two-Second Transient Input Voltage[c]	V_{IN+}, $V_{IN–}$	–6	V_{DD1} + 0.5	V
Digital Output Voltages	MCLK, MDAT	–0.5	V_{DD2} + 0.5	V
Lead Solder Temperature	260°C for 10s., 1.6 mm below seating plane			

a. DC voltage of up to –2V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.

b. Absolute maximum DC current on the inputs = 100 mA, no latch-up or device damage occurs.

c. Transient voltage of 2 seconds up to –6V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.

Recommended Operating Conditions

Table 7: Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	+110	°C
V_{DD1} Supply Voltage	V_{DD1}	4.5	5.5	V
V_{DD2} Supply Voltage	V_{DD2}	3	5.5	V
Analog Input Voltage[a]	V_{IN+}, $V_{IN–}$	–200	+200	mV

a. Full scale signal input range ±320 mV.

Electrical Specifications

Unless otherwise noted, T_A = –40°C to +110°C, V_{DD1} = 4.5V to 5.5V, V_{DD2} = 3V to 5.5V, V_{IN+} = –200 mV to +200 mV, and $V_{IN–}$ = 0V (single-ended connection); tested with $Sinc^3$ filter, 256 decimation ratio, with anti aliasing filter (AAF) as per Figure 19.

Table 8: Electrical Specifications

Parameter	Symbol	Min.	Typ.[a]	Max.	Units	Test Conditions	Figure	Notes
Static Characteristics								
Resolution		16	—	—	Bits	Decimation filter output set to 16 bits.		
Integral Nonlinearity	INL	–16	±5	16	LSB	T_A = –40°C to +110°C; see Definitions.		
Differential Nonlinearity	DNL	–0.9	—	0.9	LSB	No missing codes, guaranteed by design; see Definitions.		
Offset Error	V_{OS}	0	0.8	2	mV	T_A = –40°C to +110°C; see Definitions.	5	
Offset Drift vs. Temperature	TCV_{OS}	—	0.3	1.0	µV/°C	V_{DD1} = 5V, R_{sense} = 0Ω.		
Offset Drift vs. V_{DD1}		—	100	—	µV/V			
Internal Reference Voltage	V_{REF}		320	—	mV			

Table 8: Electrical Specifications (Continued)

Parameter	Symbol	Min.	Typ.[a]	Max.	Units	Test Conditions	Figure	Notes
Reference Voltage Tolerance	G_E	–1	—	1	%	T_A = 25°C, V_{IN+} = –320 mV to +320 mV; see Definitions.		
		–2	—	2	%	T_A = –40°C to +110°C, V_{IN+} = –320 mV to +320 mV.	6	
V_{REF} Drift vs. Temperature	TCG_E	—	40	—	ppm/°C			
V_{REF} Drift vs. V_{DD1}		—	0.1	—	mV/V			b
Analog Inputs								
Full-Scale Differential Voltage Input Range	FSR	—	±320	—	mV	$V_{IN} = V_{IN+} – V_{IN–}$.		c
Input Bias Current	I_{INA}	—	30	—	nA	V_{DD1} = 5V, V_{DD2} = 5V, V_{IN+} = 0V.	7	d
Input Resistance	R_{IN}	—	12.5	—	kΩ	Across V_{IN+} or $V_{IN–}$ to GND1.		d
Input Capacitance	C_{INA}	—	8	—	pF	Across V_{IN+} or $V_{IN–}$ to GND1.		
Dynamic Characteristics						V_{IN+} = 400 mVpp, 1-kHz sine wave.		
Signal-to-Noise Ratio	SNR	75	86	—	dB	T_A = –40°C to +110°C; see Definitions.	8	
Signal-to-(Noise + Distortion) Ratio	SNDR	65	75	—	dB	T_A = –40°C to +110°C; see Definitions.	9	
Effective Number of Bits	ENOB	—	12	—	Bits	See Definitions.		
Isolation Transient Immunity	CMR	25	—	—	kV/µs	V_{CM} = 1 kV; see Definitions.		
Digital Outputs								
Output High Voltage	V_{OH}	V_{DD2} – 0.4	V_{DD2} – 0.2	—	V	I_{OUT} = –4 mA.		
Output Low Voltage	V_{OL}	—	0.2	0.4	V	I_{OUT} = +4 mA.		
Power Supply								
V_{DD1} Supply Current	I_{DD1}	—	10	14	mA	V_{IN+} = –320 mV to +320 mV.	10	
V_{DD2} Supply Current	I_{DD2}	—	9	12	mA	V_{DD2} = 5V supply.	11	
		—	7.5	9.5	mA	V_{DD2} = 3.3V supply.	12	

a. All Typical values are at T_A = 25°C, V_{DD1} = 5V, V_{DD2} = 5V.

b. V_{REF} Drift vs. V_{DD1} can be expressed as 0.03%/V with reference to V_{REF}.

c. Beyond the full-scale input range the data output is either all zeros or all ones.

d. Because of the switched-capacitor nature of the isolated modulator, time averaged values are shown.

Timing Specifications

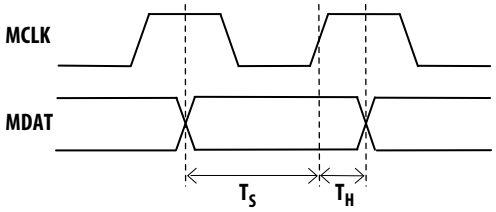
Unless otherwise noted, T_A = –40°C to +110°C, V_{DD1} = 4.5V to 5.5V, V_{DD2} = 3V to 5.5V.

Table 9: Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Notes	Figure
Modulator Clock Output Frequency	f_{MCLK}	18	20	22	MHz	C_L = 15 pF	a	13
		19	20	21	MHz	C_L = 15 pF,, T_A =25°C	a	13
Modulator Clock Rising Time	t_r	—	5	—	ns	C_L = 15 pf		
Modulator Clock Falling Time	t_f	—	5	—	ns	C_L = 15 pf		
Data Setup Time after MCLK Rising Edge	t_S	15	32	—	ns	C_L = 15 pF		4
Data Hold Time after MCLK Rising Edge	t_H	5	13	—	ns	C_L = 15 pF		4

a. f_{MCLK} specification is based on average value which is equal to SDM CLK.

Figure 4: Data Timing



Package Characteristics

Table 10: Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions/Notes	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{rms}	RH ≤ 50%, t = 1 min; T_A = 25°C	a, b
Input-Output Resistance	R_{I-O}	—	$>10^{12}$	—	Ω	V_{I-O} = 500 Vdc	c
Input-Output Capacitance	C_{I-O}	—	0.5	—	pF	f = 1 MHz	c

a. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.

b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table and your equipment level safety specification.

c. This is a two-terminal measurement: pins 1–4 are shorted together and pins 5–8 are shorted together.

Typical Performance Plots

Unless otherwise noted, T_A = 25°C, V_{DD1} = 5V, V_{DD2} = 5V, V_{IN+} = –200 mV to +200 mV, and $V_{IN–}$ = 0V, with Sinc3 filter, 256 decimation ratio.

Figure 5: Offset Change vs. Temperature

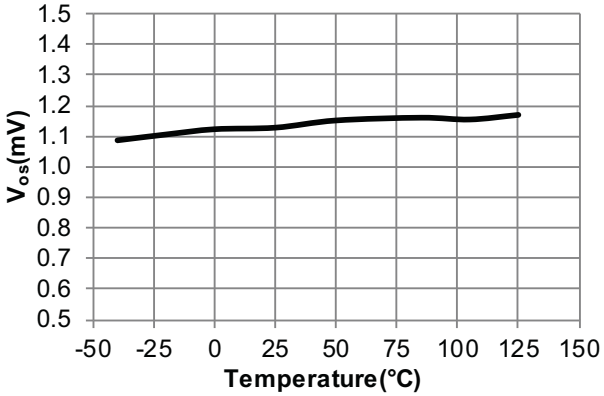


Figure 6: V_{REF} Change vs. Temperature

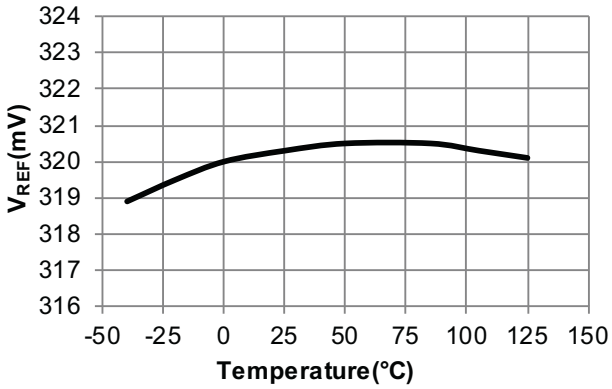


Figure 7: Input Current vs. Input Voltage

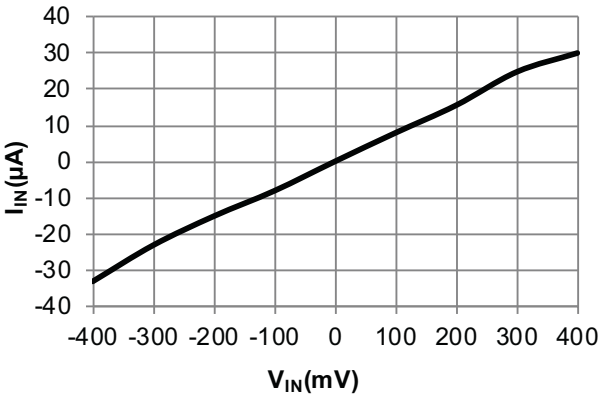


Figure 8: SNR vs. Temperature

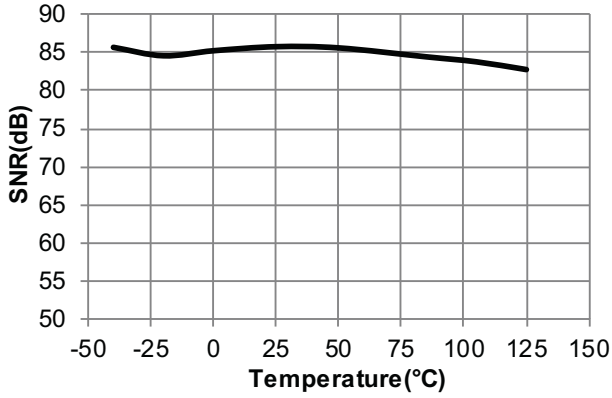


Figure 9: SNDR vs. Temperature

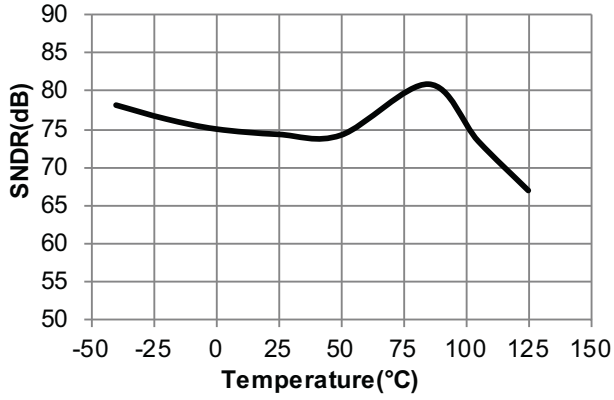


Figure 10: I_{DD1} vs. V_{IN} DC Input at Various Temperatures

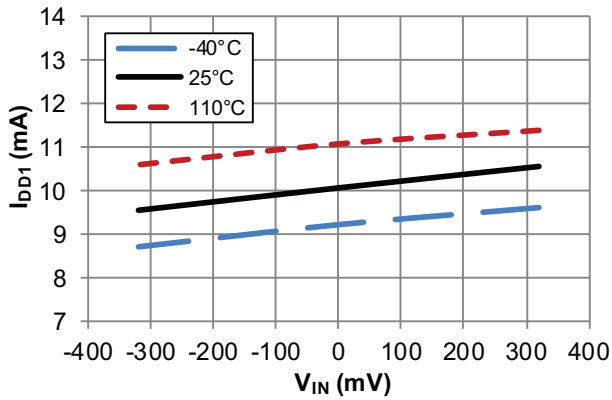


Figure 11: I_{DD2} (V_{DD2} = 5V) vs. V_{IN} DC Input at Various Temperatures

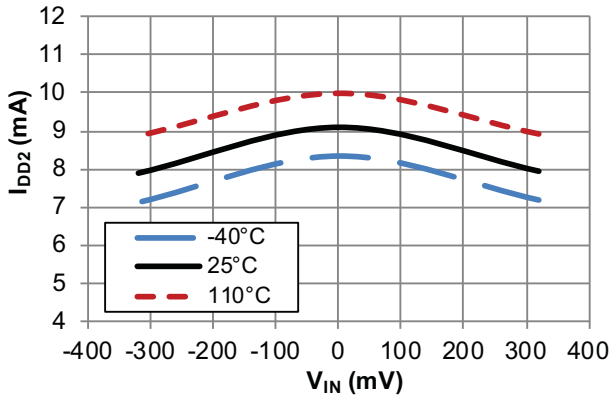


Figure 12: I_{DD2} (V_{DD2} = 3.3V) vs. V_{IN} DC Input at Various Temperatures

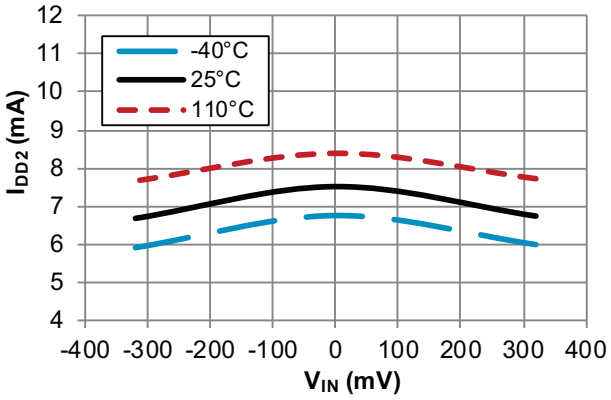
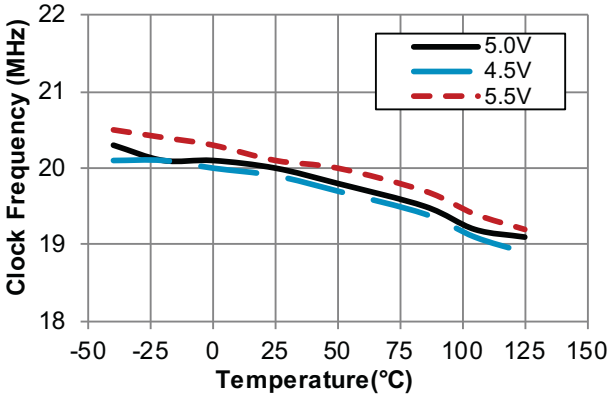


Figure 13: Clock Frequency vs. Temperature for Various V_{DD1}



Definitions

Integral Nonlinearity (INL)

INL is the maximum deviation of a transfer curve from a straight line passing through the endpoints of the ADC transfer function, with offset and gain errors adjusted out.

Differential Nonlinearity (DNL)

DNL is the deviation of an actual code width from the ideal value of 1 LSB between any two adjacent codes in the ADC transfer curve. DNL is a critical specification in closed-loop applications. A DNL error of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

Offset error is the deviation of the actual input voltage corresponding to the mid-scale code (32,768 for a 16-bit system with an unsigned decimation filter) from 0V. Offset error can be corrected by software or hardware.

Gain Error (Full-Scale Error)

Gain error includes positive full-scale gain error and negative full-scale gain error. Positive full-scale gain error is the deviation of the actual input voltage corresponding to positive full-scale code (65,535 for a 16-bit system) from the ideal differential input voltage ($V_{IN+} – V_{IN–}$ = +320 mV), with offset error adjusted out. Negative full-scale gain error is the deviation of the actual input voltage corresponding to negative full-scale code (0 for a 16-bit system) from the ideal differential input voltage ($V_{IN+} – V_{IN–}$ = –320 mV), with offset error adjusted out. Gain error includes reference error. Gain error can be corrected by software or hardware.

Signal-to-Noise Ratio (SNR)

The SNR is the measured ratio of AC signal power to noise power below half of the sampling frequency. The noise power excludes harmonic signals and DC.

Signal-to-(Noise + Distortion) Ratio (SNDR)

The SNDR is the measured ratio of AC signal power to noise plus distortion power at the output of the ADC. The signal power is the rms amplitude of the fundamental input signal. Noise plus distortion power is the rms sum of all non-fundamental signals up to half the sampling frequency (excluding DC).

Effective Number of Bits (ENOB)

The ENOB determines the effective resolution of an ADC, expressed in bits, defined by ENOB = (SNDR – 1.76) / 6.02.

Isolation Transient Immunity (CMR)

The isolation transient immunity (also known as Common-Mode Rejection or CMR) specifies the minimum rate-of-rise/fall of a common-mode signal applied across the isolation boundary beyond which the modulator clock or data is corrupted. Data and clock output are measured within specifications after 1 µs of common mode transient occurs.

Product Overview

Description

The ACPL-C740 isolated sigma-delta (Σ-Δ) modulator converts an analog input signal into a high-speed (20 MHz typical) single-bit data stream by means of a sigma-delta over-sampling modulator. The time average of the modulator data is directly proportional to the input signal voltage. The modulator uses internal clock of 20 MHz. The modulator data is encoded and transmitted across the isolation boundary where it is recovered and decoded into high-speed data stream of digital ones and zeros. The original signal information is represented by the density of ones in the data output.

The other main function of the modulator (optocoupler) is to provide galvanic isolation between the analog signal input and the digital data output. It provides high noise margins and excellent immunity against isolation-mode transients that allows direct measurement of low-level signals in highly noisy environments; for example, measurement of motor phase currents in power inverters.

With 0.5-mm minimum DTI, the ACPL-C740 provides reliable double protection and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives including devices based on capacitive- or magnetic-coupling with DTI in micro-meter range. Offered in an SSO-8 package, the isolated ADC delivers the reliability, small size, superior isolation and over-temperature performance, motor drive designers must accurately measure current at much lower price compared to traditional current transducers.

Analog Input

The differential analog inputs of the ACPL-C740 are implemented with a fully differential, switched-capacitor circuit. The ACPL-C740 accepts a signal of ±200 mV (full scale ±320 mV), which is ideal for direct connection to shunt-based current sensing or other low-level signal sources applications, such as motor phase current measurement. An internal voltage reference determines the full-scale analog input range of the modulator (±320 mV); an input range of ±200 mV is recommended to achieve optimal performance. Users are able to use higher input ranges, for example ±250 mV, as long as within full-scale range, for purpose of over-current or overload detection. Figure 14 shows the simplified equivalent circuit of the analog input.

In the typical application circuit (Figure 17), the ACPL-C740 is connected in a single-ended input mode. Given the fully differential input structure, a differential input connection method (balanced input mode as shown in Figure 15) is recommended to achieve better performance. The input currents created by the switching actions on both of the pins are balanced on the filter resistors and cancelled out each other. Any noise induced on one pin will be coupled to the other pin by the capacitor C and creates only common mode noise which is rejected by the device. Typical values for Ra (= Rb) and C are 22Ω and 10 nF, respectively.

Figure 14: Analog Input Equivalent Circuit

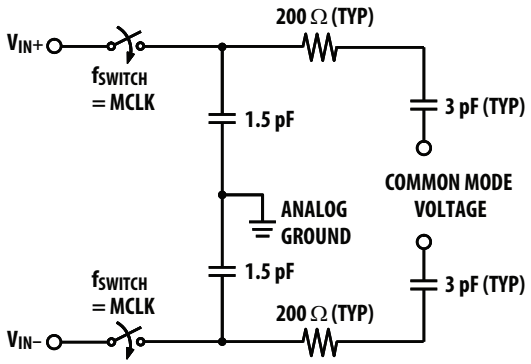
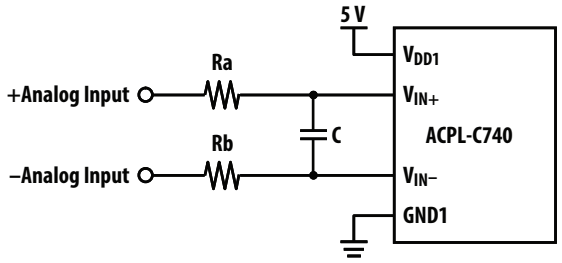


Figure 15: Simplified Differential Input Connection Diagram



Latch-up Consideration

Latch-up risk of CMOS devices needs careful consideration, especially in applications with direct connection to signal source that is subject to frequent transient noise. The analog input structure of the ACPL-C740 is designed to be resilient to transients and surges, which are often encountered in highly noisy application environments, such as motor drive and other power inverter systems. Other situations could cause transient voltages to the inputs include short circuit and overload conditions. The ACPL-C740 is tested with DC voltage of up to –2V and 2-second transient voltage of up to –6V to the analog inputs with no latch-up or damage to the device.

Modulator Data Output

Input signal information is contained in the modulator output data stream, represented by the density of ones and zeros. The density of ones is proportional to the input signal voltage, as shown in Figure 16. A differential input signal of 0V ideally produces a data stream of ones and zeros in equal densities. A differential input of –200 mV corresponds to 18.75-percent density of ones, and a differential input of +200 mV is represented by 81.25-percent density of ones in the data stream. A differential input of +320 mV or higher results in ideally all ones in the data stream, while input of –320 mV or lower will result in all zeros ideally. Table 11 shows this relationship.

Figure 16: Modulator Output vs. Analog Input

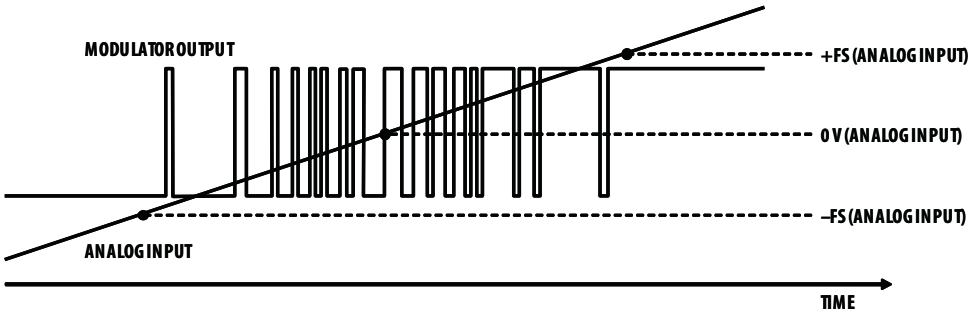


Table 11: Input Voltage with Ideal Corresponding Density of 1s at Modulator Data Output, and ADC Code

Analog Input	Voltage Input	Density of 1s	Density of 0s	ADC Code (16-bit Unsigned Decimation)
+Full-Scale	+320 mV	100%	0%	65,535
+Recommended Input Range	+200 mV	81.25%	18.75%	53,248
Zero	0 mV	50%	50%	32,768
–Recommended Input Range	–200 mV	18.75%	81.25%	12,288
–Full-Scale	–320 mV	0%	100%	0

NOTE:

1. With bipolar offset binary coding scheme, the digital code begins with digital 0 at –FS input and increases proportionally to the analog input until the full-scale code is reached at the +FS input. The zero crossing occurs at the mid-scale input.
2. Ideal density of 1s at modulator data output can be calculated with V_{IN}/640 mV + 50%; similarly, the ADC code can be calculated with (V_{IN}/640 mV) × 65,536 + 32,768, assuming a 16-bit unsigned decimation filter.

Digital Filter

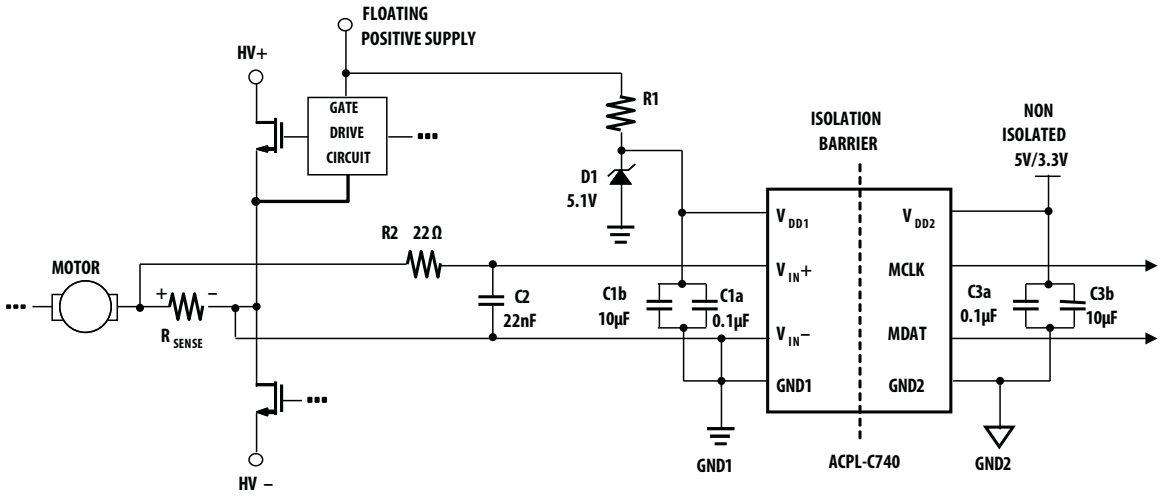
A digital filter converts the single-bit data stream from the modulator into a multi-bit output word similar to the digital output of a conventional A/D converter. With this conversion, the data rate of the word output is also reduced (decimation). A $Sinc^3$ filter is recommended to work together with the ACPL-C740. With 256 decimation ratio and 16-bit word settings, the output data rate is 78 kHz (= 20 MHz/256). This filter can be implemented in an ASIC, an FPGA, or a DSP. Some of the ADC codes with corresponding input voltages are shown in Table 11.

Application Information

Typical Application Circuit

Figure 17 shows a typical application circuit for motor control phase current sensing. By choosing the appropriate shunt resistance, a wide range of current can be monitored, from less than 1A to more than 100A.

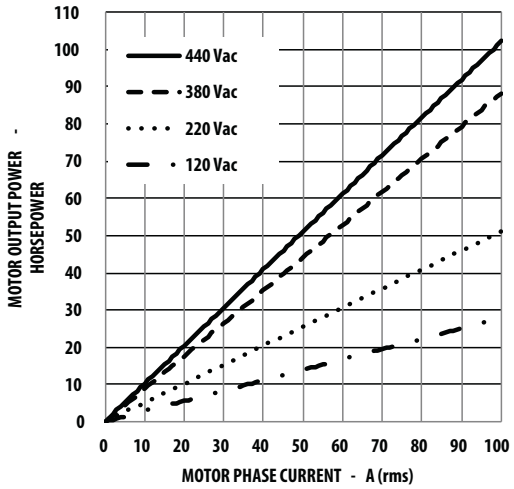
Figure 17: Typical Application Circuit in Motor Phase Current Setting



Shunt Resistors

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the shunt is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller shunt resistances decrease power dissipation, while larger shunt resistances can improve circuit accuracy by utilizing the full input range of the isolated modulator.

Figure 18: Motor Output Horsepower vs. Motor Phase Current and Supply



The first step in selecting a shunt is determining how much current the shunt will be sensing. The graph in Figure 18 shows the RMS current in each phase of a three-phase induction motor as a function of average motor output power (in horsepower, hp) and motor drive supply voltage. The maximum value of the shunt is determined by the current being measured and the maximum recommended input voltage of the isolated modulator. The maximum shunt resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the shunt should see during normal operation. For example, if a motor will have a maximum RMS current of 35 A_{rms} and can experience up to 50-percent overloads during normal operation, the peak current is 75A (= 35 × 1.414 × 1.5). Assuming a maximum input voltage of 200 mV without overload condition, the maximum value of shunt resistance in this case would be about 4 mΩ. Under overload conditions, the maximum input voltage will then be 300 mV (75A × 4 mΩ), well within the ±320 mV FSR.

The maximum average power dissipation in the shunt can also be easily calculated by multiplying the shunt resistance times the square of the maximum RMS current, which is about 4.9W in the previous example.

If the power dissipation in the shunt is too high, the resistance of the shunt can be decreased below the maximum value to decrease power dissipation. The minimum value of the shunt is limited by precision and accuracy requirements of the design. As the shunt value is reduced, the output voltage across the shunt is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the shunt will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient (tempco) of the shunt can introduce nonlinearity due to the signal dependent temperature rise of the shunt. The effect increases as the shunt-to-ambient thermal resistance increases. This effect can be minimized either by reducing the thermal resistance of the shunt or by using a shunt with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the shunt on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

For a two-terminal shunt, as the value of shunt resistance decreases, the resistance of the leads becomes a significant percentage of the total shunt resistance. This has two primary effects on shunt accuracy. First, the effective resistance of the shunt can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the lead during assembly (these issues will be discussed in more detail shortly). Secondly, the leads are typically made from a material such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco for the shunt overall. Both of these effects are eliminated when a four-terminal shunt is used. A four-terminal shunt has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage.

Several two-terminal and four-terminal surface mount type shunt resistors from various suppliers suitable for sensing currents in motor drives up to 70 A_{rms} (71 hp or 53 kW) are shown as examples in Table 12.

Table 12: Example of Two-Terminal and Four Terminal Shunt Resistors for Motor Drives up to 70 A_{rms}

Manufacturer	Sunt Resistor Part Number	Shunt Resistor Type	Shunt Resistance	Maximum RMS Current	Motor Power Range 120 Vac to 440 Vac	
			mΩ	A	hp	kW
KOA	CSR series	Four-terminal	20	7	1.8–6.7	1.4–5
TT Electronics	LRMA series	Two-terminal				
Vishay	WSL3637	Four-terminal	8	17	4–17	3–13
Isabellenhütte	SMS R008	Two-terminal				
Vishay	WSLP4026	Four-terminal	4	35	9–36	7–27
KOA	SLN5 series	Two-terminal				
Vishay	WSLP2818	Two-terminal	2	70	19–72	14–54

When laying out a PC board for the shunts, a couple of points should be kept in mind. The Kelvin connections to the shunt should be brought together under the body of the shunt and then run very close to each other to the input of the isolated modulator; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal. If the shunt is not located on the same PC board as the isolated modulator circuit, a tightly twisted pair of wires can accomplish the same thing.

Also, multiple layers of the PC board can be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the shunt to help distribute the current between the layers of the PC board. The PC board should use 2-oz. or 4-oz. copper for the layers, resulting in a current carrying capacity in excess of 20A. Making the current carrying traces on the PC board fairly large can also improve the shunt's power dissipation capability by acting as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended.

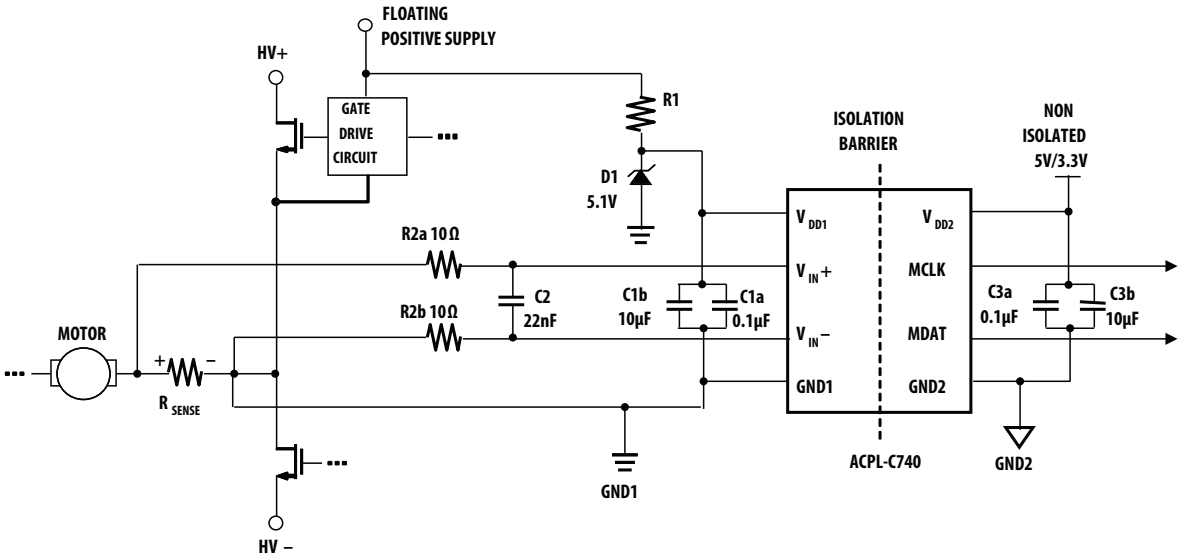
Shunt Connections

The recommended method for connecting the isolated modulator to the shunt resistor is shown in Figure 17. V_{IN+} of the ACPL-C740 is connected to the positive terminal of the shunt resistor, while V_{IN-} is shorted to GND1, with the power-supply return path functioning as the sense line to the negative terminal of the current shunt. This allows a single pair of wires or PC board traces to connect the isolated modulator circuit to the shunt resistor. By referencing the input circuit to the negative side of the sense resistor, any load current induced noise transients on the shunt are seen as a common-mode signal and will not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current shunt.

If the same power supply is used both for the gate drive circuit and for the current sensing circuit, it is very important that the connection from GND1 of the isolated modulator to the sense resistor be the only return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the isolated modulator circuit and the gate drive circuit should be the positive power supply line.

In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting V_{IN+} and $_{VIN-}$ directly across the shunt resistor with two conductors, and connecting GND1 to the shunt resistor with a third conductor for the power-supply return path, as shown in Figure 19. The input currents induced by the common-mode of the fully differential amplifier on both of the pins are balanced on the filter resistors, R2a and R2b, and cancelled out each other. Any noise induced on one pin will be coupled to the other pin by the capacitor C2 and creates only common mode noise which is rejected by the device. When connected this way, both input pins should be bypassed. To minimize electromagnetic interference of the sense signal, all of the conductors (whether two or three are used) connecting the isolated modulator to the sense resistor should be either twisted pair wire or closely spaced traces on a PC board.

Figure 19: Schematic for Three Conductor Shunt Connection

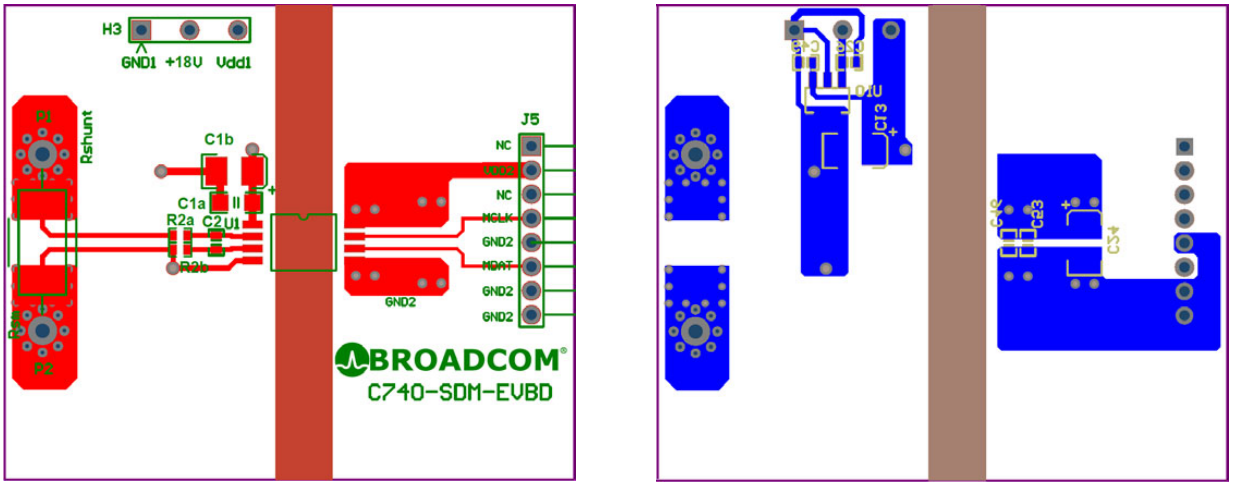


The resistors R2 in Figure 17 or R2a and R2b in Figure 19 which are in series with the input leads form a low pass anti-aliasing filter with the input bypass capacitor C2. These resistors perform another important function as well; to dampen any ringing which might present in the circuit formed by the shunt, the input bypass capacitor, and the inductance of wires or traces connecting the two. Undamped ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device.

PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, and so on. Figure 20 shows an example of PCB layout where the VDD1 is supplied from the 18V floating power supply of gate drive circuitry through LDO voltage regulator. In addition, the layout of the PCB can also affect the isolation transient immunity (CMR) of the isolated modulator, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the isolated modulator.

Figure 20: An Example of Good PCB Layout for ACPL-C740



Top Layer Bottom Layer

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