

**FEATURES**

**44 V supply maximum ratings**  
**V<sub>SS</sub> to V<sub>DD</sub> analog signal range**  
**Low on resistance: <35 Ω**  
**Ultralow power dissipation: < 35 μW**  
**Fast transition time: 160 ns maximum**  
**Break-before-make switching action**  
**Plug-in replacement for DG419**

**APPLICATIONS**

**Precision test equipment**  
**Precision instrumentation**  
**Battery-powered systems**  
**Sample hold systems**

**GENERAL DESCRIPTION**

The ADG419 is a monolithic CMOS SPDT switch. This switch is designed on an enhanced LC<sup>2</sup>MOS process that provides low power dissipation yet gives high switching speed, low on resistance, and low leakage currents.

The on resistance profile of the ADG419 is very flat over the full analog input range, ensuring excellent linearity and low distortion. The part also exhibits high switching speed and high signal bandwidth. CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

Each switch of the ADG419 conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. The ADG419 exhibits break-before-make switching action.

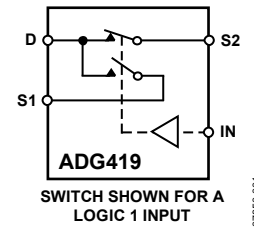
**FUNCTIONAL BLOCK DIAGRAM**

Figure 1.

**PRODUCT HIGHLIGHTS**

1. Extended Signal Range.  
The ADG419 is fabricated on an enhanced LC<sup>2</sup>MOS process, giving an increased signal range that extends to the supply rails.
2. Ultralow Power Dissipation.
3. Low R<sub>ON</sub>.
4. Single-Supply Operation.  
For applications where the analog signal is unipolar, the ADG419 can be operated from a single rail power supply. The part is fully specified with a single 12 V power supply and remains functional with single supplies as low as 5 V.

**Rev. B**

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# ADG419\* Product Page Quick Links

Last Content Update: 08/30/2016

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View a parametric search of comparable parts

## [Evaluation Kits](#)

- Evaluation Board for 8 lead MSOP Devices in the Switch/Mux Portfolio

## [Documentation](#)

### **Data Sheet**

- ADG419-DSCC: Military Data Sheet
- ADG419-EP: Enhanced Product Data Sheet
- ADG419: LC<sup>2</sup>MOS Precision Mini-DIP Analog Switch Data Sheet

### **User Guides**

- UG-893: Evaluating the 8-Lead MSOP Devices in the Switch/Mux Portfolio

## [Reference Materials](#)

### **Product Selection Guide**

- Switches and Multiplexers Product Selection Guide

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- CMOS Switches Offer High Performance in Low Power, Wideband Applications
- Data-acquisition system uses fault protection
- Enhanced Multiplexing for MEMS Optical Cross Connects
- Temperature monitor measures three thermal zones

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- ADG419 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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**REVISION HISTORY**

**8/09—Rev. B to Rev. C**

Updated Format.....	Universal
Changes to Table 1.....	3
Changes to Table 2.....	4
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	13

# SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $V_L = 5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter <sup>1</sup>	B Version			T Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C	-40°C to +125°C	+25°C	-55°C to +125°C		
ANALOG SWITCH							
Analog Signal Range			$V_{SS}$ to $V_{DD}$		$V_{SS}$ to $V_{DD}$		
$R_{ON}$	25 35	45	45	25 35	45	$\Omega$ typ $\Omega$ max	$V_D = \pm 12.5\text{ V}$ , $I_S = -10\text{ mA}$ $V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
LEAKAGE CURRENTS							
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			$\pm 0.1$		nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}$ , $V_S = \mp 15.5\text{ V}$ ; see Figure 12
Drain Off Leakage, $I_D$ (Off)	$\pm 0.25$ $\pm 0.1$	$\pm 5$	$\pm 15$	$\pm 0.25$ $\pm 0.1$	$\pm 15$	nA max nA typ	$V_D = \pm 15.5\text{ V}$ , $V_S = \mp 15.5\text{ V}$ ; see Figure 12
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.75$ $\pm 0.4$ $\pm 0.75$	$\pm 5$	$\pm 30$	$\pm 0.75$ $\pm 0.4$ $\pm 0.75$	$\pm 30$	nA max nA typ nA max	$V_S = V_D = \pm 15.5\text{ V}$ ; see Figure 13
DIGITAL INPUTS							
Input High Voltage, $V_{INH}$		2.4	2.4		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	0.8		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$		$\pm 0.005$ $\pm 0.5$	$\pm 0.005$ $\pm 0.5$		$\pm 0.005$ $\pm 0.5$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
DYNAMIC CHARACTERISTICS <sup>2</sup>							
$t_{TRANSITION}$	160	200	200	145	200	ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = \pm 10\text{ V}$ , $V_{S2} = \mp 10\text{ V}$ ; see Figure 14
Break-Before-Make Time Delay, $t_D$	30			30		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = V_{S2} = \pm 10\text{ V}$ ; see Figure 15
Off Isolation	5			5		ns min	
Channel-to-Channel Crosstalk	80			80		dB typ	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ; see Figure 16
$C_S$ (Off)	90			70		dB typ	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ; see Figure 17
$C_S$ (On)	6			6		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	55			55		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS							
$I_{DD}$	0.0001			0.0001		$\mu\text{A}$ typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ $V_{IN} = 0\text{ V}$ or $5\text{ V}$
	1	2.5	2.5	1	2.5	$\mu\text{A}$ max	
$I_{SS}$	0.0001			0.0001		$\mu\text{A}$ typ	
	1	2.5	2.5	1	2.5	$\mu\text{A}$ max	
$I_L$	0.0001			0.0001		$\mu\text{A}$ typ	$V_L = 5.5\text{ V}$
	1	2.5	2.5	1	2.5	$\mu\text{A}$ max	

<sup>1</sup> Temperature ranges are as follows: B Version:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ ; T Version:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

<sup>2</sup> Guaranteed by design, not subject to production test.

# ADG419

## SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $V_L = 5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 2.

Parameter <sup>1</sup>	B Version			T Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C	-40°C to +125°C	+25°C	-55°C to +125°C		
<b>ANALOG SWITCH</b>							
Analogue Signal Range			0 to $V_{DD}$		0 to $V_{DD}$	V	
$R_{ON}$	40	60	70	40	70	$\Omega$ typ $\Omega$ max	$V_D = 3\text{ V}, 8.5\text{ V}, I_S = -10\text{ mA}$ $V_{DD} = 10.8\text{ V}$
<b>LEAKAGE CURRENT</b>							
Source OFF Leakage, $I_S$ (Off)	$\pm 0.1$			$\pm 0.1$		nA typ	$V_{DD} = 13.2\text{ V}$ $V_D = 12.2\text{ V}/1\text{ V}, V_S = 1\text{ V}/12.2\text{ V}$ ; see Figure 12
Drain OFF Leakage, $I_D$ (Off)	$\pm 0.25$ $\pm 0.1$	$\pm 5$	$\pm 15$	$\pm 0.25$ $\pm 0.1$	$\pm 15$	nA max nA typ	$V_D = 12.2\text{ V}/1\text{ V}, V_S = 1\text{ V}/12.2\text{ V}$ ; see Figure 12
Channel ON Leakage, $I_D, I_S$ (On)	$\pm 0.75$ $\pm 0.4$ $\pm 0.75$	$\pm 5$	$\pm 30$	$\pm 0.75$ $\pm 0.4$ $\pm 0.75$	$\pm 30$	nA max nA typ nA max	$V_S = V_D = 12.2\text{ V}/1\text{ V}$ ; see Figure 13
<b>DIGITAL INPUTS</b>							
Input High Voltage, $V_{INH}$		2.4	2.4		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	0.8		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$		$\pm 0.005$ $\pm 0.5$	$\pm 0.005$ $\pm 0.5$		$\pm 0.005$ $\pm 0.5$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>							
$t_{TRANSITION}$	180	250	250	170	250	ns max	$R_L = 300\ \Omega, C_L = 35\text{ pF}; V_{S1} = 0\text{ V}/8\text{ V},$ $V_{S2} = 8\text{ V}/0\text{ V}$ ; see Figure 14
Break-Before-Make Time Delay, $t_D$	60			60		ns typ	$R_L = 300\ \Omega, C_L = 35\text{ pF};$ $V_{S1} = V_{S2} = 8\text{ V}$ ; see Figure 15
Off Isolation	80			80		dB typ	$R_L = 50\ \Omega, f = 1\text{ MHz}$ ; see Figure 16
Channel-to-Channel Crosstalk	90			70		dB typ	$R_L = 50\ \Omega, f = 1\text{ MHz}$ ; see Figure 17
$C_S$ (Off)	13			13		pF typ	$f = 1\text{ MHz}$
$C_D, C_S$ (On)	65			65		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>							
$I_{DD}$	0.0001			0.0001		$\mu\text{A}$ typ	$V_{DD} = 13.2\text{ V}$ $V_{IN} = 0\text{ V}$ or $5\text{ V}$
	1	2.5	2.5	1	2.5	$\mu\text{A}$ max	
$I_L$	0.0001			0.0001		$\mu\text{A}$ typ	$V_L = 5.5\text{ V}$
	1	2.5	2.5	1	2.5	$\mu\text{A}$ max	

<sup>1</sup> Temperature ranges are as follows: B Version:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ ; T Version:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$  unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	44 V
$V_{DD}$ to GND	-0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to -25 V
$V_L$ to GND	-0.3 V to $V_{DD} + 0.3$ V
Analog, Digital Inputs <sup>1</sup>	$V_{SS} - 2$ V to $V_{DD} + 2$ V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty-Cycle Maximum)	100 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +125°C
Extended (T Version)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
CERDIP Package, Power Dissipation	600 mW
$\theta_{JA}$ , Thermal Impedance	110°C/W
Lead Temperature, Soldering (10 sec)	300°C
PDIP Package, Power Dissipation	400 mW
$\theta_{JA}$ , Thermal Impedance	100°C/W
Lead Temperature, Soldering (10 sec)	260°C
SOIC Package, Power Dissipation	400 mW
$\theta_{JA}$ , Thermal Impedance	155°C/W
MSOP Package, Power Dissipation	315 mW
$\theta_{JA}$ , Thermal Impedance	205°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

<sup>1</sup>Overvoltages at IN, S or D is clamped by internal diodes. Limit current to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADG419

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

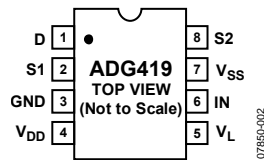


Figure 2. Pin Configuration

Table 4. Pin Function Description

Pin No.	Mnemonic	Description
1	D	Drain terminal. May be an input or an output.
2	S1	Source terminal. May be an input or an output.
3	GND	Ground (0 V) reference.
4	V <sub>DD</sub>	Most positive power supply potential.
5	V <sub>L</sub>	Logic power supply (5 V).
6	IN	Logic control input.
7	V <sub>SS</sub>	Most negative power supply potential in dual-supply applications. In single-supply applications, it may be connected to GND.
8	S2	Source terminal. May be an input or an output.

Table 5. Truth Table

Logic	Switch 1	Switch 2
0	On	Off
1	Off	On

# TYPICAL PERFORMANCE CHARACTERISTICS

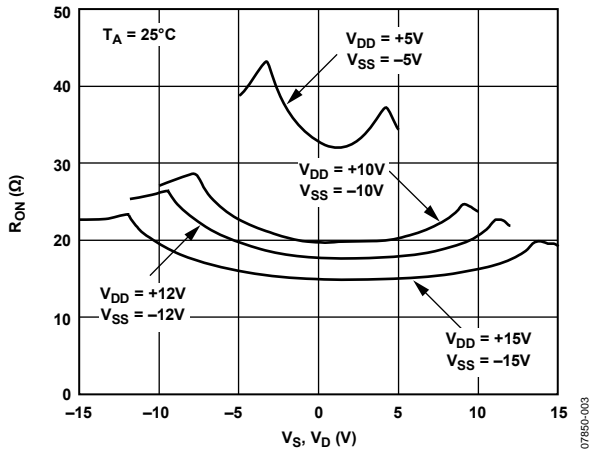


Figure 3.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ), Dual-Supply Voltage

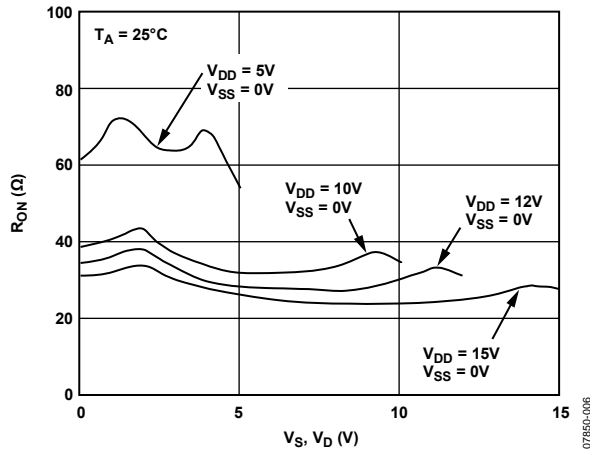


Figure 6.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ), Single-Supply Voltage

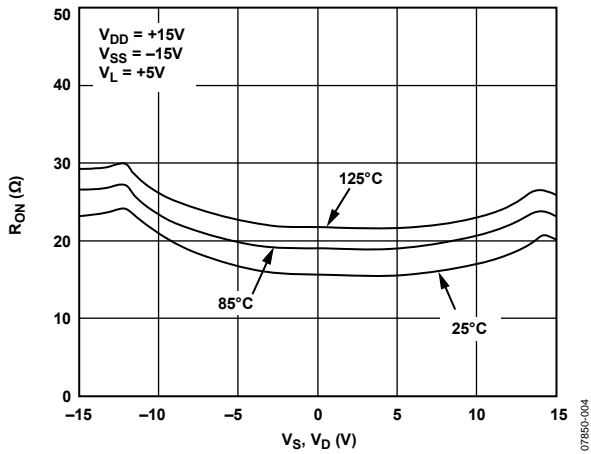


Figure 4.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures

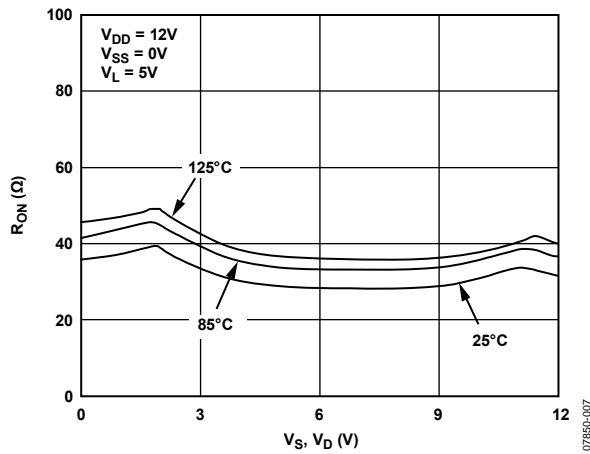


Figure 7.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures

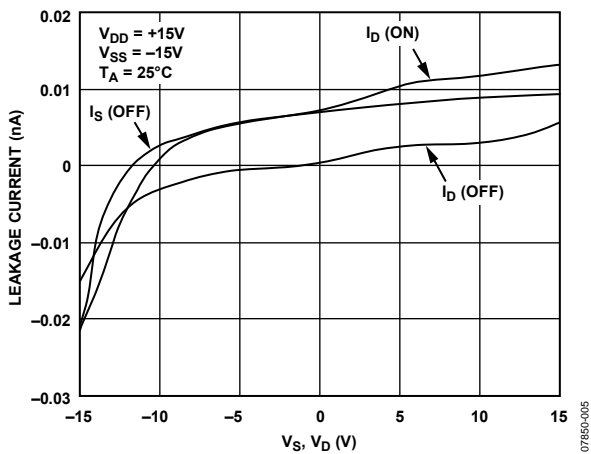


Figure 5. Leakage Currents as a Function of  $V_S$  ( $V_D$ )

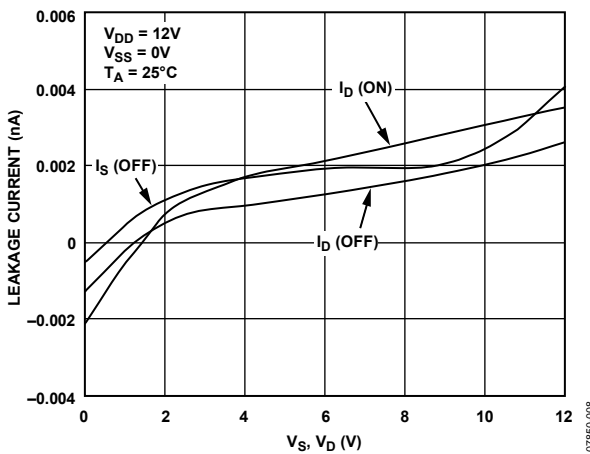


Figure 8. Leakage Currents as a Function of  $V_S$  ( $V_D$ )



# ADG419

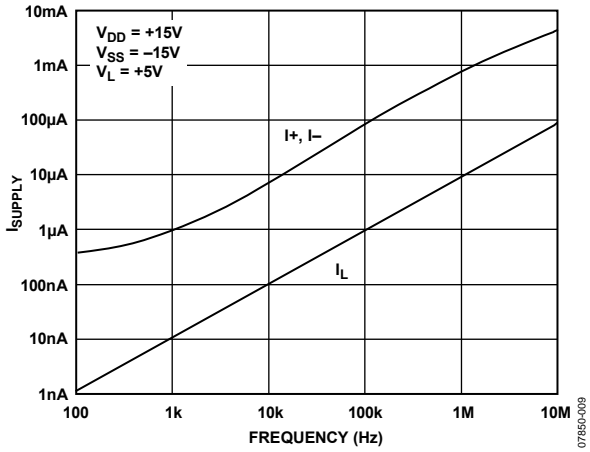


Figure 9. Supply Current ( $I_{SUPPLY}$ ) vs. Input Switching Frequency

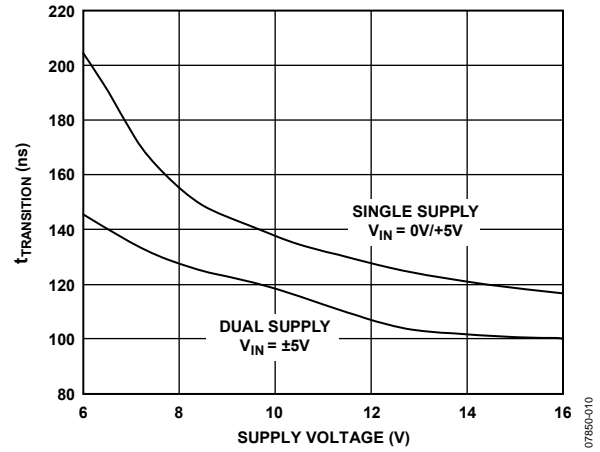


Figure 10. Transition Time ( $t_{TRANSITION}$ ) vs. Power Supply Voltage

# TEST CIRCUITS

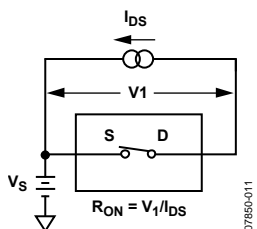


Figure 11. On Resistance

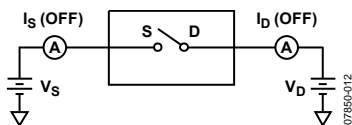


Figure 12. Off Leakage

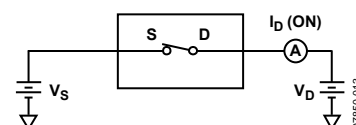


Figure 13. On Leakage

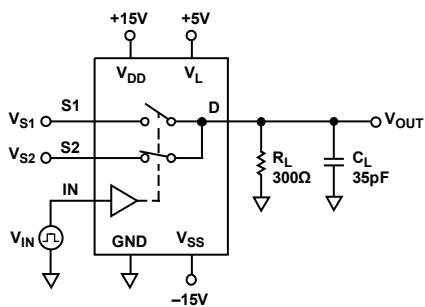
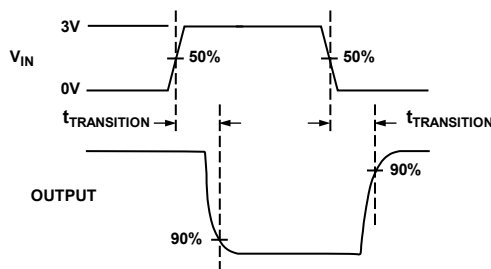


Figure 14. Transition Time,  $t_{\text{TRANSITION}}$



07850-014

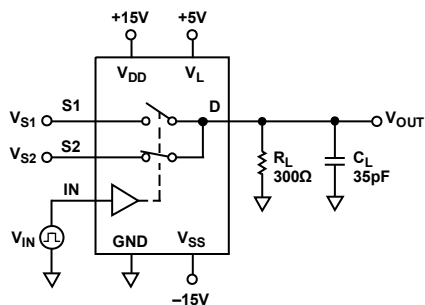
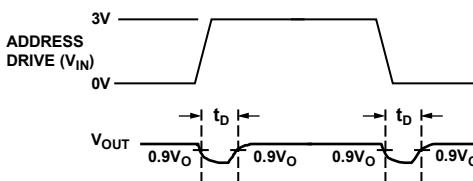


Figure 15. Break-Before-Make Time Delay,  $t_D$



07850-015

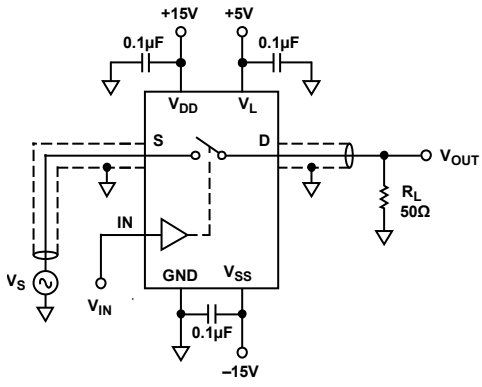
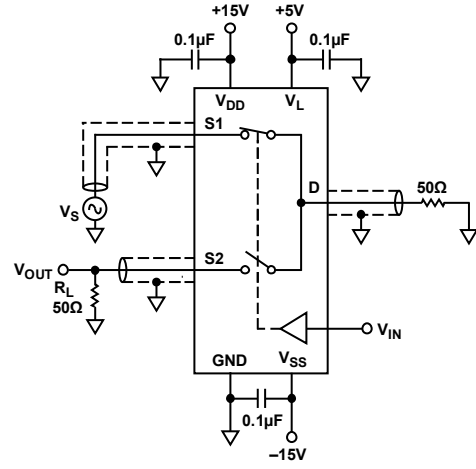


Figure 16. Off Isolation

07860-016



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \times \log |V_S/V_{OUT}|$$

Figure 17. Crosstalk

07860-017

## TERMINOLOGY

$V_{DD}$

Most positive power supply potential.

$V_{SS}$

Most negative power supply potential in dual-supply applications.  
In single-supply applications, it may be connected to GND.

$V_L$

Logic power supply (5 V).

**GND**

Ground (0 V) reference.

**S**

Source terminal. May be an input or an output.

**D**

Drain terminal. May be an input or an output.

**IN**

Logic control input.

**R<sub>ON</sub>**

Ohmic resistance between D and S.

**I<sub>S</sub> (Off)**

Source leakage current with the switch off.

**I<sub>D</sub> (Off)**

Drain leakage current with the switch off.

**I<sub>D</sub>, I<sub>S</sub> (On)**

Channel leakage current with the switch on.

**V<sub>D</sub> (V<sub>S</sub>)**

Analog voltage on terminals D, S.

**C<sub>S</sub> (Off)**

Off switch source capacitance.

**C<sub>D</sub>, C<sub>S</sub> (On)**

On switch capacitance.

**t<sub>TRANSITION</sub>**

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

**t<sub>D</sub>**

Off time or on time measured between the 90% points of both switches when switching from one address state to the other.

**V<sub>INL</sub>**

Maximum input voltage for Logic 0.

**V<sub>INH</sub>**

Minimum input voltage for Logic 1.

**I<sub>INL</sub> (I<sub>INH</sub>)**

Input current of the digital input.

**Crosstalk**

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

**Off Isolation**

A measure of unwanted signal coupling through an off channel.

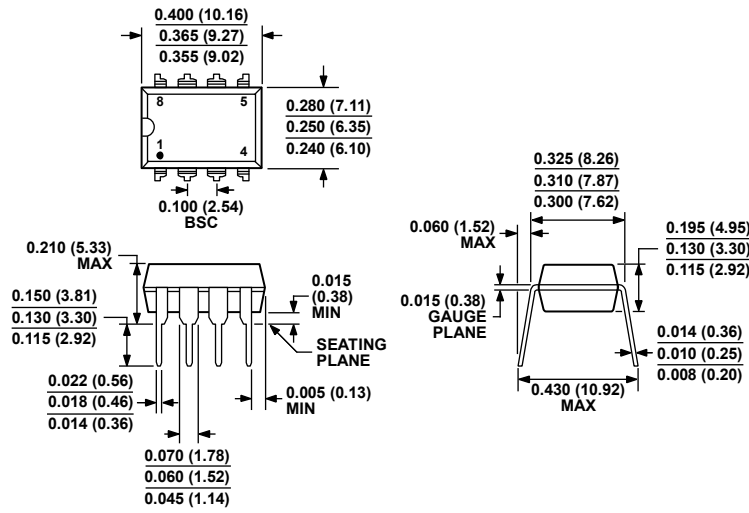
**I<sub>DD</sub>**

Positive supply current.

**I<sub>SS</sub>**

Negative supply current.

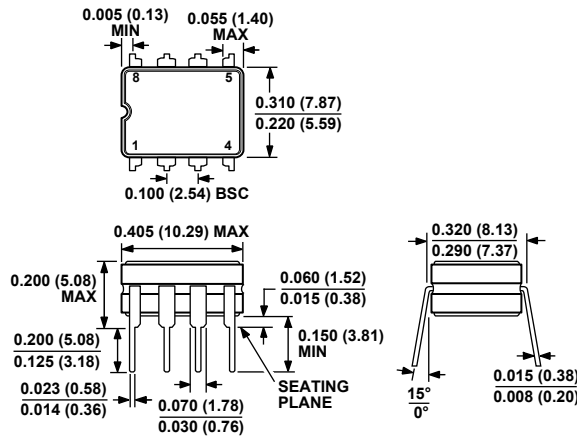
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 18. 8-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-8)

Dimensions shown in inches and (millimeters)

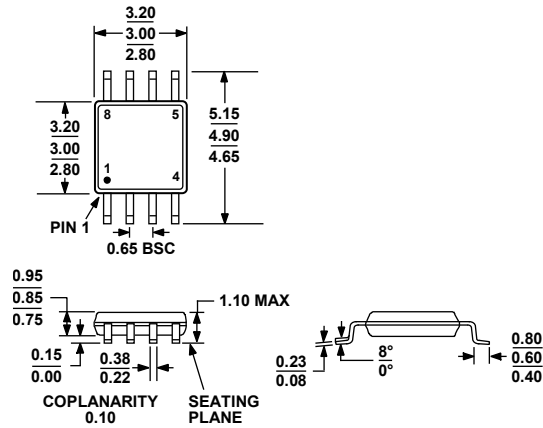


CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 19. 8-Lead Ceramic Dual In-Line Package [CERDIP] (Q-8)

Dimensions shown in inches and (millimeters)

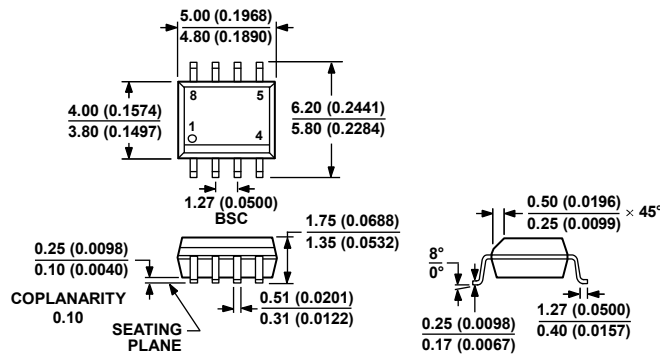
070606-A



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 20. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 21. 8-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

012407-A

**ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option	Branding
ADG419BN	-40°C to +125°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8	
ADG419BNZ <sup>1</sup>	-40°C to +125°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8	
ADG419BR	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BR-REEL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BR-REEL7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRZ <sup>1</sup>	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRZ-REEL <sup>1</sup>	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRZ-REEL7 <sup>1</sup>	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRM	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB
ADG419BRM-REEL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB
ADG419BRM-REEL7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB
ADG419BRMZ <sup>1</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB#
ADG419BRMZ-REEL <sup>1</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB#
ADG419BRMZ-REEL7 <sup>1</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB#
ADG419TQ	-55°C to +125°C	8-Lead Ceramic Dual In-Line Package [CERDIP]	Q-8	

<sup>1</sup> Z = RoHS Compliant Part, # denotes that RoHS compliant part is top or bottom marked.

**ADG419**

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