iMOTION™ IMC100

High performance motor control IC series

IMC100
Quality Requirement Category: Industry

Feature list

- Motion Control Engine (MCE) as ready-to-use solution for variable speed drives
- Field oriented control (FOC) for permanent magnet synchronous motor (PMSM)
- Space vector PWM with sinusoidal commutation and integrated protection features
- Current sensing via single or leg shunt
- Sensorless operation
- Optional support for hall sensors (analog or digital)
- Optional boost or totem pole PFC control integrated
- Flexible host interface options for motor control commands: UART, PWM or analog input signal
- Support for IEC 60335 (‘Class B’)
- Integrated scripting engine for application flexibility
- Multiple package options

Applications

- Refrigerators
- Home appliances
- Pumps, fans
- ...any other PMSM drive

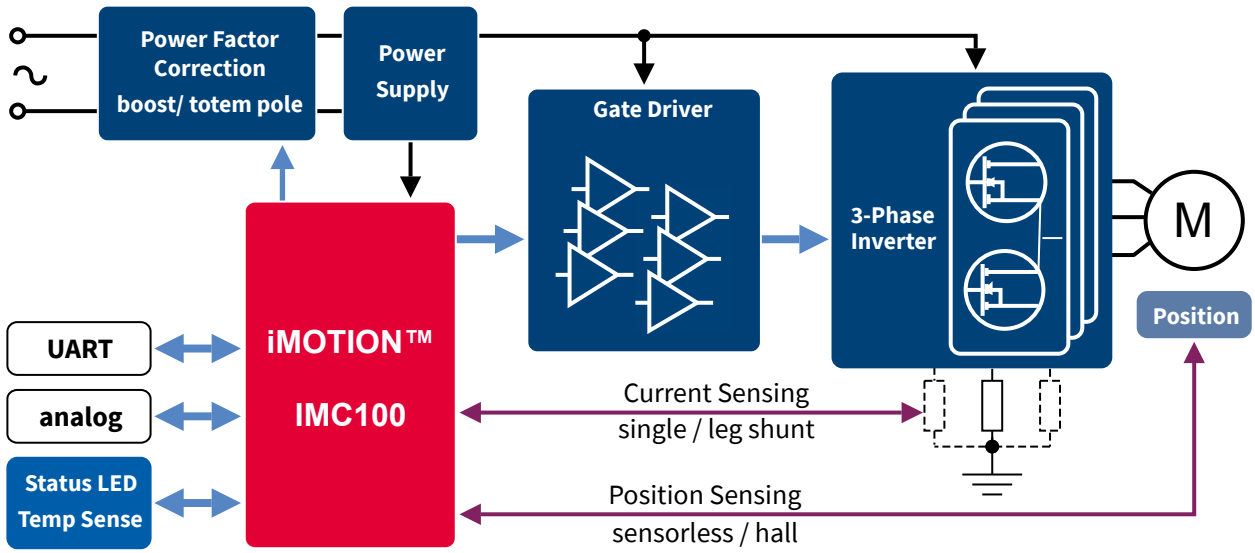
Ordering Information

Product Type	Application	Package
IMC101T-T038	single motor	TSSOP-38
IMC101T-Q048		QFN-48
IMC101T-F048		TQFP-48
IMC101T-F064		LQFP-64
IMC102T-F048	single motor + PFC (boost, totem pole)	TQFP-48
IMC102T-F064		LQFP-64

Note: *Variants in TQFP-48 package under development.*

Description

iMOTION™ IMC100 is a family of highly integrated ICs for the control of variable speed drives. By integrating both the required hardware and software to perform control of a permanent magnet synchronous motor (PMSM) they provide the shortest time to market for any motor system at the lowest system and development cost.



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About this document

Scope and purpose

This Datasheet describes the mechanical, electrical and functional characteristics of the iMOTION™ IMC100 series of motor control ICs. If no specific device is given the characteristics are valid for all devices within the iMOTION™ IMC100 series.

For a detailed description of the functionality and configuration options please refer to the reference manual of the Motion Control Engine.

Intended audience

The Datasheet is targeting developers implementing a variable speed drive.

1 Block Diagram Reference

The block diagram below gives an overview on the available functional units in the iMOTION™ IMC100 family. Not all units are required in all applications and some modules might share pins in smaller packages. Please refer to the pin configuration for the individual packages and the application schematic examples given.

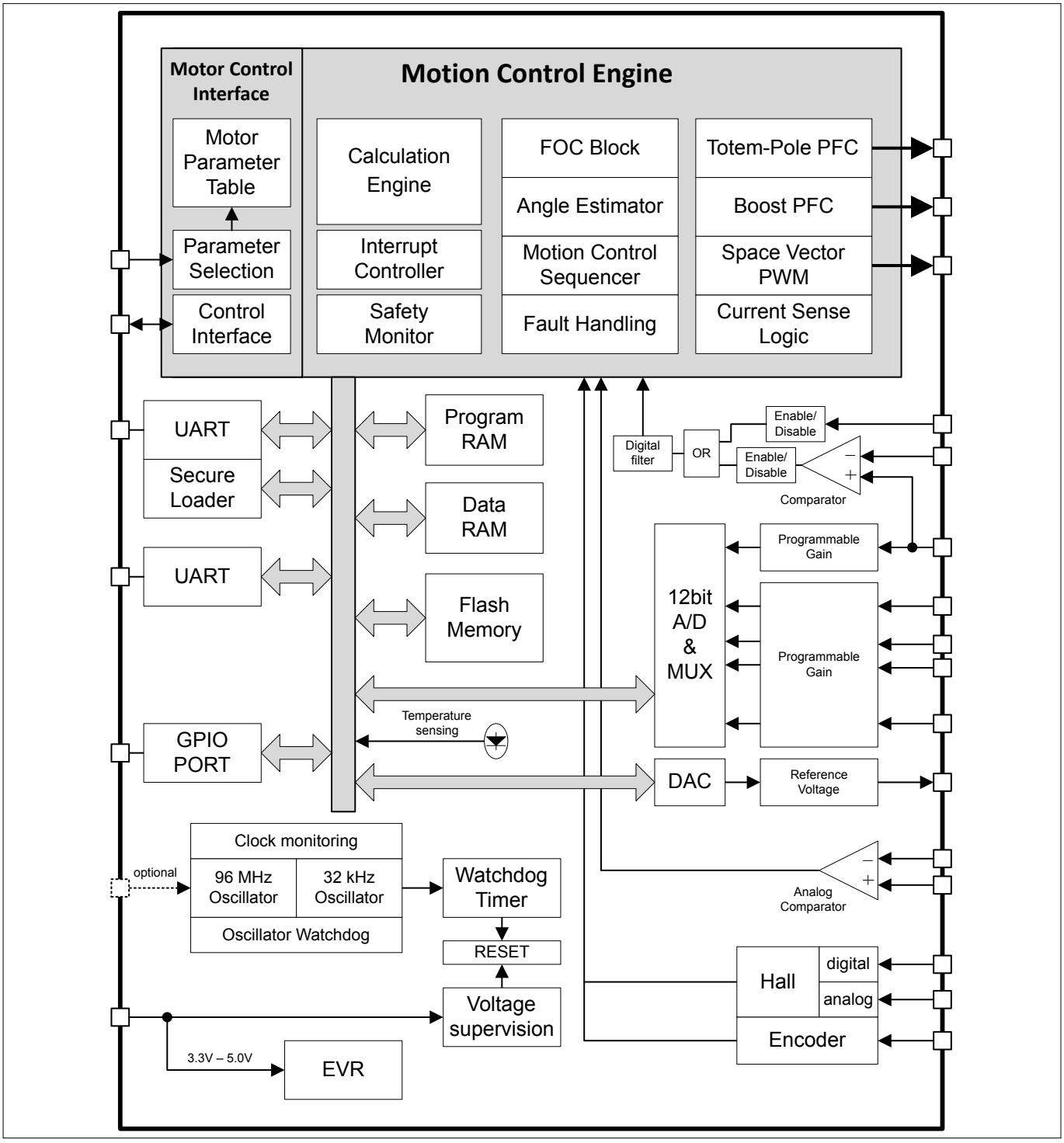

Figure 1 Block diagram

2 Pin Configuration

The following tables give the pin configurations of the individual devices of the IMC100 series in the available packages.

The pin type is specified as follows:

- I - digital input
- O - digital output
- AIN - analog input

The pin function given below refers to the standard software configuration. Different software might configure pins differently. Some of the input pins can be configured to have pull up or pull down resistor and some output pins can be configured to push-pull or open drain. This is described in the reference manual of the respective software.

Pins that do not have any signal assigned are reserved for future use. These pins should be left unconnected and neither be connected to ground nor to the positive supply.

Note: *All required reference voltages are generated by an internal DAC, therefor the pins like REFU, REFV, REFW and PFCREF only require a blocking capacitor.*

2.1 Pin Configuration IMC101T

Table 1 Pin list

Signal	Type	LQFP-64	VQFN-48	TQFP-48	TSSOP-38	Description
Supply						
VDD	Power	2, 24, 25, 35, 50	18, 19, 27, 38	18, 19, 27, 38	10, 26	Supply Voltage
VSS	Power	1, 23, 49	17, 37	17, 37	9, 25	Ground
Motor control						
PWMUL	O	29	21	21	11	PWM output phase U low side
PWMUH	O	30	22	22	12	PWM output phase U high side
PWMVL	O	31	23	23	13	PWM output phase V low side
PWMVH	O	32	24	24	14	PWM output phase V high side
PWMWL	O	33	25	25	15	PWM output phase W low side
PWMWH	O	34	26	26	16	PWM output phase W high side
GK	I	36	28	28	18	Motor gate kill input
VDC	AIN	14	8	8	2	DC bus sensing input
IU/ISS	AIN	18	12	12	6	Current sense input phase U / single shunt
IV	AIN	15	9	9	3	Current sense input phase V / analog input
IW	AIN	11	5	5	37	Current sense input phase W / analog input
REFU	AIN	17	11	11	5	Itrip phase U reference / analog input
REFV	AIN	16	10	10	4	Itrip phase V reference / analog input
REFW	AIN	10	4	4	36	Itrip phase W reference / analog input

Table 1 Pin list (continued)

Signal	Type	LQFP-64	VQFN-48	TQFP-48	TSSOP-38	Description
Interface						
DIR	I	52	40	40	28	Direction input
DUTYFREQ	I	55	43	43	31	Duty/Frequency input
VSP	AIN	9	3	3	35	Analog speed reference input
PGOUT	O	42	30	30	21	Pulse output
PARAM	AIN	20	14	14	8	Parameter table selection, analog
PAR0	I	3	33	33	22	Parameter page select 0
PAR1	I	4	34	34	23	Parameter page select 1
PAR2	I	5	35	35	24	Parameter page select 2
PAR3	I	6	36	36	27	Parameter page select 3
NTC	AIN	13	7	7	7	External thermistor input
LED	O	41	29	29	17	Status LED
Communication						
RX0	I	57	45	45	33	Serial port 0, receive input
TX0	O	58	46	46	34	Serial port 0, transmit output
RX1	I	63	47	47	20	Serial port 1, receive input
TX1	O	64	48	48	19	Serial port 1, transmit output

2.2 Pin Configuration Drawing IMC101T

The following drawings give the position of the functional pins for the available packages.

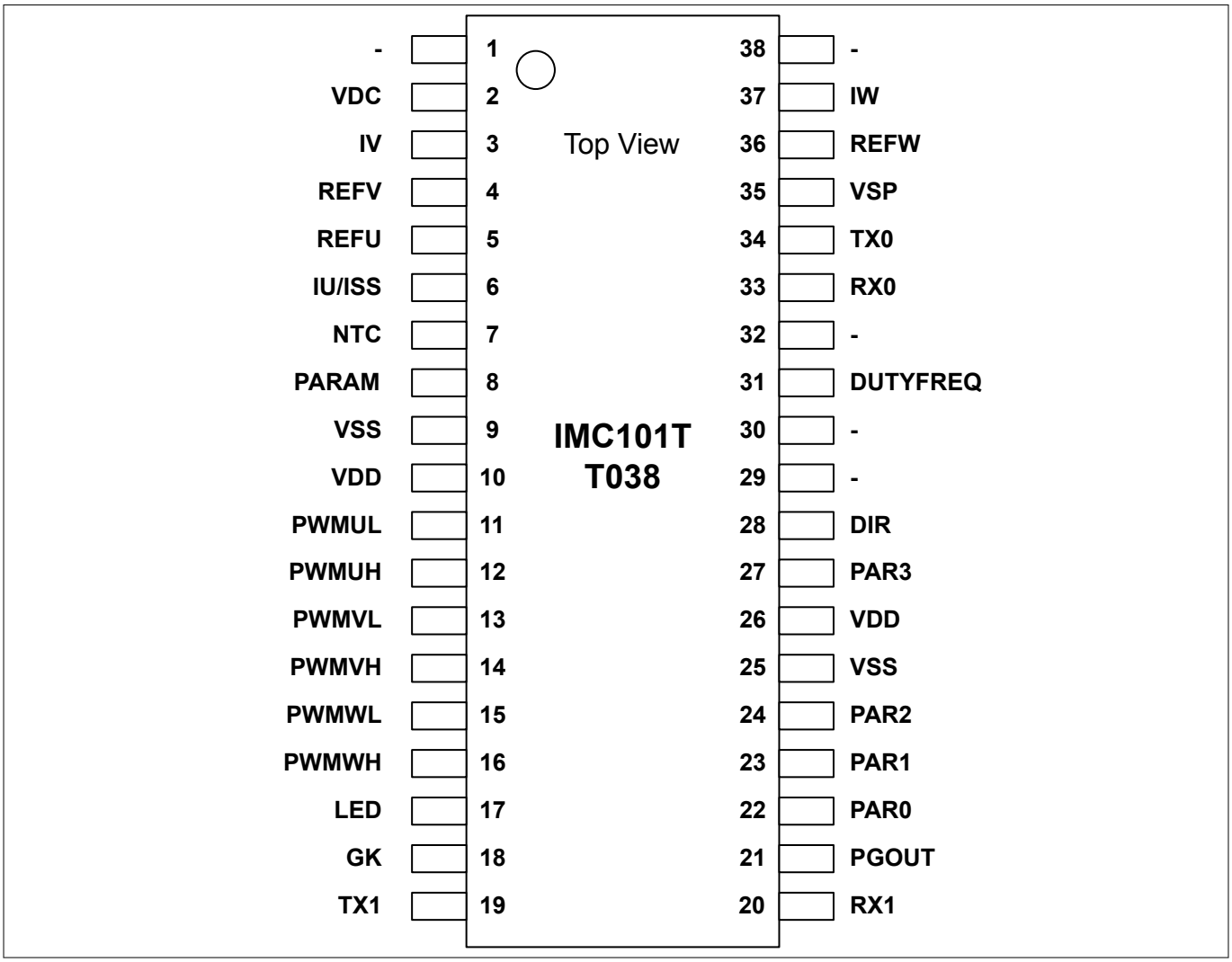

Figure 2 IMC101T-T038

Pins that do not have any signal assigned are reserved for future use. These pins should be left unconnected and neither be connected to ground nor to the positive supply.

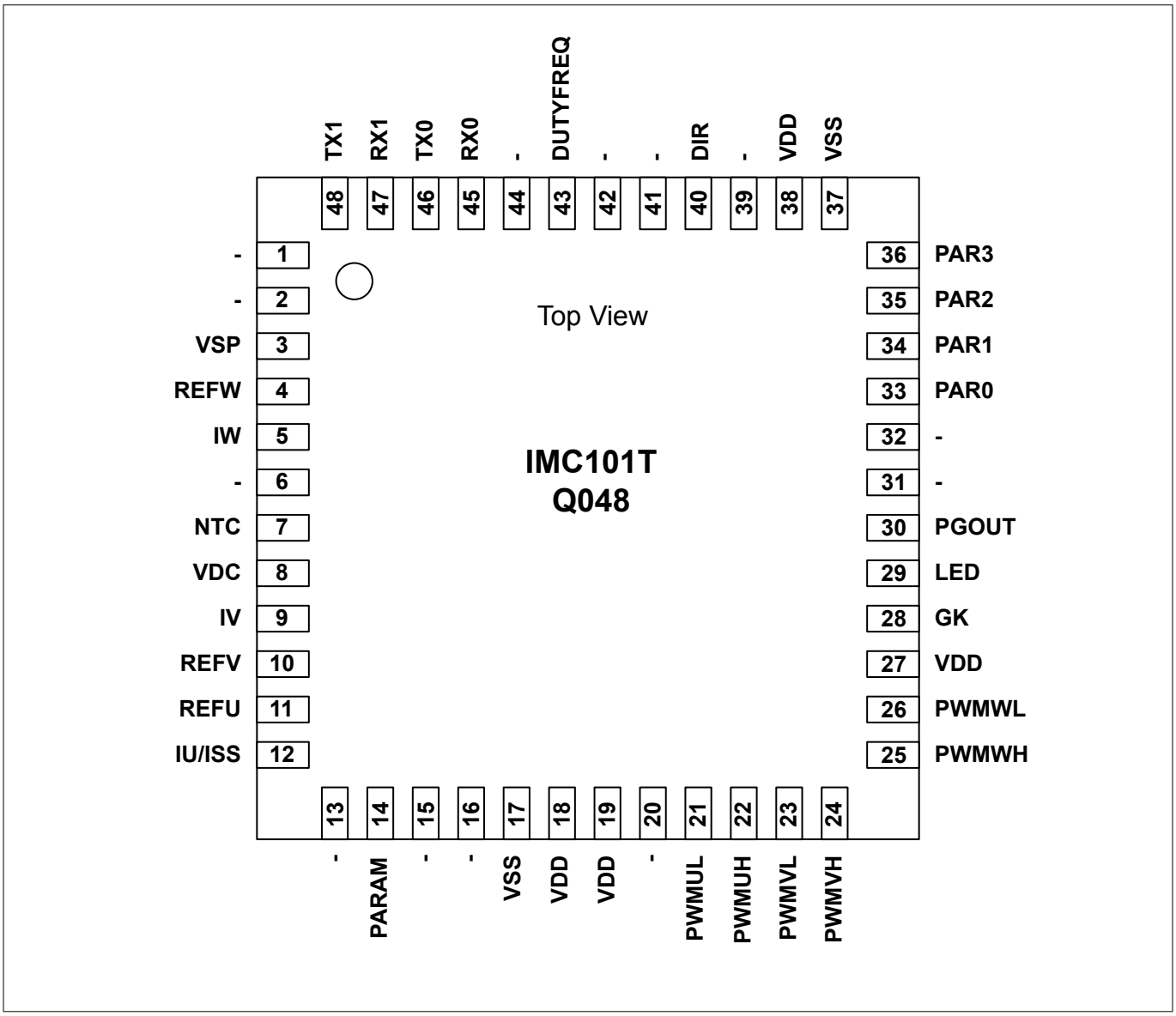

Figure 3 IMC101T-Q048

Pins that do not have any signal assigned are reserved for future use. These pins should be left unconnected and neither be connected to ground nor to the positive supply.

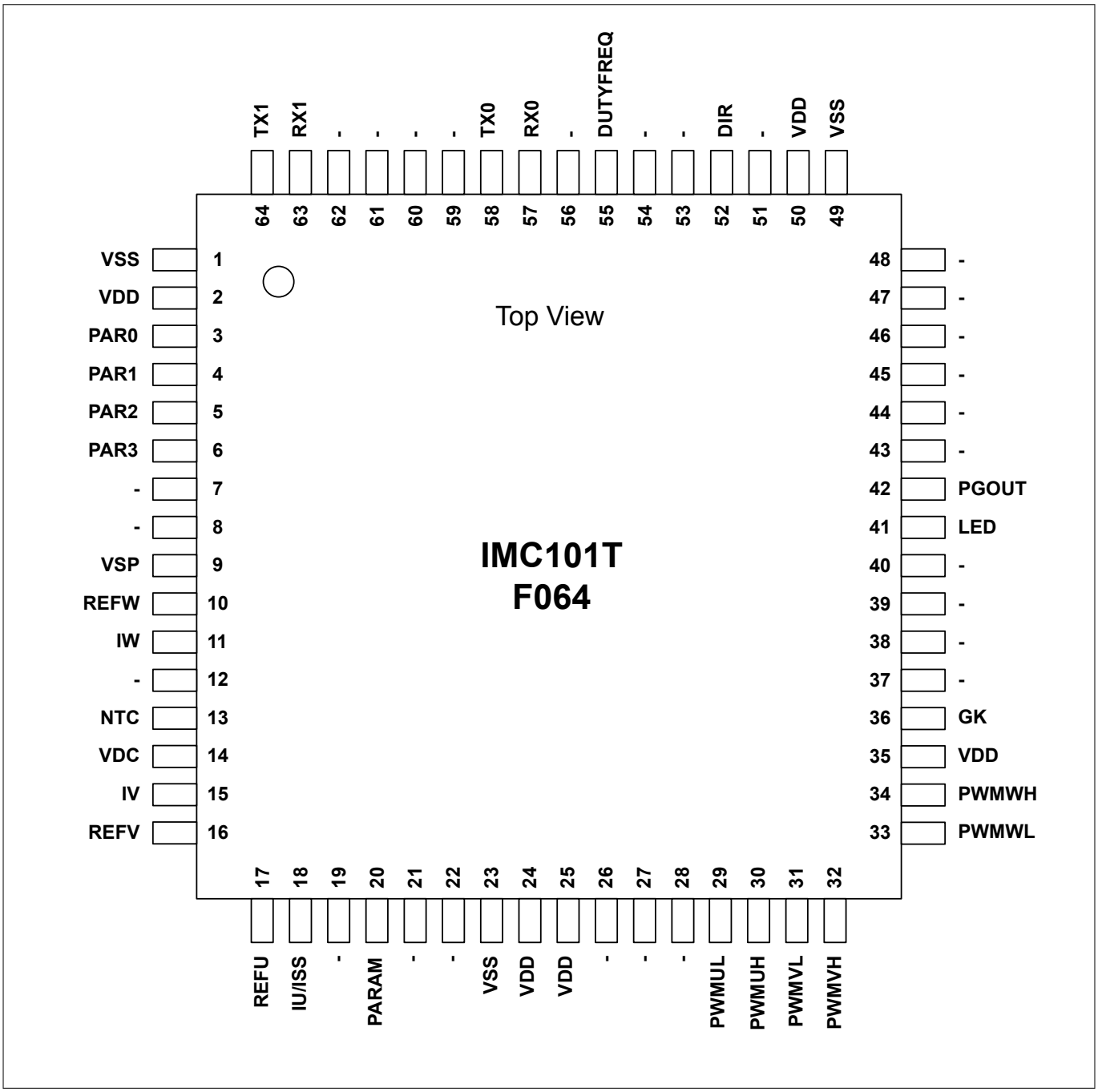

Figure 4 IMC101T-F064

Pins that do not have any signal assigned are reserved for future use. These pins should be left unconnected and neither be connected to ground nor to the positive supply.

2.3 Pin Configuration IMC102T

Table 2 Pin list

Signal	Type	LQFP-64	TQFP-48	Description
Supply				
VDD	Power	2, 24, 25, 35, 50	18, 19, 27, 38	Supply Voltage
VSS	Power	1, 23, 49	17, 37	Ground
Motor control				
PWMUL	O	29	21	PWM output phase U low side
PWMUH	O	30	22	PWM output phase U high side
PWMVL	O	31	23	PWM output phase V low side
PWMVH	O	32	24	PWM output phase V high side
PWMWL	O	33	25	PWM output phase W low side
PWMWH	O	34	26	PWM output phase W high side
GK	I	36	28	Motor gate kill input
VDC	AIN	14	8	DC bus sensing input
IU/ISS	AIN	18	12	Current sense input phase U / single shunt
IV	AIN	15	9	Current sense input phase V / analog input
IW	AIN	11	5	Current sense input phase W / analog input
REFU	AIN	17	11	Itrip phase U reference / analog input
REFV	AIN	16	10	Itrip phase V reference / analog input
REFW	AIN	10	4	Itrip phase W reference / analog input
Power factor correction				
PFCG0	O	44	31	PFC gate drive 0
PFCG1	O	43	32	PFC gate drive 1 (totem pole only - high side switch)
PFCI	AIN	12	6	PFC current sensing
PFCREF	AIN	21	15	Itrip PFC reference input
PFCITRIP	AIN	22	16	Itrip PFC input
VAC1	AIN	20	14	VAC sense input line 1
VAC2	AIN	19	13	VAC sense input line 2
Interface				
DIR	I	52	40	Direction input
DUTYFREQ	I	55	43	Duty/Frequency input
VSP	AIN	9	3	Analog speed reference input
PGOUT	O	42	30	Pulse output
PAR0	I	3	33	Parameter page select 0
PAR1	I	4	34	Parameter page select 1

Table 2 Pin list (continued)

Signal	Type	LQFP-64	TQFP-48	Description
PAR2	I	5	35	Parameter page select 2
PAR3	I	6	36	Parameter page select 3
NTC	AIN	13	7	External thermistor input
LED	O	41	29	Status LED
Communication				
RX0	I	57	45	Serial port 0, receive input
TX0	O	58	46	Serial port 0, transmit output
RX1	I	63	47	Serial port 1, receive input
TX1	O	64	48	Serial port 1, transmit output

2.4 Pin Configuration Drawing IMC102T

The following drawings give the position of the functional pins for the available packages.

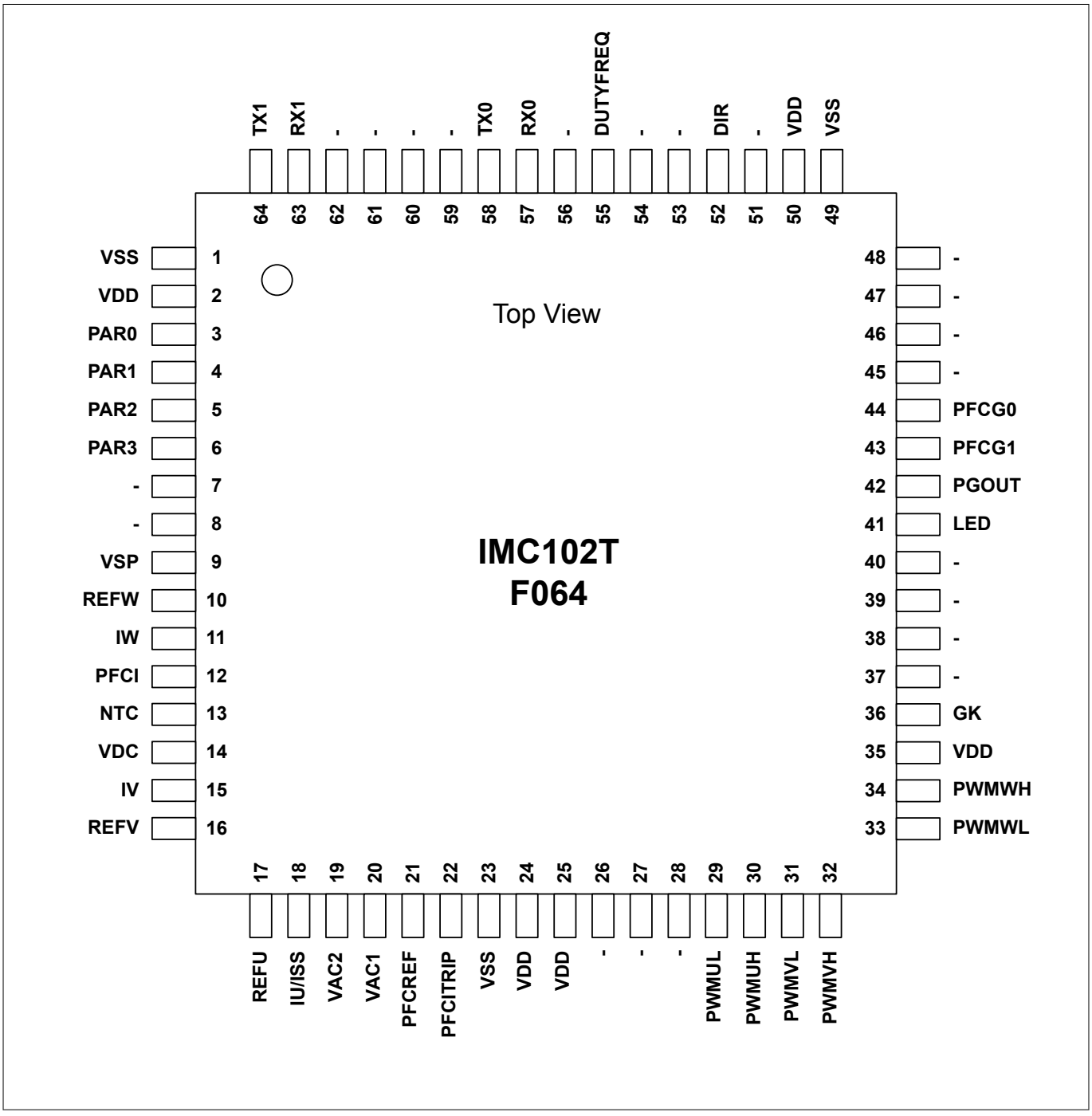

Figure 5 IMC102T-F064

Pins that do not have any signal assigned are reserved for future use. These pins should be left unconnected and neither be connected to ground nor to the positive supply.

3 Functional description

iMOTION™ IMC100 is a series of highly integrated ICs for the control of a Permanent Magnet Synchronous Motor (PMSM). IMC101 devices provide control of a single motor while the IMC102 devices control the motor and additionally a boost or totem pole power factor correction (PFC).

The IMC100 series is based on Infineon's Motion Control Engine (MCE) and integrate all hardware and software functions required to implement a closed loop sensorless (or optionally sensor based) control algorithm for permanent magnet motors. IMC100 devices do not require any software programming and can be configured for a wide range of motor control inverters.

The IMC100 series takes advantage of a new hardware platform that is based on a comprehensive set of innovative analog and motor control peripherals. The high level of integration both in terms of hardware modules and software algorithms results in a minimum number of external components required for the implementation of the inverter control.

Infineon's patented and field proven Motion Control Engine (MCE) implements field oriented control (FOC) using single or leg shunt current feedback and uses space vector pulse width modulation (PWM) with sinusoidal signals to achieve highest energy efficiency. In addition to the motor control algorithm it also integrates multiple configurable protection features like over- and under-voltage, over current, rotor lock etc. to protect both the power stage as well as the motor during application tuning or in case of malfunction.

The second generation of the MCE further improves the performance of the sensorless control algorithm and adds functionality like optional sensor support for applications that require accurate rotor positioning, two types of ready-to-use PFC algorithms as well as more and flexible and faster host interface options.

The IMC100 series is offered in several device and package variants for applications from single motor control to motor control plus PFC. All devices can be used in applications requiring functional safety according to IEC 60335 ('Class B').

There are multiple versions of the MCE software offered by Infineon and made available for download from the Infineon web site.

By using a special secure boot loader algorithm in combination with type specific chip IDs it is assured that these MCE software versions can only be installed onto the matching hardware derivatives, i.e. IMC100 variants for which the software has been tested and released for. Infineon provides the tools to program these software images for download from the website.

This data sheet provides all electrical, mechanical, thermal and quality parameters. A detailed description of the features, functionality and configuration of the Motion Control Engine (MCE) can be found in the respective reference manual of the MCE.

The application schematics in the following chapters show some examples of different use cases for the IMC100 devices. The combination of the different configuration options like leg vs. single shunt, sensorless or sensored operation, boost or totem pole PFC etc. is not limited to the examples shown here but can be chosen according to the individual application requirements.

3.1 Application schematic motor control single shunt

Figure 6 gives the schematic diagram for a motor control system using the IMC101 in sensorless operation and single shunt mode.

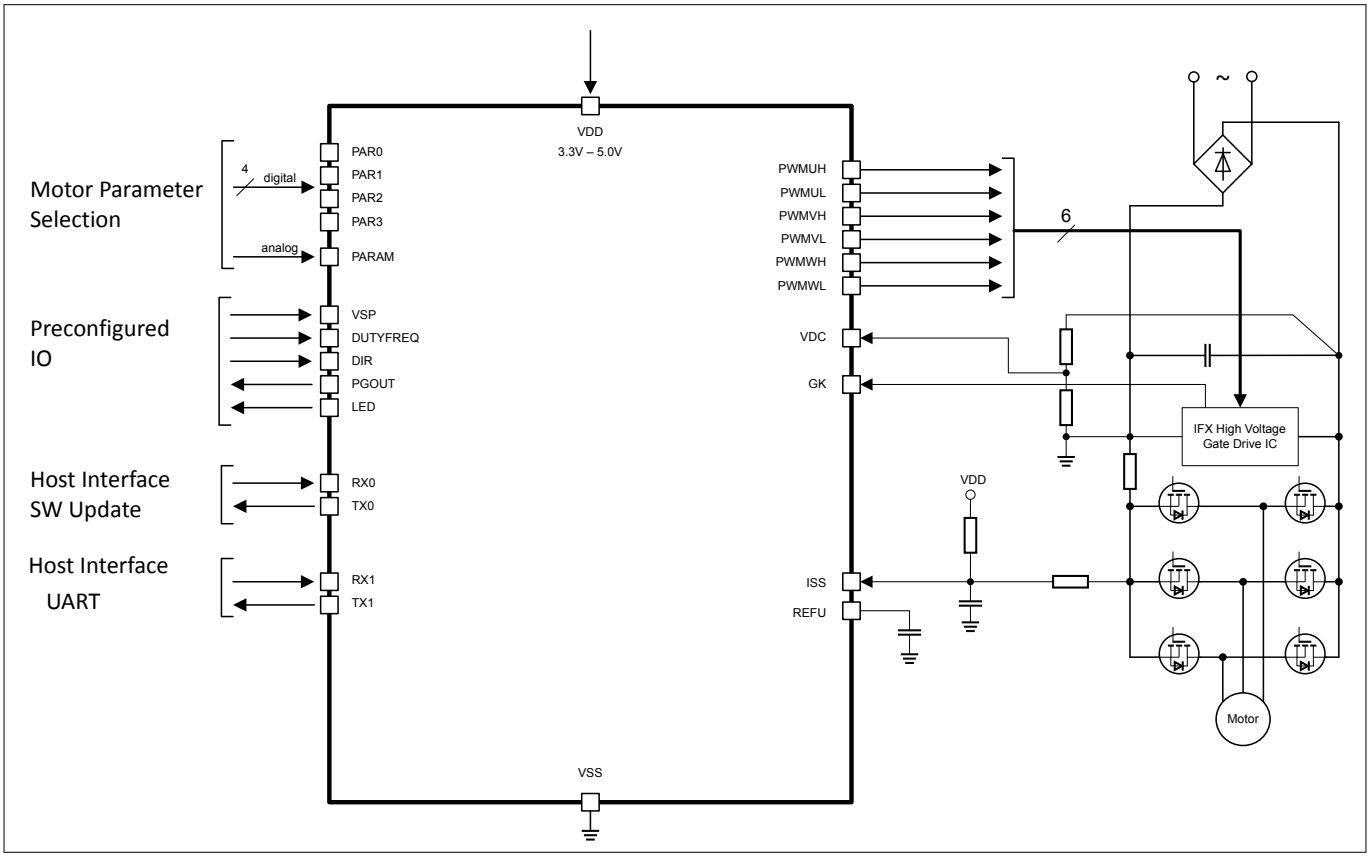

Figure 6 IMC101 in single shunt configuration

3.2 Application schematic motor control leg shunt

Figure 7 gives the schematic diagram for a motor control system using the IMC101 in sensorless operation and leg shunt mode.

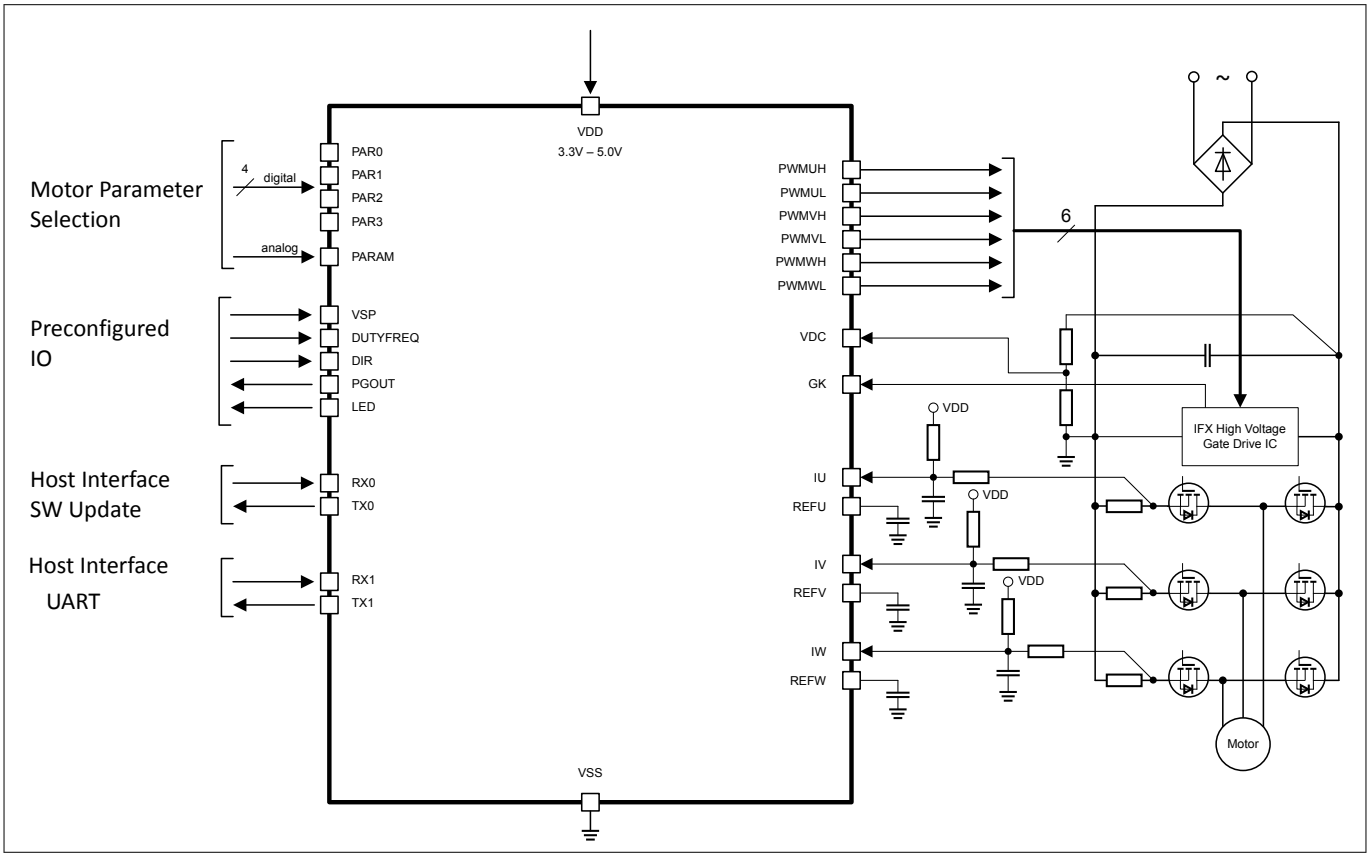

Figure 7 IMC101 in leg shunt configuration

3.3 Application schematic motor control plus boost PFC

Figure 8 gives the schematic diagram for a motor control system with boost PFC using the IMC102 in sensorless operation and single shunt mode.

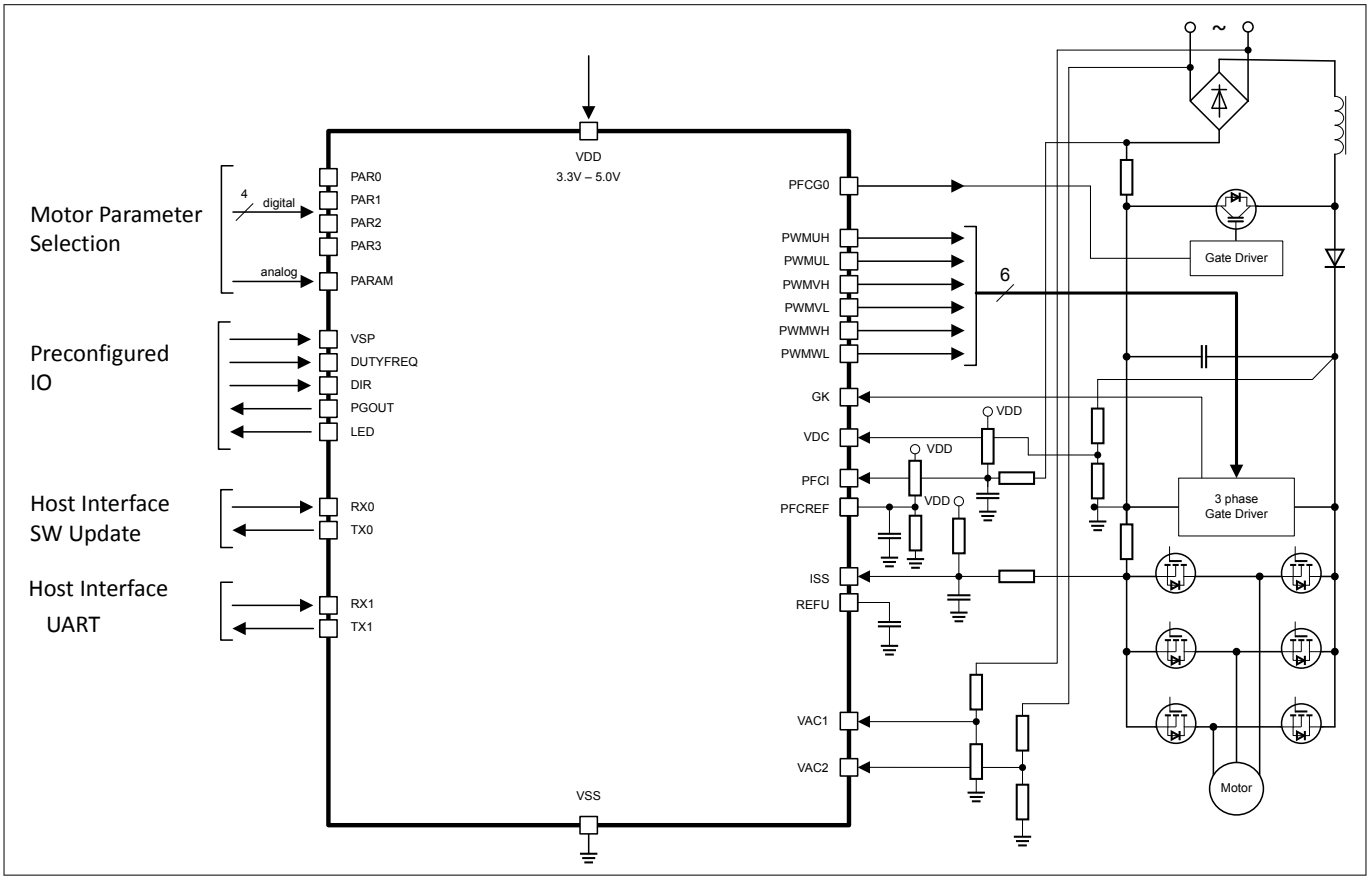

Figure 8 IMC102 in single shunt configuration with boost PFC control

3.4 Application schematic motor control plus totem pole PFC

Figure 9 gives the schematic diagram for a motor control system with totem pole PFC using the IMC102 in sensorless operation and single shunt mode.

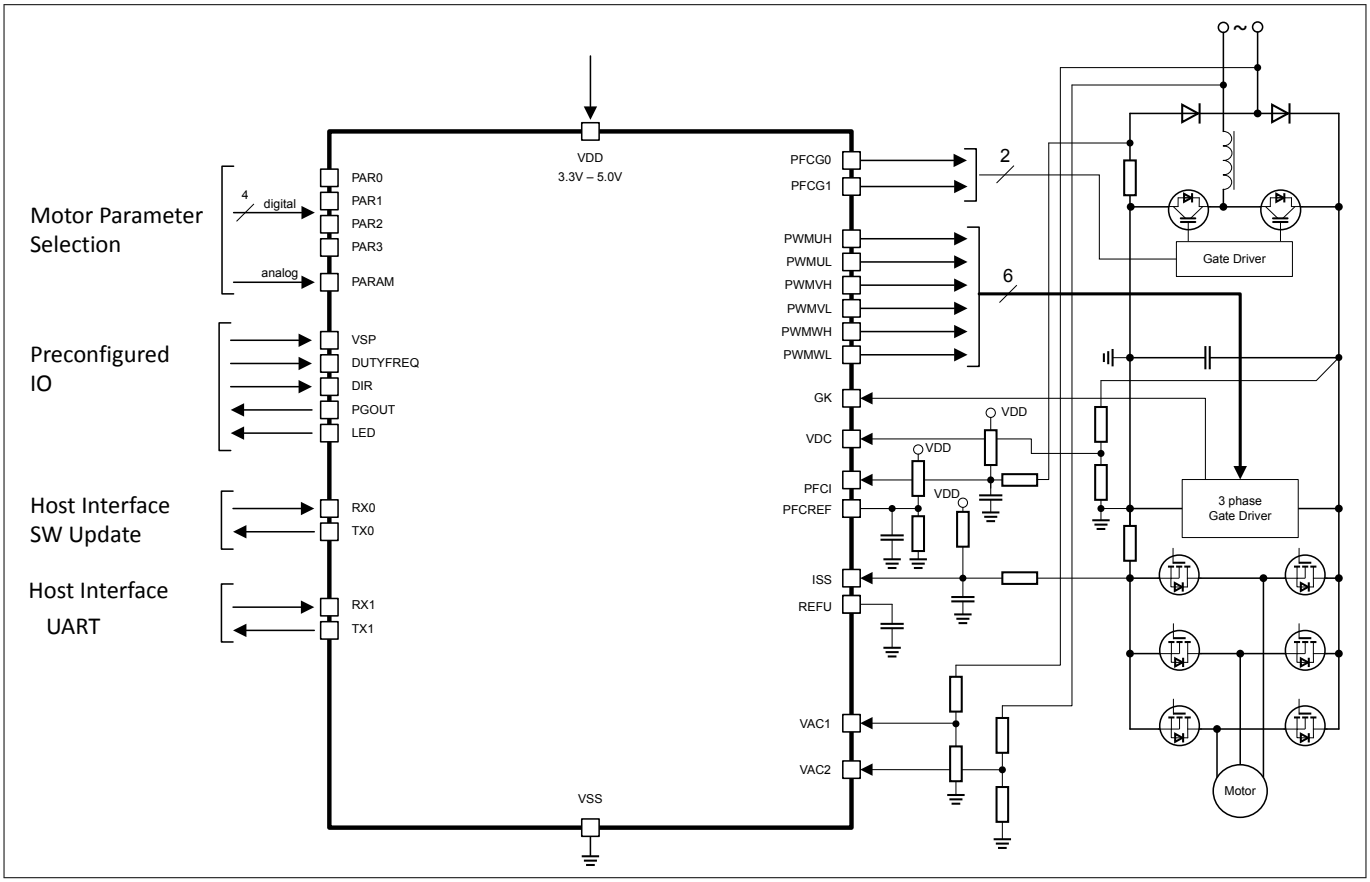

Figure 9 IMC102 in single shunt configuration with totem pole PFC

4 Electrical characteristics and parameters

4.1 General Parameters

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the IMC100 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**

  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the IMC100 and must be regarded for a system design.
- **SR**

  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the IMC100 is designed in.

4.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Ambient temperature	T_A SR	-40	–	105	°C	–
Junction temperature	T_J SR	-40	–	115	°C	–
Storage temperature	T_{ST} SR	-55	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP} *SR*	-0.3	–	6	V	–
Voltage on digital pins with respect to V_{SSP}	V_{IN} SR	-0.3	–	V_{DDP} + 0.3 or max. 6	V	whichever is lower
Voltage on analog input pins with respect to V_{SSP}	V_{AIN} V_{AREF} SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Input current on any pin during overload condition	I_{IN} *SR*	-10	–	10	mA	–
Absolute maximum sum of all input currents during overload condition	ΣI_{IN} *SR*	-50	–	+50	mA	–

4.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 4 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- ***Operating Conditions*** are met for
  - pad supply levels (V_{DDP})
  - temperature

If a pin current is outside of the ***Operating Conditions*** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: *An overload condition on one or more pins does not require a reset.*

Note: *A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.*

Table 4 Overload Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input current on analog port pins during overload condition	I_{OVA} SR	-3	–	3	mA	
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 10 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

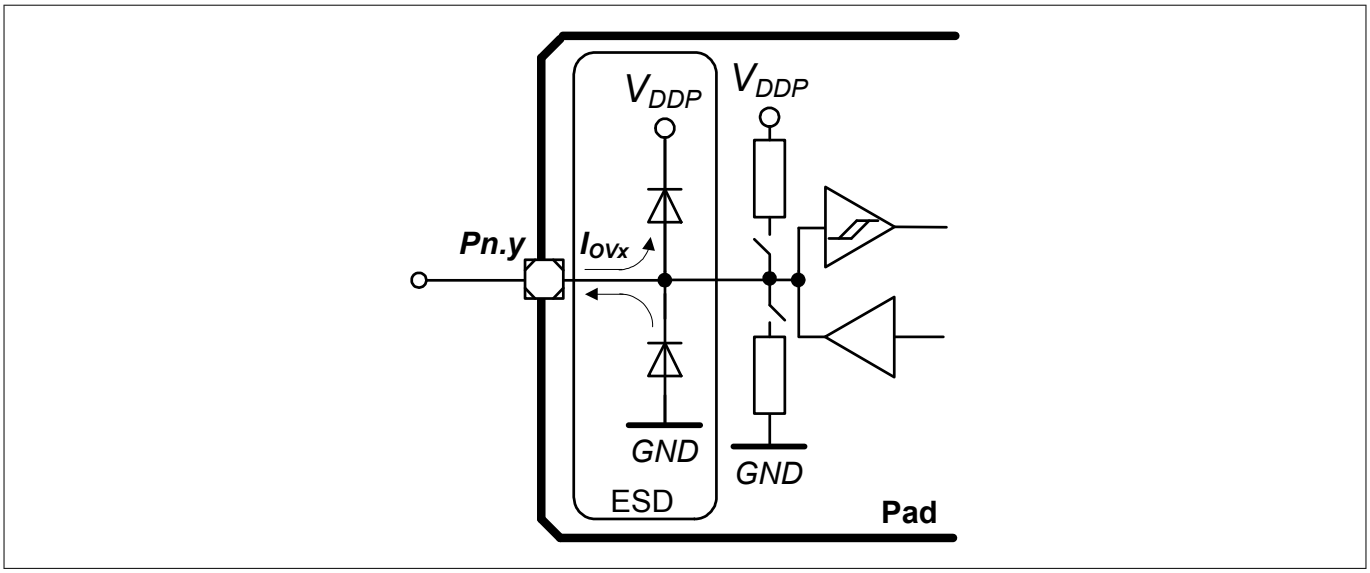

Figure 10 Input Overload Current via ESD structures

Table 5 and *Table 6* list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the *Absolute Maximum Ratings* must not be exceeded during overload.

Table 5 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP}$ +(0.3 ... 0.5) V $V_{AIN} = V_{DDP}$ + 0.5 V $V_{AREF} = V_{DDP}$ + 0.5 V

Table 6 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS}$ - (0.3 … 0.5) V $V_{AIN} = V_{SS}$ - 0.5 V $V_{AREF} = V_{SS}$ - 0.5 V

4.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the IMC100. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 7 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	105	°C	
Junction temperature	T_J SR	-40	–	115	°C	
Digital supply voltage[1)]	V_{DDP} SR	3.0	3.3	5.5	V	
Short circuit current of digital outputs[2)]	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device[3)]	ΣI_{SC_D} SR	–	–	25	mA	

1 See also the Supply Monitoring thresholds ***Power-Up and Supply Threshold Characteristics***.
2 Applicable for digital outputs.
3 See also section "Pin Reliability in Overload" for overload current definitions.

4.2 DC Parameters

4.2.1 Input/Output Characteristics

The table below provides the characteristics of the input/output pins of the IMC100.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Note: *Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.*

Table 8 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins	V_{OLP}	CC	–	1.0	V	I_{OL} = 11 mA (5 V) I_{OL} = 7 mA (3.3 V)
			–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output low voltage on PWM outputs	V_{OLP1}	CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
			–	0.32	V	I_{OL} = 10 mA (5 V)
			–	0.4	V	I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins	V_{OHP}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = -7 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4.5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on PWM outputs	V_{OHP1}	CC	V_{DDP} - 0.32	–	V	I_{OH} = -6 mA (5 V)
			V_{DDP} - 1.0	–	V	I_{OH} = -8 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4 mA (3.3 V)
Rise/fall time on PWM outputs[4)]	t_{HCPR}, t_{HCPF}	CC	–	9	ns	50 pF @ 5 V
			–	12	ns	50 pF @ 3.3 V
Rise/fall time on standard pad	t_R, t_F	CC	–	12	ns	50 pF @ 5 V
			–	15	ns	50 pF @ 3.3 V.
Pin capacitance (digital inputs/outputs)	C_{IO}	CC	–	10	pF	
Pull-up/-down resistor on port pins (if enabled in software)	R_{PUP}	CC	20	50	kΩ	$V_{IN} = V_{SSP}$

4 Rise/Fall time parameters are taken with 10% - 90% of supply.

Table 8 Input/Output Characteristics (Operating Conditions apply) (continued)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input leakage current [5)]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, T_A 105°C
Maximum current per pin standard pin	I_{MP}	SR	-10	11	mA	–
Maximum current per PWM outputs pins	I_{MP1A}	SR	-10	50	mA	–
Maximum current into V_{DDP} / out of V_{SS}	I_{MVDD} / I_{MVSS}	SR	–	260	mA	

5 An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

4.2.2 Analog to Digital Converter (ADC)

The following table shows the Analog to Digital Converter (ADC) characteristics. This specification applies to all analog input as given in the pin configuration list.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 9 ADC Characteristics (Operating Conditions apply)[6)]

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage range	V_{DD} SR	3.0	–	5.5	V	
Analog input voltage range	V_{AIN} SR	V_{SSP}- 0.05	–	V_{DDP}+ 0.05	V	
Conversion time	t_{C12} CC	–	1.0	1.6	µs	
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	
Sample time	t_{sample} CC	–	200	–	ns	
RMS noise	EN_{RMS} CC	–	1.5	–	LSB12	
DNL error	EA_{DNL} CC	–	±2.0	–	LSB12	
INL error	EA_{INL} CC	–	±4.0	–	LSB12	
Gain error	EA_{GAIN} CC	–	±0.5	–	%	V_{DD} = 3.3V
Offset error	EA_{OFF} CC	–	±8.0	–	mV	

6 All parameters are defined for the full supply range if not stated otherwise.

4.2.3 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 10 Power Supply parameter table; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Active mode current motor control only	I_{DDPWM} CC	–	10	20	mA	
Active mode current motor control plus PFC	I_{DDPFC} CC	–	14	20	mA	IMC102 only
Deep Sleep mode current[7)]	I_{DDPDS} CC	–	0.27	–	mA	
Wake-up time from Sleep to Active mode	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode	t_{DSA} CC	–	290	–	µsec	

4.2.4 Flash Memory Parameters

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 11 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Data Retention Time	t_{RET} CC	10			years	Max. 100 erase / program cycles
Erase Cycles[8)]	N_{ECYC} CC			$5*10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	N_{TECYC} CC			$2*10^6$	cycles	

7 CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.

8 Sum of page erase and sector erase cycles a page sees.

4.3 AC Parameters

4.3.1 Testing Waveforms

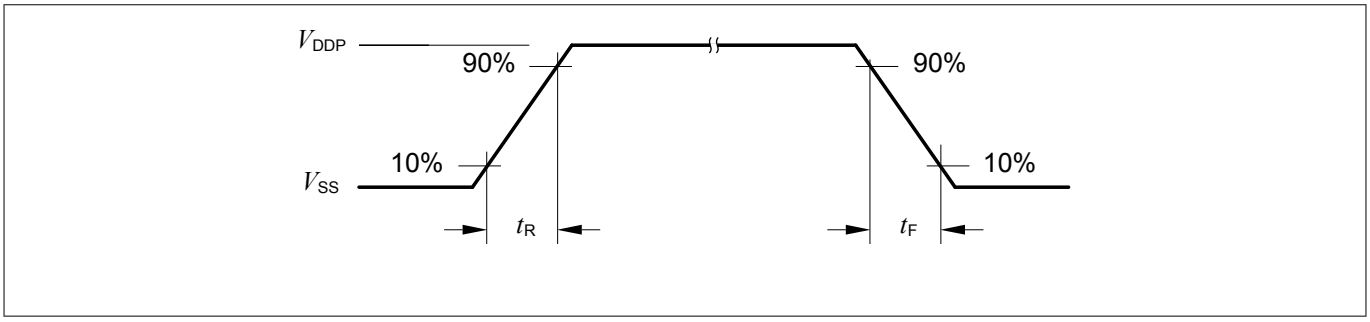

Figure 11 Rise/Fall Time Parameters

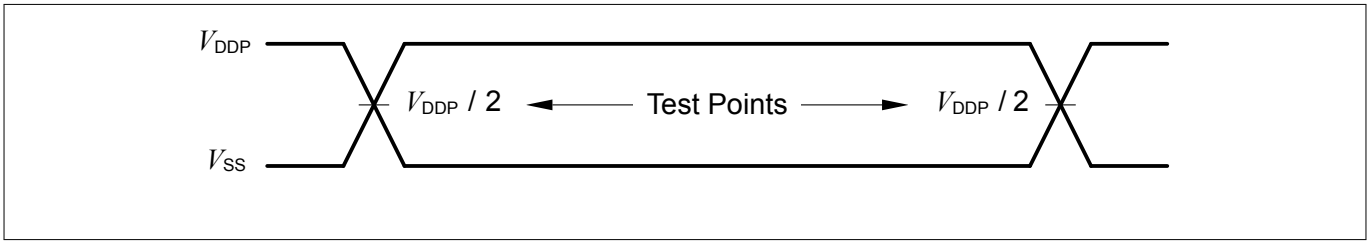

Figure 12 Testing Waveform, Output Delay

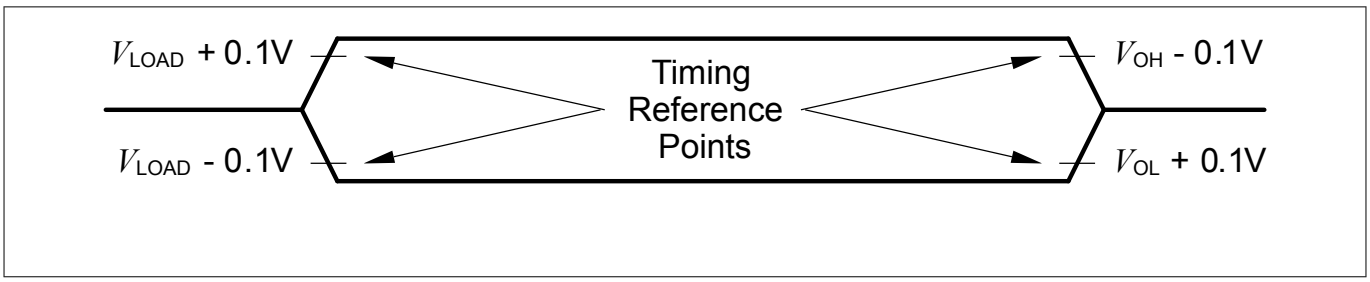

Figure 13 Testing Waveform, Output High Impedance

4.3.2 Power-Up and Supply Threshold Characteristics

This chapter provides the characteristics of the supply threshold in IMC100.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Note: *Operating Conditions apply.*

Table 12 Power-Up and Supply Threshold Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/-10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$ [9] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits [10]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B
V_{DDP} brownout reset voltage	V_{DDPBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	

9 A capacitor of at least 100 nF has to be added between VDDP and VSSP to fulfill the requirement as stated for this parameter.

10 Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

Table 12 Power-Up and Supply Threshold Parameters (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Start-up time from power-on reset	t_{SSW} CC	–	260	–	µs	Time to the first user code instruction[11)]
Start-up time to PWM on	t_{PWMON} CC	5.2	-	360	ms	Time to PWM enabled

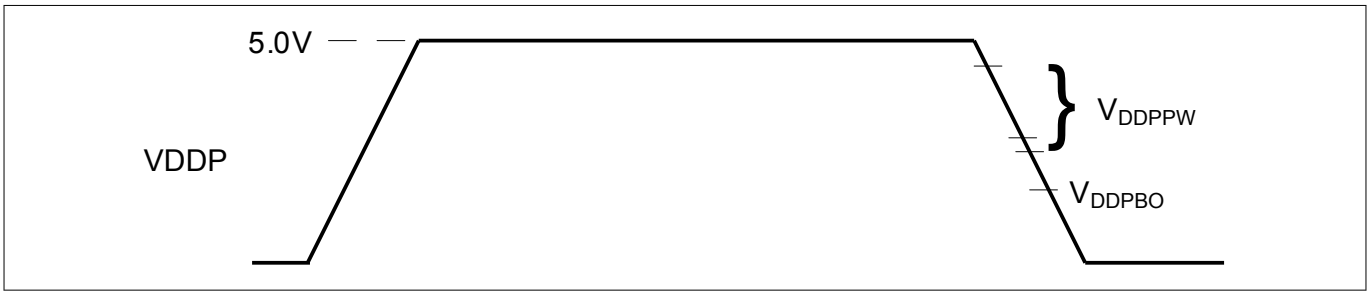

Figure 14 Supply Threshold Parameters

11 This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 48 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

4.3.3 On-Chip Oscillator Characteristics

Table 13 provides the characteristics of the 96 MHz digital controlled oscillator DCO1. The DCO1 is used as the time base during normal operation.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 13 96 MHz DCO1 Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Nominal frequency	f_{NOM} CC	95.7	96	96.3	MHz	under nominal conditions[12] after trimming
Short term frequency deviation (over V_{DDC})	Δf_{ST} CC	-1	–	1	%	with respect to f_{NOM} (typ), at 25°C
Accuracy	Δf_{LT} CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0°C to 85°C)
		-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40°C to 105°C)

Table 14 provides the characteristics of the 32 kHz digital controlled oscillator DCO2. The DCO2 is only used internally as a secondary clock source for the internal watchdog and as a fallback in case of failure of DCO1.

Table 14 32 kHz DCO2 Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Nominal frequency	f_{NOM} CC	32.5	32.75	33	kHz	under nominal conditions[13] after trimming
Short term frequency deviation (over V_{DDC})	Δf_{ST} CC	-1	–	1	%	with respect to f_{NOM}(typ), at 25°C
Accuracy	Δf_{LT} CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0°C to 85°C)
		-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40°C to 105°C)

12 The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25°C.
13 The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25°C.

4.4 Motor Control Parameters

The following parameters are defined in the iMOTION™ motion control engine (MCE) software.

4.4.1 PWM Characteristics

Table 15 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Motor PWM Frequency	f_{PWM}	5	16	20	kHz	

4.4.2 Current Sensing

Table 16 Motor Current Sensing

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input range	I_{PWM}	V_{SS}-0.05	-	V_{DD}+0.05	V	
Configurable analog gain		-	1/ 3/ 6/ 12	-		
Itrip input range	$I_{PWMTRIP}$	V_{SS}-0.05	-	V_{DD}+0.05	V	
Itrip offset		-	±8	-	mV	
Input capacitance	C_{REF}	-	-	10	pF	REFU, REFV, REFW capacitor

4.4.3 Fault Timing

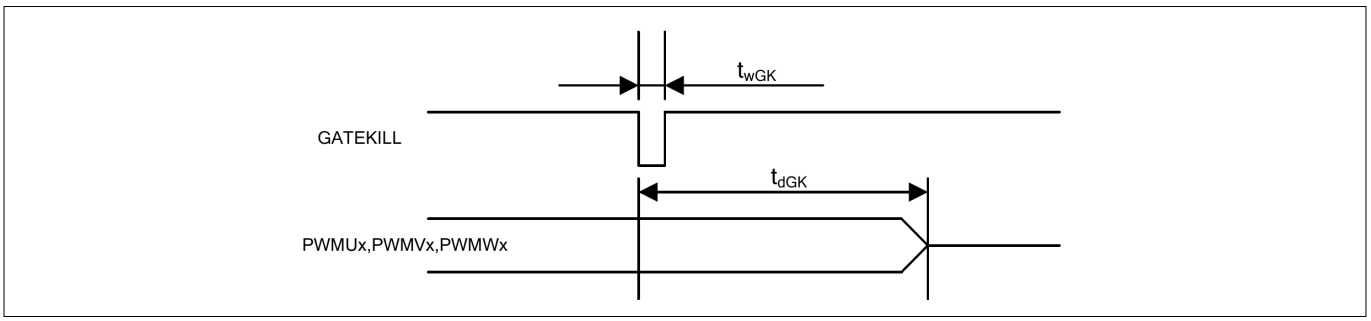

Figure 15 Fault timing

Table 17 Gatekill timing

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
GK pulse width	t_{wGK}	1	-	-	µs	
GK input to PWM shutoff	t_{GK}	-	1.3	-	µs	

Table 17 Gatekill timing (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Motor Fault reset timing	t_{RESET}	-	1.84	-	ms	fault reset command via UART to PWM reactivation
Itrip to PWM shutoff	t_{PWMOFF}	-	1.0	-	µs	single shunt
Itrip to PWM shutoff	t_{PWMOFF}	-	1.0	-	µs	leg shunt

4.5 Power Factor Correction (PFC) parameters

The parameters specified for the power factor correction only refer to the IMC102 with integrated PFC control algorithms.

4.5.1 Boost PFC characteristics

Table 18 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
PFC frequency	f_{PFC}	-	20	50	kHz	Motor PWM frequency within specified range

4.5.2 Totem Pole PFC characteristics

Table 19 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
PFC frequency	f_{PFC}	-	20	50	kHz	Motor PWM frequency within specified range

4.5.3 PFC Current Sensing

The current sensing specification applies to both PFC algorithms, boost mode and totem pole.

Table 20 PFC Current Sensing

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input range	I_{PFC}	V_{SS}- 0.05	-	V_{DD}+ 0.05	V	V_{DD}= 3.3 or 5.0 V
Configurable analog gain		-	1/ 3/ 6/ 12	-		
PFC Itrip input range	$I_{PFCTRIP}$	V_{SS}-0.05	-	V_{DD}+ 0.05	V	V_{DD}= 3.3 or 5.0 V
Itrip offset		-	± 3	-	mV	Input voltage difference > 200mV
Input capacitance	C_{REF}	-	-	10	pF	PFCREF capacitor

4.5.4 PFC Fault Timing

Table 21 PFC Fault timing

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Itrip to PFC PWM shutoff	t_{PFCOFF}	-	1.18	-	µs	
PFC fault reset timing	t_{RESET}	-	1.0	-	ms	fault reset command via UART to PWM reactivation

4.6 Control Interface Parameters

The following tables specify the interfaces that can be used to control the motor drive in the application.

4.6.1 Serial Interface Parameters

The IMC100 series provides the following communication interfaces.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

4.6.1.1 UART Interface

The UART interface is configured as given below.

Note: *Operating Conditions apply.*

Table 22 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
UART baud rate		1200	57600	-	Bps	
UART mode		-	8-N-1	-		data-parity-stop bit
UART sampling filter period [14)]	$T_{UARTFIL}$	-	1/16	-	T_{BAUD}	

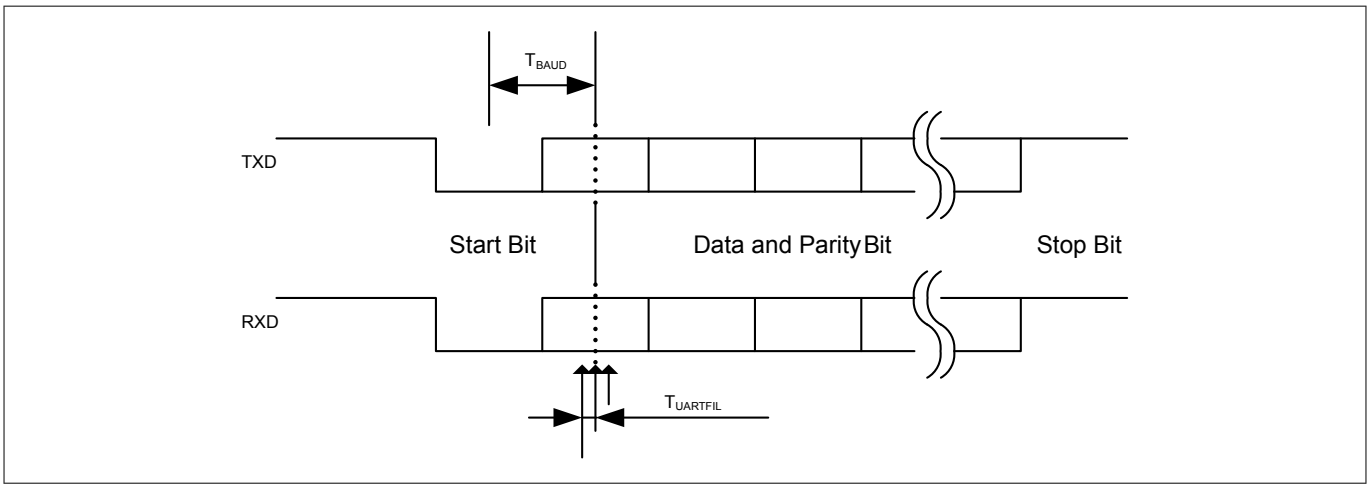

Figure 16 UART timing

14 Each bit including start and stop bit is sampled three times at center of a bit at an interval of 1/16 T_{BAUD}. If three sampled values do not agree, then UART noise error is generated.

4.6.2 Analog Speed Input

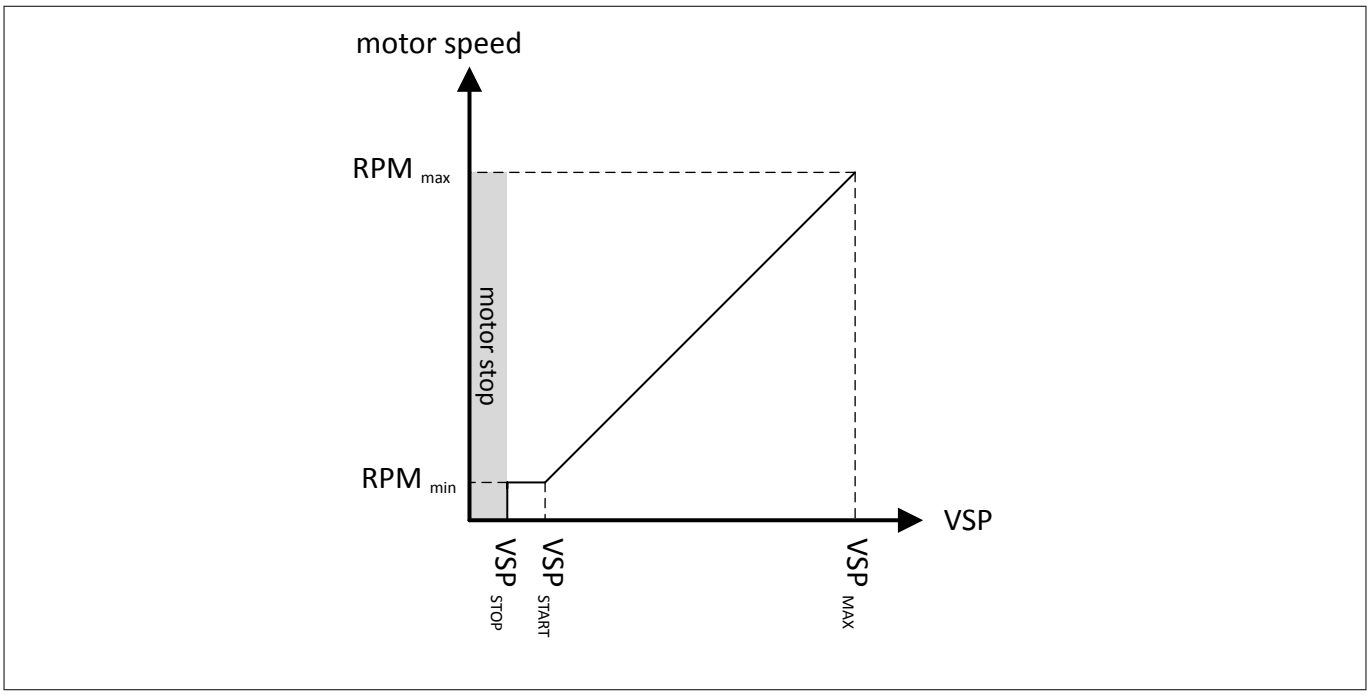

Figure 17 VSP analog control mode

Table 23 Analog Speed Control Voltage (VSP)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Motor start voltage	VSP_{START}	-	1.2	-	V	Configured VSP_{START}=1.0V
Motor stop voltage	VSP_{STOP}	-	1.0	-	V	Configured VSP_{STOP}=1.0V
Motor max voltage	VSP_{MAX}	-	4.9	4.95	V	V_{DD}=5.0V
VSP active to PWM start	t_{START}	-	44	-	ms	
VSP inactive to PWM stop	t_{STOP}	-	16	-	ms	

4.6.3 Frequency Input

In frequency input control mode, the motor operations like motor start, motor stop and speed change are controlled by applying a square wave frequency signal on a digital input pin.

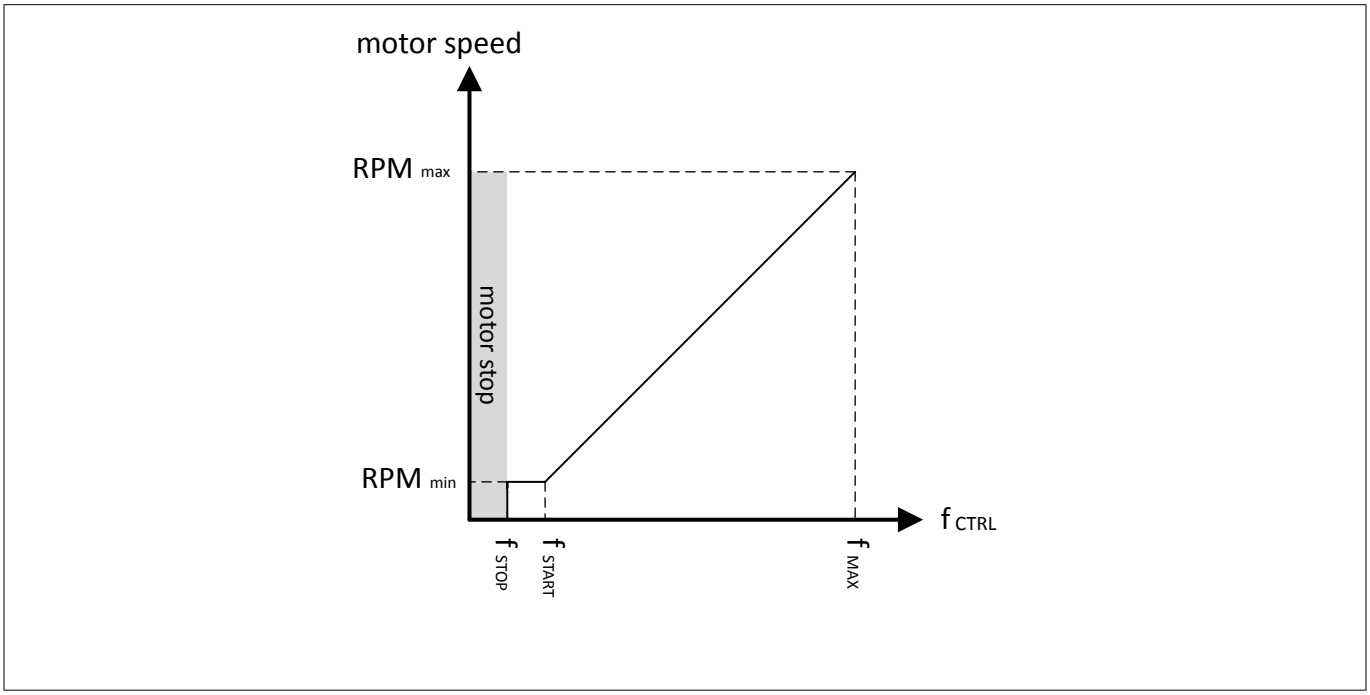

Figure 18 Frequency input control mode

Table 24 Frequency Control Mode

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Motor start frequency	f_{START}	-	100	360	Hz	$f_{START} > f_{STOP}$
Motor stop frequency	f_{STOP}	-	50	-	Hz	
Motor max speed frequency	f_{MAX}	-	-	1000	Hz	
Frequency input duty cycle	T_{DUTY}	10	-	90	%	

4.6.4 Duty Cycle Input

In duty cycle input control mode, the motor operations like motor start, stop and speed change are controlled by varying the duty cycle of a rectangular wave signal on a digital input pin.

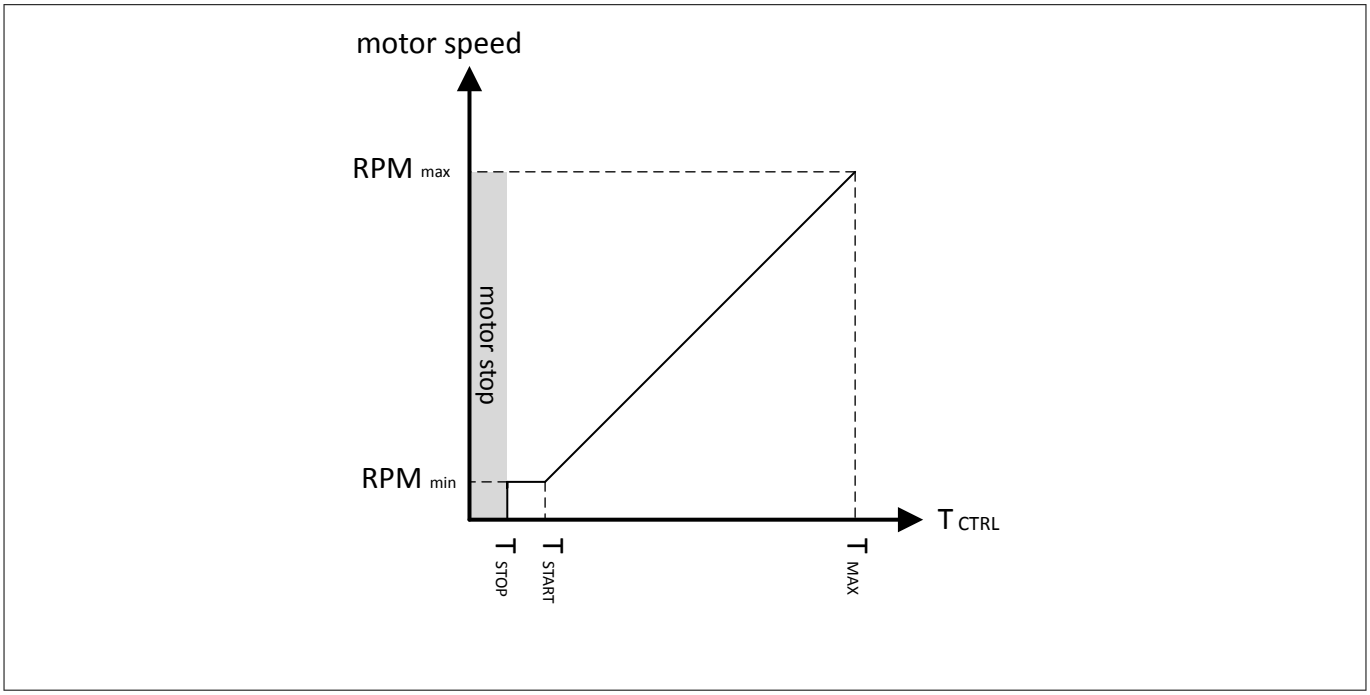

Figure 19 Duty cycle input control mode

Table 25 Duty Cycle Control Mode

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input signal frequency	f_{DUTY}	5	1000	20000	Hz	
Motor start duty cycle	T_{START}	-	10	-	%	$T_{START} > T_{STOP}$
Motor stop duty cycle	T_{STOP}	-	5	-	%	
Motor max duty cycle	T_{MAX}	-	95	-	%	

4.6.5 Over Temperature Input

The over temperature input can be used to continuously monitor an external temperature sensor like an NTC.

Table 26 Over Temperature Input

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Over Temperature Input Threshold	V_{OT}	0.1	1.0	3.0	V	V_{DD}=3.3V, Configurable parameter e.g. via MCEDesigner, default=1.0V
Over Temperature to PWM shutdown	t_{OT}		1.0	2.1	ms	

4.6.6 Pulse Output

The IMC100 series can generate a square wave pulse output in sync with the motor rotation which can be used to monitor the motor speed. The number of pulses to be generated for a full rotation can be configured.

Table 27 Pulse Output

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Pulses per Rotation	*PPR*	4	-	24		
Pulse duty cycle	t_{PPR}	-	50	-	%	

4.6.7 LED Output

The IMC100 series provides an output that can be connected to an LED to give a visual indication of the status of the motor drive.

Table 28 LED Output

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Fault to LED delay	$t_{LEDFAULT}$	-	53	-	ms	
Fault reset to LED delay	$t_{LEDRESET}$	-	1.84	-	ms	
LED blinking frequency	f_{LED}	1		1000	Hz	
LED blinking duty cycle	t_{LED}	5		95	%	

4.7 Quality Declaration

Table 29 shows the characteristics of the quality parameters in the IMC100.

Table 29 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	2000	V	Conforming to EIA/ JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	3	–	JEDEC J-STD-020C
Soldering temperature	T_{SDR} SR	–	260	°C	Profile according to JEDEC J-STD-020D

5 Package specification

5.1 Package Outlines

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: ***www.infineon.com/packages***

5.1.1 Package Outline PG-TSSOP-38-9

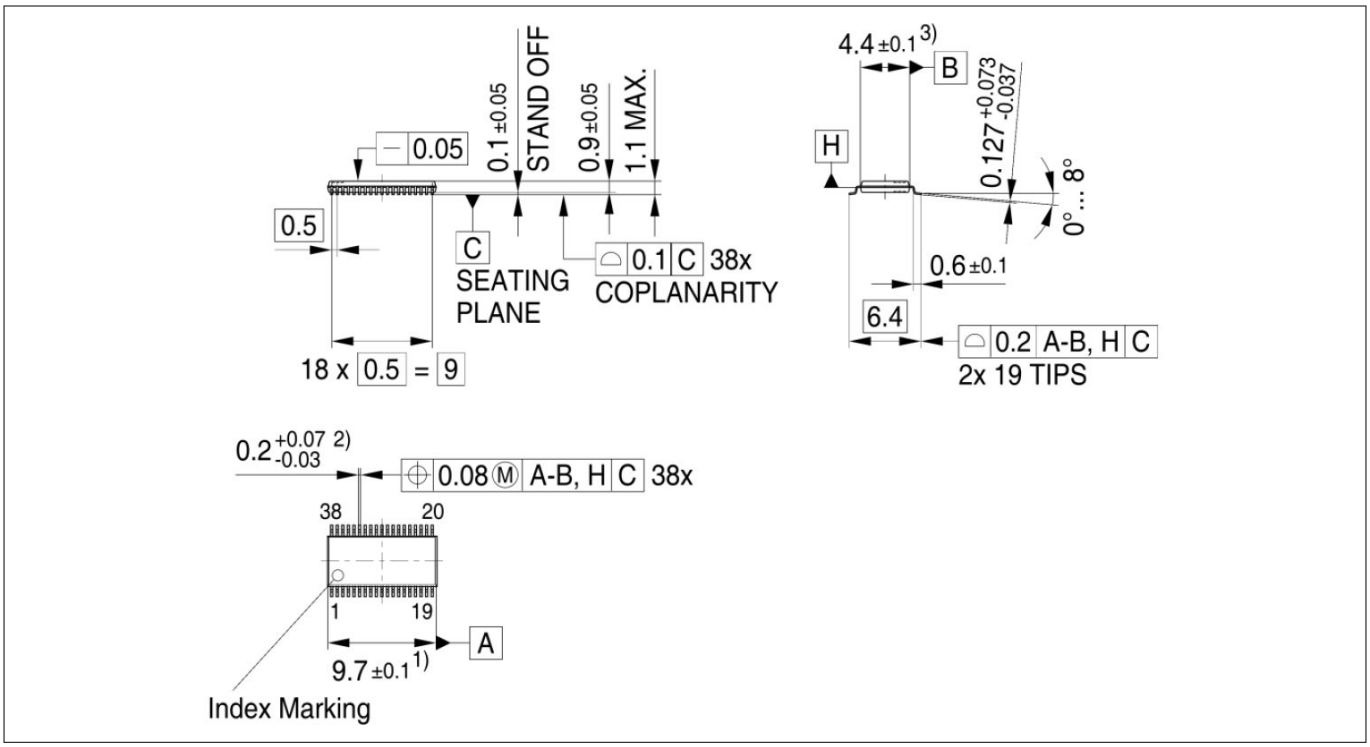

Figure 20 PG-TSSOP-38-9

5.1.2 Package Outline PG-VQFN-48-73

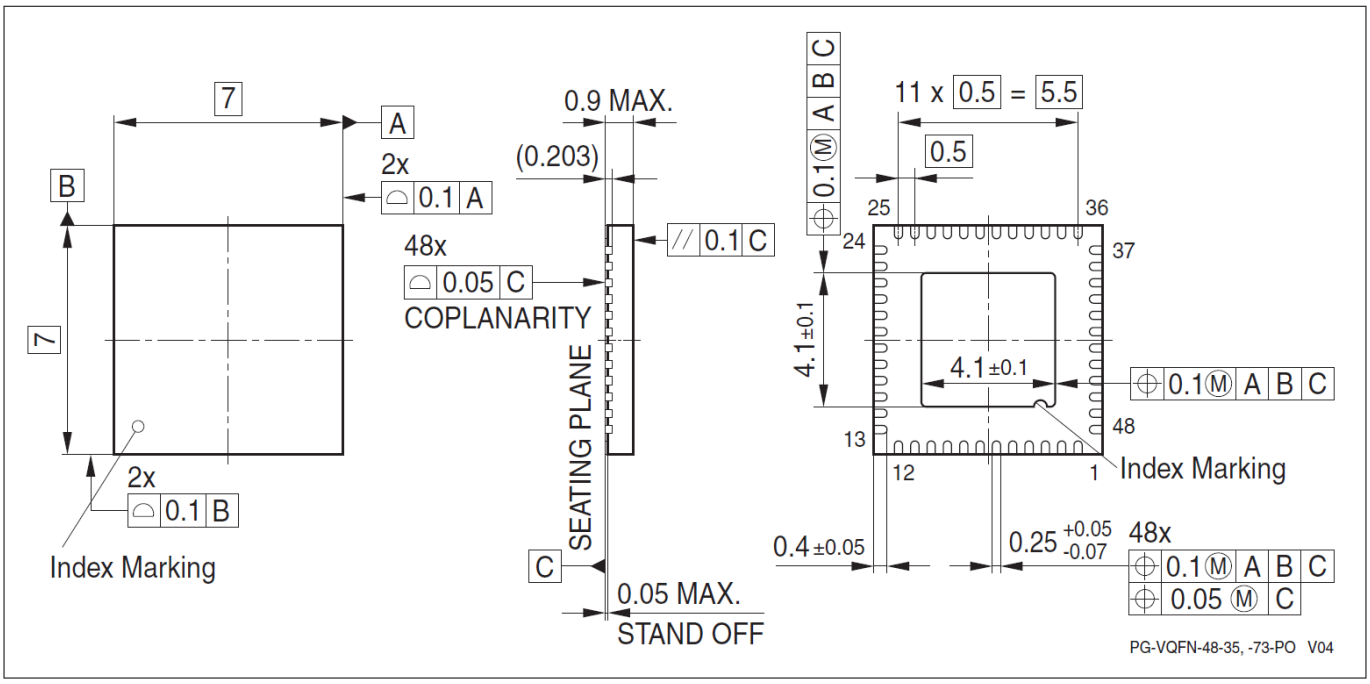

Figure 21 PG-VQFN-48-73

5.1.3 Package Outline PG-TQFP-48

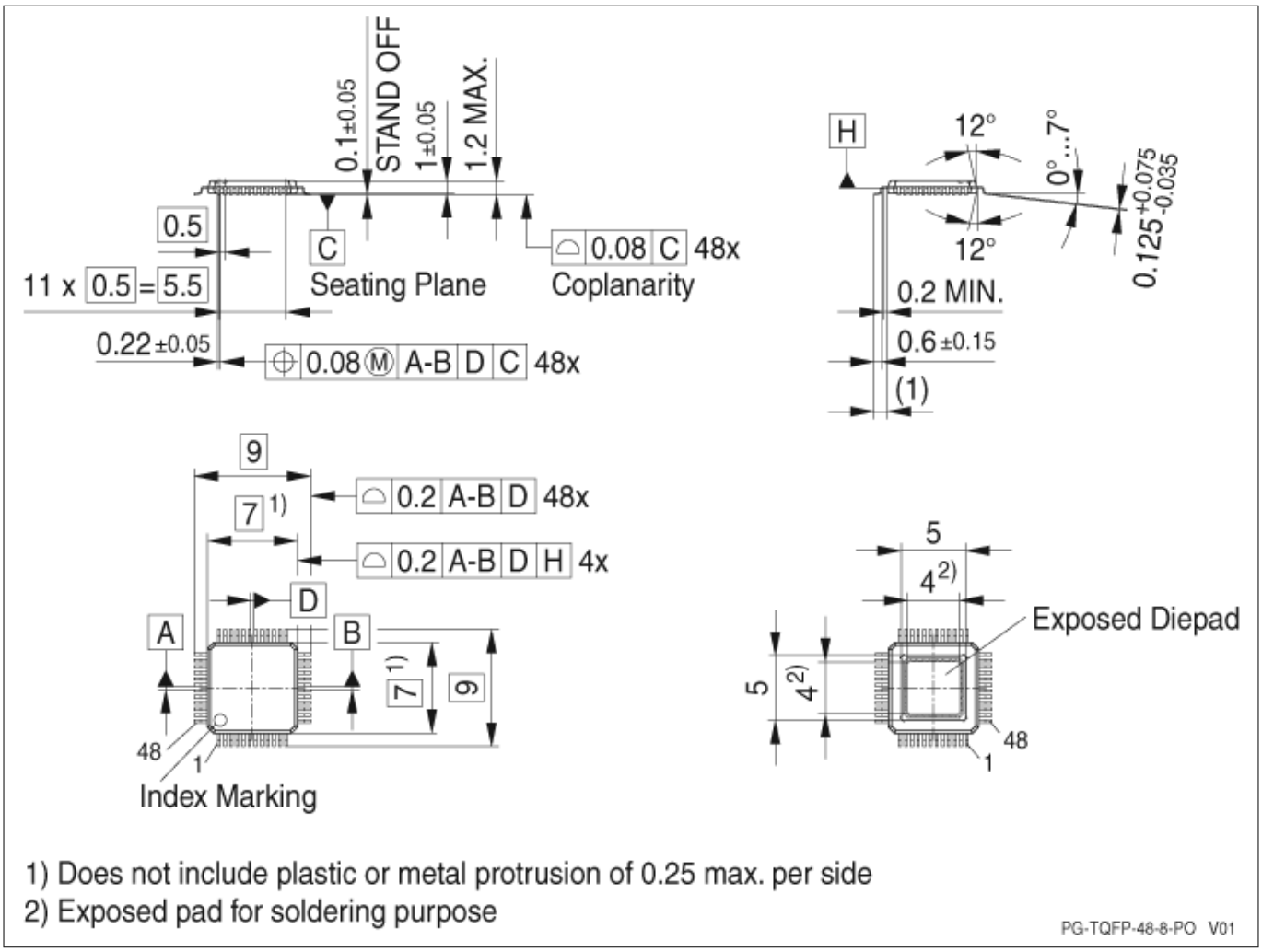

Figure 22 PG-TQFP-48

5.1.4 Package Outline PG-LQFP-64-26

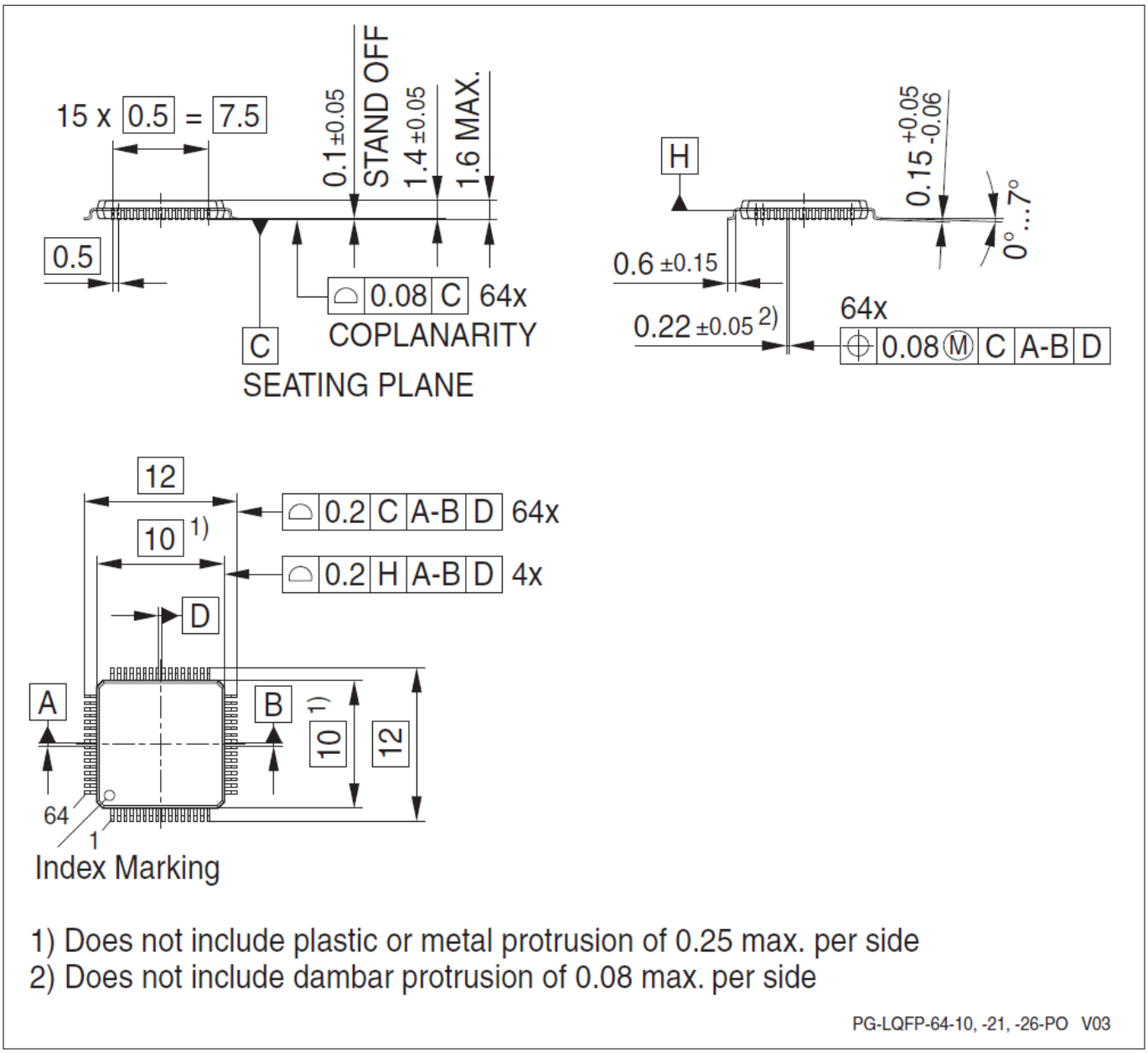

Figure 23 PG-LQFP-64-26

5.2 Thermal Considerations

Table 30 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	4.2 × 4.2	mm	PG-VQFN-48-73
Thermal resistance Junction-Ambient[1)]	$R_{\Theta JA}$ CC	-	86.0	K/W	PG-TSSOP-38-9
		-	44.9	K/W	PG-VQFN-48-73
		-	t.b.d.	K/W	PG-TQFP-48
			66.7	K/W	PG-LQFP-64-26

Note: *For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.*

When operating the IMC100 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115°C.

The difference between junction temperature and ambient temperature is determined by

$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as

$P_{IOSTAT} = \Sigma((V_{DDP} - V_{OH}) \times I_{OH}) + \Sigma(V_{OL} I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

1 Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad of VQFN soldered.

5.3 Part marking

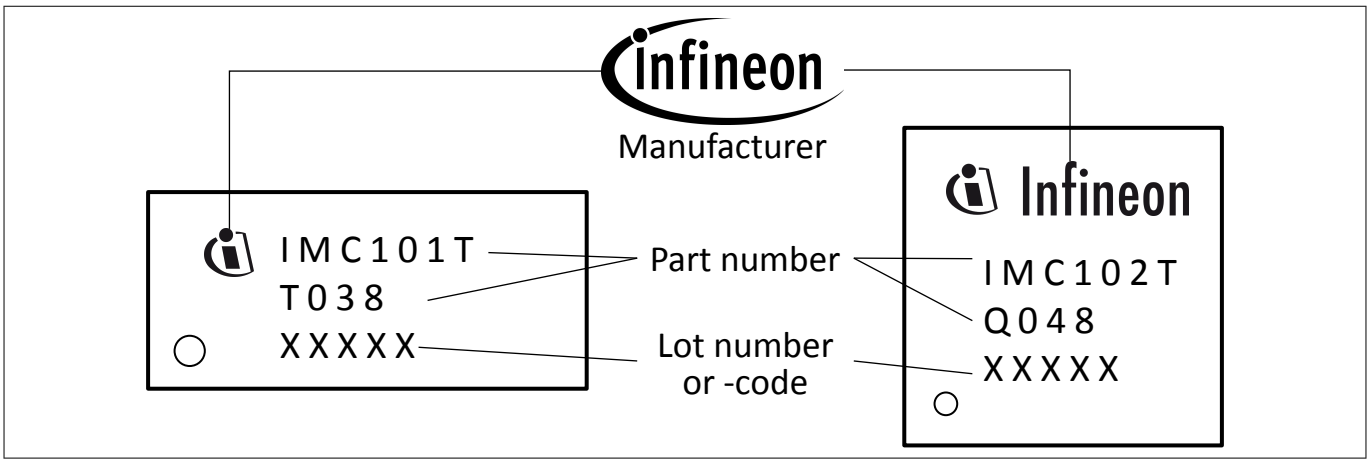

Figure 24 Part marking

6 References

Revision history

Document version	Date of release	Description of changes
1.0	2018-02-09	• Initial version
1.1	2018-02-20	• corrected RX1, TX1 in QFN-48, QFP-48 and LQFP-64

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Edition 2018-02-20

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-utn1491921304081

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