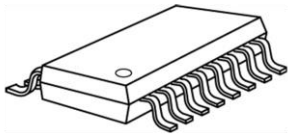
PWM-Embedded 3-Channel Constant Current LED Sink Driver for Small RGB Cluster

Features

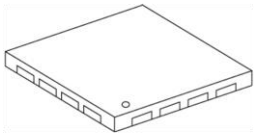
- 3-channel constant current sink driver for RGB LED clusters
- Constant current range 5~50mA
- Individual output current adjusted through external resistors
- Sustaining voltage at output channels: 17V (max.)
- Supply voltage 3V~5.5V
- Embedded 16-bit PWM generator
  - Gray scale clock generated by the embedded oscillator
  - PWM counter reset function
  - S-PWM technology
- Two selectable gray scale modes
  - 16-bit gray scale mode (with optional 8-bit dot correction)
  - 10-bit gray scale mode (with optional 6-bit dot correction)
- Reliable data transmission
  - Daisy-chain topology
  - Two-wire only transmission interface
  - Clock reverse
  - Built-in buffer for long-distance transmission
- Flexible operation modes
  - Auto-synchronization mode
  - Manual-synchronization mode
- Selectable polarity reversion to drive high-power drivers or MOS
- RoHS-compliant packages

Shrink SOP



GP: SSOP16L-150-0.64

QFN



GFN: QFN16L-3*3-0.5

Application

- Architecture decorative lighting
- Mesh display, LED strip
- Neon lamp alternative
- PWM generator

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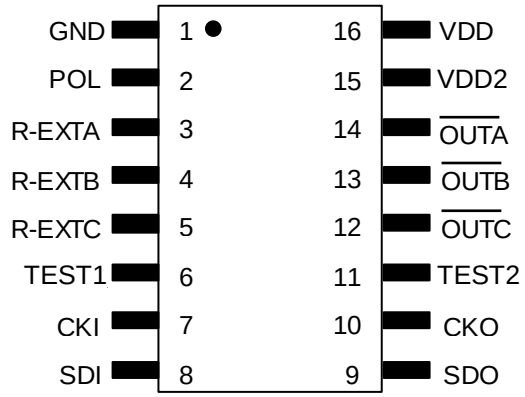
Product Description

MBI6020 is a 3-channel, constant current, PWM-embedded LED sink driver for small RGB LED cluster. MBI6020 provides constant current ranging from 5mA to 50mA for each output channel and three output channels are adjustable with three corresponding external resistors. Besides, MBI6020 can support both 3.3V and 5V power systems and sustain 17V at output channels.

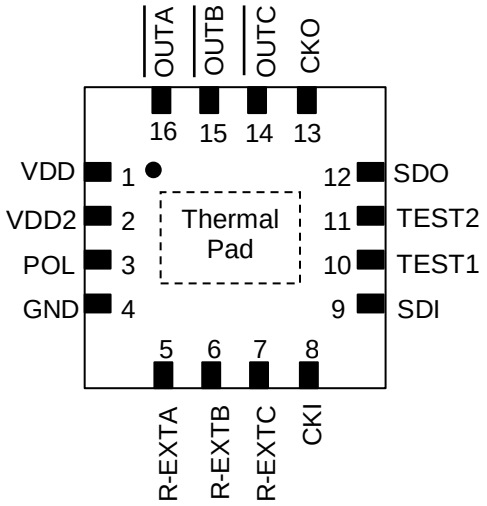
With Scrambled-PWM (S-PWM) technology, MBI6020 enhances pulse width modulation by scrambling the “on” time into several “on” periods, so that MBI6020 reduces the data transmission bandwidth at the same gray scale performance. The gray scale clock, GCLK, is generated by the embedded oscillator. Moreover, MBI6020 provides two selectable gray scale modes: 16-bit gray scale mode and 10-bit gray scale mode. The 16-bit gray scale mode provides 65,536 gray scales for each LED to enrich the color with optional 8-bit dot correction to adjust each LED by 256-step dot correction to calibrate the LED brightness. On the other hand, the 10-bit gray scale mode provides 1,024 gray scales with optional 6-bit dot correction to adjust each LED by 64-step dot correction.

Furthermore, MBI6020 features a two-wire only transmission interface to simplify the system controller design. To improve the transmission quality, MBI6020 provides clock reverse function to enhance long-distance transmission. MBI6020 is flexible for either auto-synchronization or manual-synchronization. In addition, MBI6020 preserves selectable polarity reversion to drive high-power drivers or MOS as a PWM controller.

Pin Configuration



MBI6020GP
Top View



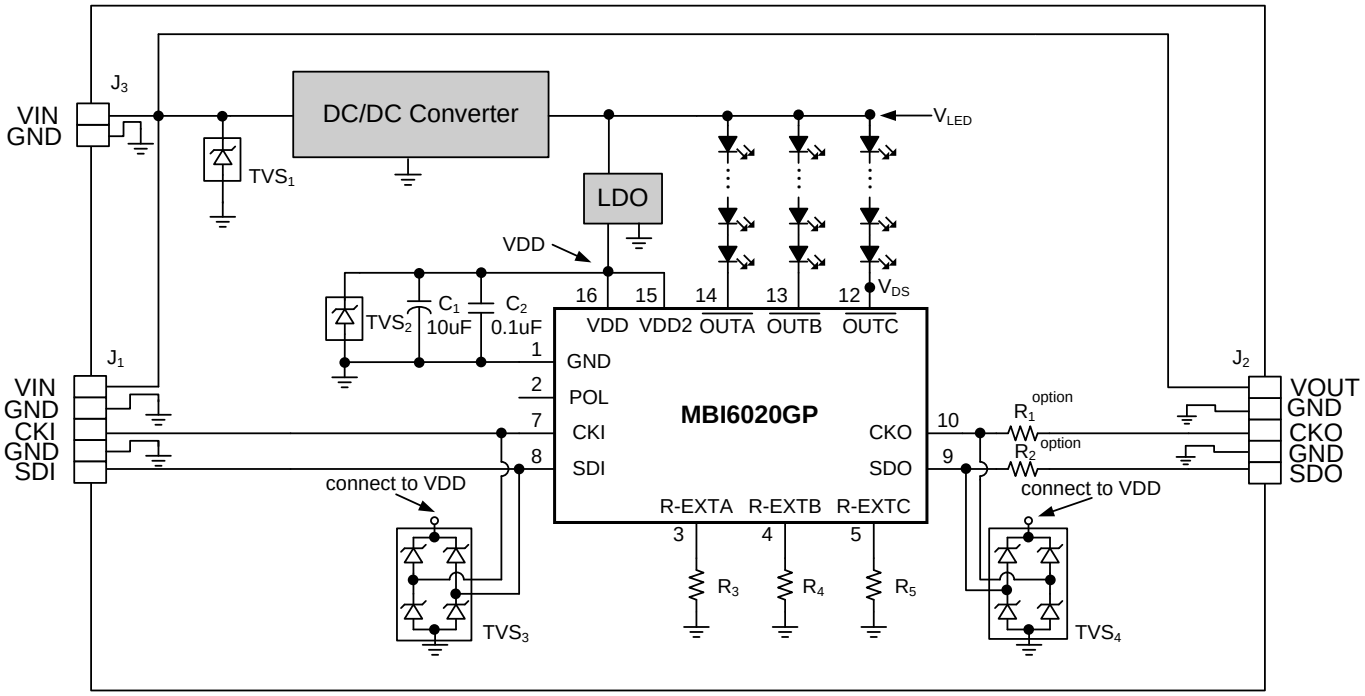
MBI6020GFN
Top View

Terminal Description

Pin		Name	Function
GP	GFN		
1	4	GND	Ground terminal
2	3	POL	Input terminal for selecting output polarity Internal pull-high High: drive LED or low-active regulators or PMOS Low: output reversed to work as a PWM controller to drive high-active regulators or NMOS
3,4,5	5,6,7	R-EXTA,B,C	Input terminals for setting output current by connecting to an external resistor
14,13,12	16,15,14	$\overline{\text{OUTA,B,C}}$	Output terminals for constant current output
6	10	TEST1	Test pin 1 (Default: pull-low)
11	11	TEST2	Test pin 2 (Default: pull-low)
7	8	CKI	Input terminal for clock input
8	9	SDI	Input terminal for serial data input
10	13	CKO	Output terminal for clock output
9	12	SDO	Output terminal for serial data output
15	2	VDD2	Internal pull-high to VDD 3.3V/5V supply voltage terminal
16	1	VDD	3.3V/5V supply voltage terminal
-	-	Thermal Pad	Heat dissipation pad* Please connect to GND.

*The desired thermal conductivity will be improved on condition that a heat-conducting copper foil on PCB is soldered with thermal pad.

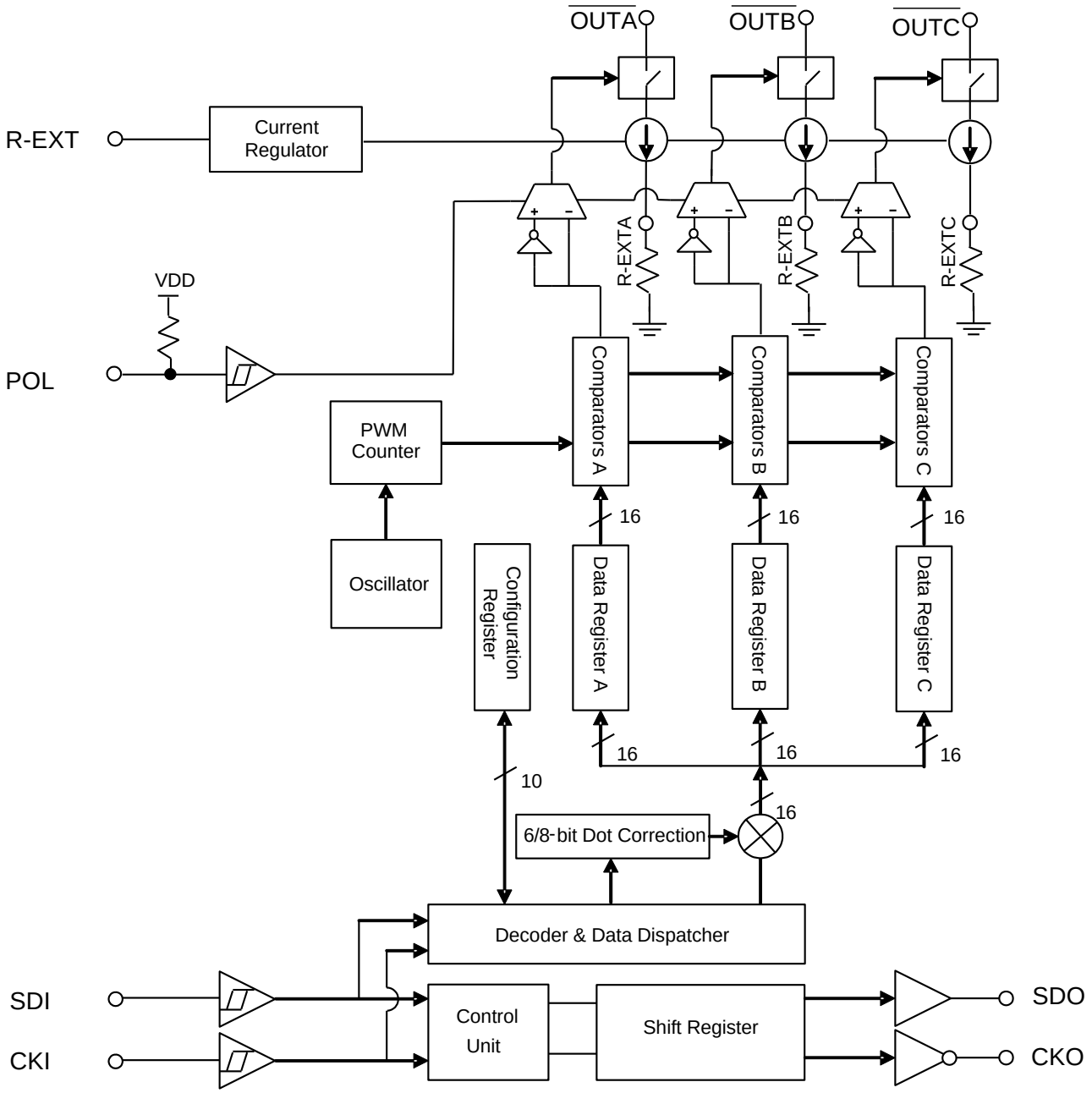
Typical Application Circuit



Note:

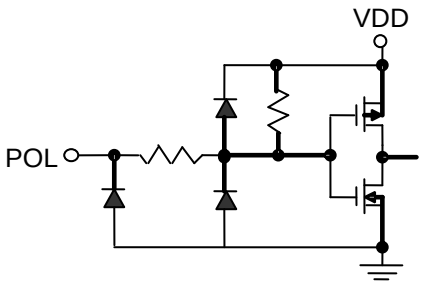
1. TVS_1~TVS_4 are Transient Voltage Suppressor (TVS) for overshoot/undershoot/ESD protection.
2. C_1~C_2 are required. The values of the C_1~C_2 are reference only. Tantalum capacitors and Ceramic capacitors are recommended.
3. About further information of hot swapping, system grounding, connector design, external ESD protection, or detailed circuit information, please refer to the latest version of ***"MBI6020 Application Note"***.

Block Diagram

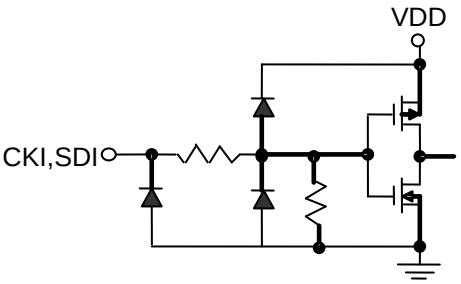


Equivalent Circuits of Inputs and Outputs

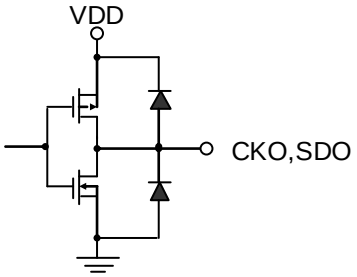
POL terminal



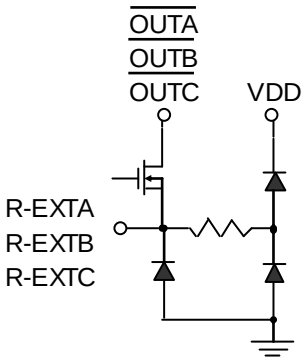
CKI, SDI terminal



CKO, SDO terminal



R-EXTA,B,C, $\overline{\text{OUTA,B,C}}$ terminal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7	V
Sustaining Voltage at CKI, SDI, POL Pins		V_{IN}	-0.4~V_{DD}+0.4	V
Sustaining Voltage at CKO, SDO Pins		V_{OUT}	-0.4~V_{DD}+0.4	V
Sustaining Voltage at $\overline{OUTA}$ ~ $\overline{OUTC}$		V_{DS}	-0.5~+17	V
Output Current per Output Channel		I_{OUT}	+50	mA
GND Terminal Current		I_{GND}	160	mA
Power Dissipation (On 4 Layer PCB, Ta=25°C)*	GP	P_D	1.66	W
	GFN		2.48	W
Thermal Resistance (By simulation, on 4 Layer PCB)*	GP	$R_{th(j-a)}$	75.33	°C/W
	GFN		50.31	°C/W
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	Human Body Mode (MIL-STD-883G Method 3015.7)	HBM	Class 3A (4000V~7999V)	-
	Machine Mode (JEDEC EIA/JESD22-A115)	MM	Class C (≧400V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. Users should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V, Ta=25˚C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUTA}$ ~ $\overline{OUTC}$=Off		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		5	-	50	mA
Driving Current		I_{OH}	CKO, SDO at V_{OH}=4.8V		2.0	2.5	3.8	mA
		I_{OL}	CKO, SDO at V_{OH}=0.2V		2.0	2.5	4.3	mA
Output Leakage Current		I_{OUT}	V_{DS}=17.0V and channel =off		-	-	1.0	μA
Current Skew (Channel)		dI_{OUT}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=20Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=20Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.5	%/V
Output Current vs. Supply Voltage Regulation*		$\%/dV_{DD}$	V_{DD} within 4.5V and5.5V		-	±1.0	±2.0	%/V
Input Voltage of CKI, SDI, POL Pins	"H" level	V_{IH}	-		0.73xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	-		GND	-	0.28xV_{DD}	V
Output Voltage of CKO, SDO Pins	"H" level	V_{OH}	I_{OH}=-2.5mA		V_{DD}-0.2	-	-	V
	"L" level	V_{OL}	I_{OL}=+2.5mA		-	-	0.2	V
Voltage at R-EXTA,B,C Pins		V_{REXT}	$\overline{OUTA}$ ~ $\overline{OUTC}$ =On		0.36	0.41	0.44	V
Knee Voltage		V_{Knee}	R_{ext}=8Ω@50mA		0.75	0.85	1.00	V
Pull-up Resistor at POL Pin		R_{IN}(up)	-		-	470	-	KΩ
Pull-down Resistor at TEST1, TEST2 Pins		R_{IN}(down)	-		-	470	-	KΩ
Supply Current**	"Off"	I_{DD}(off)	R_{ext}=10Ω, CKI=Low, CKO, SDO= NC, $\overline{OUTA}$ ~ $\overline{OUTC}$ =Off		-	2.0	3.5	mA
	"On"	I_{DD}(on)	R_{ext}=20Ω, CKI=Low, CKO, SDO= NC, $\overline{OUTA}$ ~ $\overline{OUTC}$ =On		-	3.0	4.0	
			R_{ext}=20Ω, CKI=10MHz, CKO, SDO= NC, $\overline{OUTA}$ ~ $\overline{OUTC}$= On		-	5.0	6.0	

*One channel turns on.

** The supply current may vary with the loading conditions.

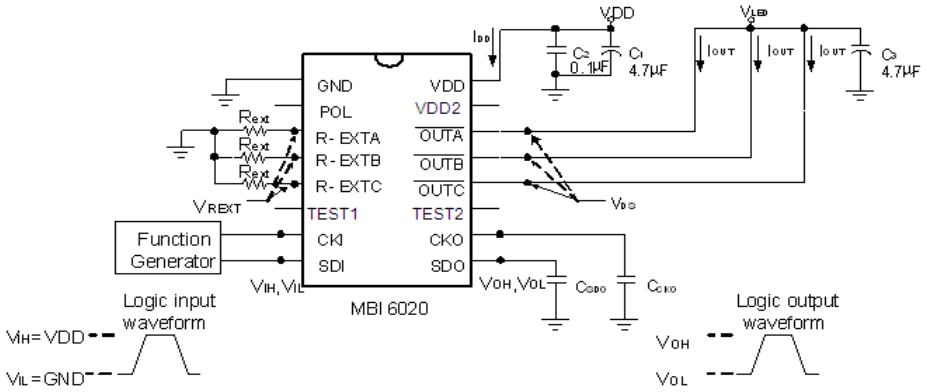
Electrical Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-	3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUTA}$ ~ $\overline{OUTC}$=Off	-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"	5	-	50	mA
Driving Current		I_{OH}	CKO, SDO at V_{OH}=3.1V	1.8	2.0	2.8	mA
		I_{OL}	CKO, SDO at V_{OH}=0.2V	1.8	2.0	3.4	mA
Output Leakage Current		I_{OUT}	V_{DS}=17.0V and channel =off	-	-	1.0	μA
Current Skew (Channel)		dI_{OUT}	I_{OUT}=20mA, V_{DS}=1.0V, R_{ext}=20Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA, V_{DS}=1.0V, R_{ext}=20Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V	-	±0.1	±0.5	%/V
Output Current vs. Supply Voltage Regulation*		$\%/dV_{DD}$	V_{DD} within 2.7V and 3.6V	-	±1.0	±2.0	%/V
Input Voltage of CKI, SDI, POL Pins	"H" level	V_{IH}	-	0.73xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	-	GND	-	0.28xV_{DD}	V
Output Voltage of CKO, SDO Pins	"H" level	V_{OH}	I_{OH}=-2.0mA	V_{DD}-0.2	-	-	V
	"L" level	V_{OL}	I_{OL}=+2.0mA	-	-	0.2	V
Voltage at R-EXTA,B,C Pins		V_{REXT}	$\overline{OUTA}$ ~ $\overline{OUTC}$ =On	0.36	0.41	0.44	V
Knee Voltage		V_{Knee}	R_{ext}=8Ω@50mA	0.75	0.85	1.00	V
Pull-up Resistor at POL Pin		R_{IN}(up)	-	-	450	-	KΩ
Pull-down Resistor at TEST1, TEST2 Pins		R_{IN}(down)	-	-	450	-	KΩ
Supply Current**	"Off"	I_{DD}(off)	R_{ext}=10Ω, CKI=Low, CKO, SDO= NC, $\overline{OUTA}$ ~ $\overline{OUTC}$ =Off	-	2.0	3.5	mA
	"On"	I_{DD}(on)	R_{ext}=20Ω, CKI=Low, CKO, SDO= NC, $\overline{OUTA}$ ~ $\overline{OUTC}$ =On	-	2.5	3.5	
			R_{ext}=20Ω, CKI=10MHz, CKO, SDO= NC, $\overline{OUTA}$ ~ $\overline{OUTC}$= On	-	4.0	5.0	

*One channel turns on.

**The supply current may vary with the loading conditions.

Test Circuit for Electrical Characteristics



Switching Characteristics (V_{DD}=5.0V, Ta=25˚C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI–CKI↓	t_{SU}	V_{LED}=4V V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND I_{OUT}=20mA R_L=150Ω C_L=10pF C1=4.7uF C2=0.1uF C3=4.7uF C_{CKO}=8pF C_{SDO}=8pF	7.5	-	-	ns
Hold Time	CKI↓–SDI	t_{HD}		7.5	-	-	ns
Propagation Delay Time (“H” to “L”)	CKI↑–CKO↓	t_{PHL1}		25	30	35	ns
	GCLK↑–$\overline{OUTA}$↓	t_{PHL3}		25	36	46	ns
Propagation Delay Time (“L” to “H”)	SDO↑↓-CKO↑	t_{PHL2}		7	10	14	ns
Staggered Delay of Output	$\overline{OUTA}$~$\overline{OUTB}$	t_{SD}		-	5	-	ns
	$\overline{OUTB}$~$\overline{OUTC}$	t_{SD}		-	5	-	ns
Pulse Width	CKI*	$t_{W(I)}$		15	-	-	ns
Minimum Pulse Width of PWM	$\overline{OUTA}$~$\overline{OUTC}$	t_{WDM}		30	35	40	ns
Rise Time	CKO–SDO	t_{OR}		2	6	10	ns
	$\overline{OUTA}$~$\overline{OUTC}$	t_{OR1}		6.0	11.0	16.0	ns
Fall Time	CKO–SDO	t_{OF}		2	6	10	ns
	$\overline{OUTA}$~$\overline{OUTC}$	t_{OF1}		15	20	25	ns
Frequency	CKI*	F_{CKI}		0.2	-	10	MHz
	GCLK	F_{GCLK}		-	-	20	
	Internal Oscillator	F_{OSC}		18.0	20.0	22.0	

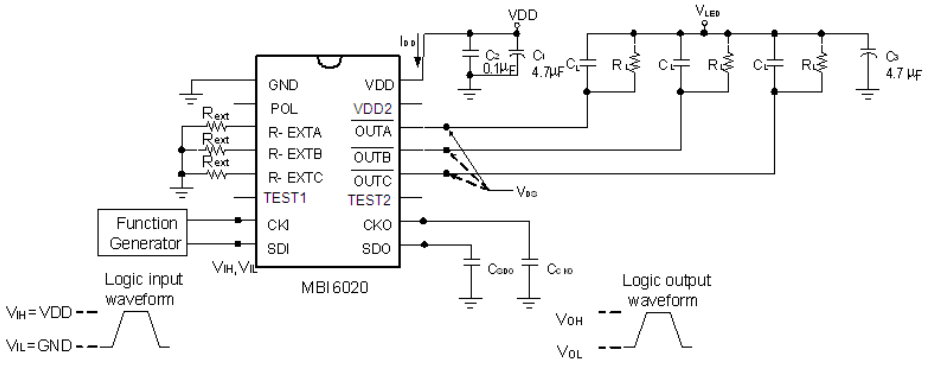
*The maximum frequency may be limited by different application conditions. Please refer to the application note for details.

Switching Characteristics (V_{DD}=3.3V, Ta=25˚C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	CKI↓–SDI	t_{SU}	V_{LED}=4V V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND I_{OUT}=20mA R_L=150Ω C_L=10pF C1=4.7uF C2=0.1uF C3=4.7uF C_{CKO}=8pF C_{SDO}=8pF	7.5	-	-	ns
Hold Time	SDI–CKI↓	t_{HD}		7.5	-	-	ns
Propagation Delay Time (“H” to “L”)	CKI↑–CKO↓	t_{PHL1}		40	45	50	ns
	GCLK↑–$\overline{OUTA}$↓	t_{PHL3}		30	42	54	ns
Propagation Delay Time (“L” to “H”)	SDO↑↓-CKO↑	t_{PHL2}		8	12	16	ns
Staggered Delay of Output	$\overline{OUTA}$ ~ $\overline{OUTB}$	t_{SD}		-	8	-	ns
	$\overline{OUTB}$ ~ $\overline{OUTC}$	t_{SD}		-	8	-	ns
Pulse Width	CKI	$t_{W(I)}$		15	-	-	ns
Minimum Pulse Width of PWM	$\overline{OUTA}$ ~ $\overline{OUTC}$	t_{WDM}		40	55	70	ns
Rise Time	CKO–SDO	t_{OR}		4	10	15	ns
	$\overline{OUTA}$ ~ $\overline{OUTC}$	t_{OR1}		13.0	20.0	25.0	ns
Fall Time	CKO–SDO	t_{OF}		4	10	15	ns
	$\overline{OUTA}$ ~ $\overline{OUTC}$	t_{OF1}		20.0	25.0	30.0	ns
Frequency	CKI*	F_{CKI}		0.2	-	10	MHz
	GCLK	F_{GCLK}		-	-	20	
	Internal Oscillator	F_{OSC}		18.0	20.0	22.0	

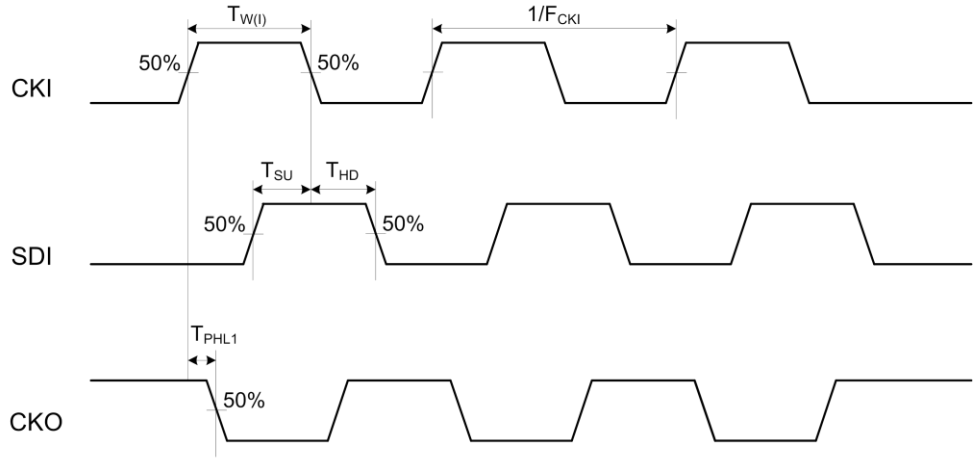
*The maximum frequency may be limited by different application conditions. Please refer to the application note for details.

Test Circuit for Switching Characteristics

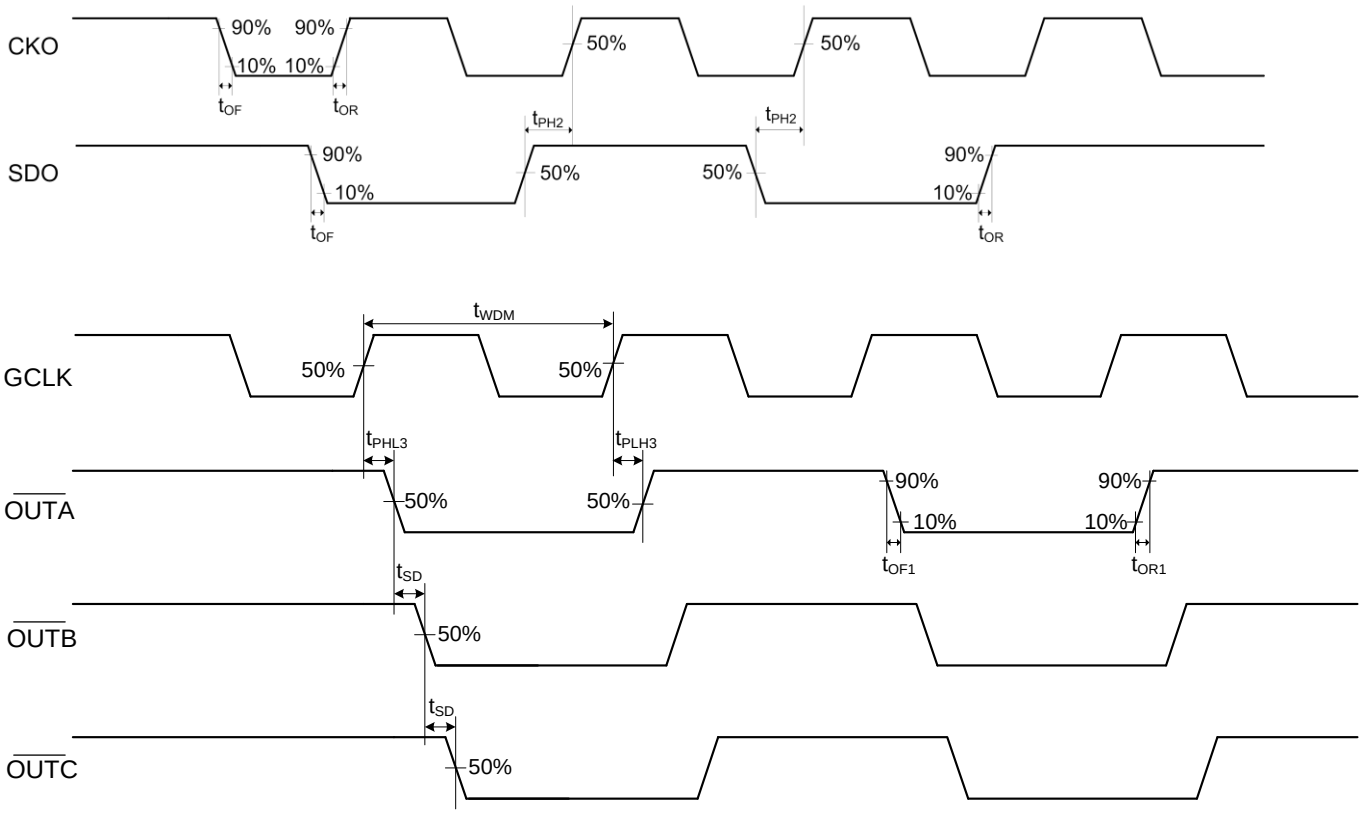


Timing Waveform

Signal Input and Output with Clock Reverse



Output Timing



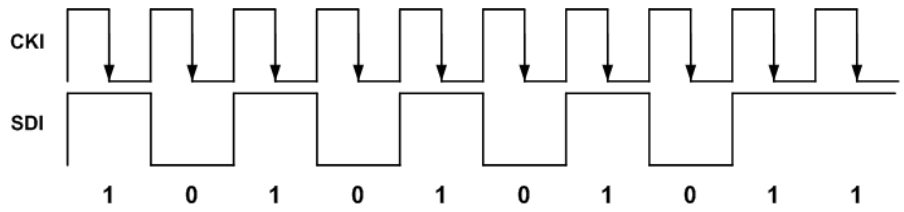
Principle of Operation

MBI6020 receives the data packet containing targeted gray scale data from the controller, and turns on the output channels according to the gray scale data. The gray scale clock of PWM generator, GCLK, is generated by the embedded oscillator. MBI6020 provides SPI-like interface (CKI, SDI), a two-wire only transmission interface, to address the data, so that MBI6020 receives the data directly without latching data. The sequence of operation should follow the steps below:

Step 1. Set the configuration register
Step 2. Send the dot correction data
Step 3. Send the gray scale data

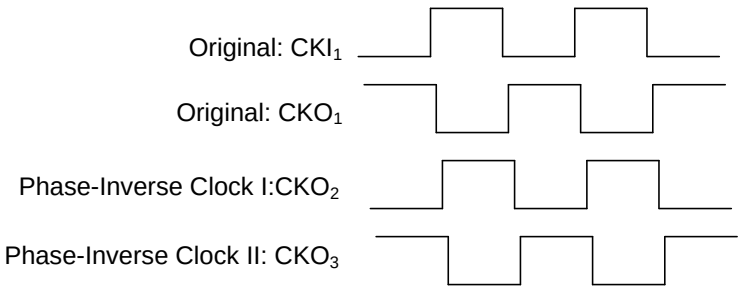
Control Interface: SPI-Like Interface (CKI, SDI)

MBI6020 adopts the SPI-like interface (CKI/SDI). By SPI-like interface, MBI6020 samples the data (SDI) at the falling edge of the clock (CKI).The following waveforms is the example of the SPI-like interface.



Phase-inversed Output Clock

MBI6020 enhances the capability of cascading MBI6020 by phase-inversed output clock function. By phase-inversed output clock, the clock phase will be inversed from CKI to CKO to eliminate the accumulation of the pulse width deviation. This improves the signal integrity of data transmission. The following chart illustrates the phase-inversed output clock results.



The Structure of Data Packet

MBI6020's data packet contains three parts:

1. Prefix:
   The prefix is a symbol of "Silent-to-Reset", i.e. a time period for MBI6020 to distinguish two data packets. During the prefix, both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.
2. Preamble:
   The preamble defines the cascaded IC numbers and also contains a command to decide the data type.
3. Data:
   This is the data for each IC. It may be gray scale data, dot correction data, or configuration data.

Structure of a data packet:

Prefix	Preamble	Data

Setting the Data Types by the Header

MBI6020 provides six kinds of headers and input data types shown as the table below:

Header H[5:0]	Data Type
6'b11 1111	16-bit gray scale data
6'b10 1011	10-bit gray scale data
6'b11 0011	8-bit dot correction data
6'b10 0111	6-bit dot correction data
6'b10 0011	16-bit configuration data
6'b11 0111	10-bit configuration data

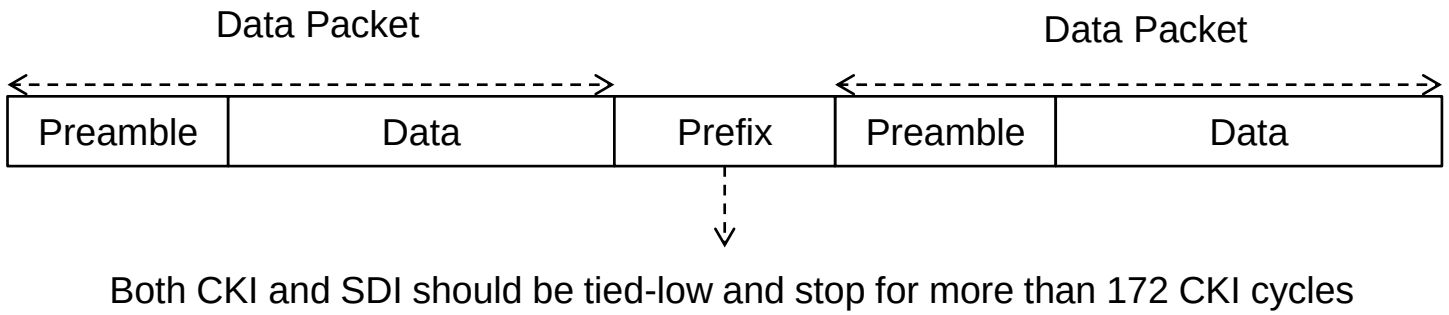
Once MBI6020 receives the SDI=1 (1'b1), MBI6020 will start to check if the data is a valid header or not. If the 6-bit data is a valid header, the driver will latch the specific data according to the protocol. If the 6-bit data is not a valid header, MBI6020 will wait for another SDI=1 (1'b1) to check the validity of the next header.

Time-Out Reset for Transmission Abort

MBI6020 CKI signal cannot be stopped for more than 95 CKI cycles during the data transmission to prevent ICs from misreading. If the CKI is stopped for more than 95 CKI cycles, MBI6020 will ignore the present input data and continuously show the previous image data until the next image data is correctly recognized.

The Prefix in the Beginning of a Data Packet

The prefix is a symbol of "Silent-to-Reset", i.e. a time period for MBI6020 to distinguish two data packets. During the prefix, both CKI and SDI should be tied-low and stop for more than 172 CKI cycles. The prefix between two data packets helps MBI6020 identify the data packet correctly.



Definition of Configuration Register

MBI6020 provides two configuration register banks: configuration register bank 1 (CF1) as defined in the tables below.

Configuration Register Bank 1 (CF1):

	MSB									LSB
Bit	9	8	7	6	5	4	3	2	1	0
Default Value	10		0	11		1	1	11		0

Note: Bit [15:10] should be set as “0” to avoid signal misjudgment.

Bit	Definition	Value	Function	
9:8	PWM clock frequency selection	11	Bit[6:5]=11	PWM clock=20MHz
			Bit[6:5]=10	PWM clock=1.25MHz
		10 (Default)	Bit[6:5]=11	PWM clock=10MHz
			Bit[6:5]=10	PWM clock=625kHz
		01	Bit[6:5]=11	PWM clock=5MHz
			Bit[6:5]=10	PWM clock=312.5kHz
		00	Bit[6:5]=11	PWM clock=2.5MHz
			Bit[6:5]=10	PWM clock=156.25kHz
7	Dot correction mode	0 (Default)	Enable dot correction	
		1	Disable dot correction	
6:5	High/Low frequency GCLK selection	11 (Default)	Select high GCLK frequency 20MHz/10MHz/5MHz/2.5MHz	
		10	Select low GCLK frequency 1.25MHz/625kHz/312.5kHz/156.25kHz	
		01	Reserved	
		00	Reserved	
4	PWM counter reset	1 (Default)	PWM counter reset after configuring control register	
		0	PWM counter does not reset after configuring control register	
3	PWM data synchronization	1 (Default)	Automatic synchronization	
		0	Manual synchronization	
2:1	Phase-inverted output clock	11 (Default)	The waveform is reversed from CKI to CKO; Please fill in 11. Other combinations are reserved.	
0	Parity check	1	Enable	
		0 (Default)	Disable	

PWM Clock Frequency

MBI6020 provides eight kinds of internal GCLK frequency, which are the internal oscillator frequency divided by 1, 2, 4, 8, 16, 32, 64, and 128 for different applications according to the bits of CF1[9:8] and CF1[6:5].

GCLK Source Selection

MBI6020 provides flexibility to select GCLK source by setting the bits of CF1[6:5].

Dot Correction Mode

MBI6020 also provides 8-bit or 6-bit dot correction in 16-bit or 10-bit gray scale mode respectively. Dot correction control helps compensate LED brightness and reduces the loading of calculation in controllers. In addition, with the built-in multiplier, MBI6020 operates dot correction without sacrificing the visual refresh rate.

PWM Counter Reset

MBI6020 can optionally reset the PWM counter by setting the bit of CF1[4] after programming configuration data.

PWM Data Synchronization

MBI6020 is also flexible for either manual-synchronization or auto-synchronization by setting the bit of CF1[3]. For auto-synchronization, the bit of CF1[3] is set to “1” (default). MBI6020 will automatically process the synchronization of previous data and next data for PWM counting. The next image data will be updated to output buffers and start PWM counting when the previous data finishes one internal PWM cycle.

For manual-synchronization, the bit of CF1[3] is set to “0”. Once the next input data is correctly recognized, MBI6020 will stop the present PWM cycle and restart a new PWM cycle to show the new data immediately.

Phase-inverted Output Clock

MBI6020 enhances the capability of cascading MBI6020 from clock reverse function by setting the bits of CF1[2:1]. The waveform will be reversed from CKI to CKO to balance the duty of the clock signal. This improves the signal integrity of data transmission.

The advantage of manual-synchronization is to maintain the synchronization of image frames between ICs, but the PWM cycle may not be finished, so the gray scale accuracy is slightly affected. Since S-PWM scrambles the 16-bit PWM cycle into 64 small periods, the gray scale accuracy remains good. For better gray scale performance, auto-synchronization keeps accurate gray scale especially when using the built-in oscillator, but the drawback is the synchronization of image frames between ICs.

Parity Check

Parity check is to check the data in the header for any error, especially to prevent the configuration register and dot correction register from miswriting.

Configuration Register Bank 2 (CF2):

Default Value

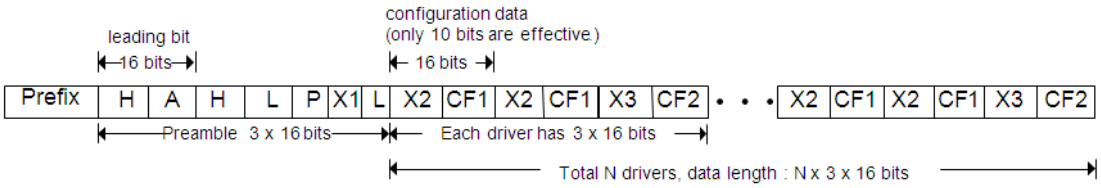
	MSB		LSB
Bit	2	1	0
Value	111		

Note: Bit [15:3] should be set as “0” to avoid signal misjudgment.

Bit	Definition	Value	Function
2	Reserved	1 (Default)	Must fill in 1
1:0	Reserved	11 (Default)	Must fill in 11

16-bit Configuration Data

For 16-bit configuration data, each word is 16 bits. Each MBI6020 needs 3 words (3x16=48 bits) for the configuration data. However, each configuration data has only 10 bits, and the MSB 6 bits of each word are invalid. Prior to the configuration data, there is a 48-bit preamble. MBI6020 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

48-bit preamble

Bit	Definition	Value	Function
47:42	H[5:0]	100011	The header of 16-bit configuration data
41:32	A[9:0]	0000000000	Address. Always send 10’b 0000000000
31:26	H[5:0]	100011	Double check the header
25:16	L[9:0]	N-1. N=Number of IC in series	Set the number of IC in series
15:12	P[3:0]	0000~1111	P[0] is the parity check bit of L[9:0] P[0]=1 if the count of “1” within L[9:0] is odd; P[0]=0 if the count of “1” within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of “1” within A[9:0] is odd; P[1]=0 if the count of “1” within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of “1” within H[5:0] is odd; P[2]=0 if the count of “1” within H[5:0] is even. P[3] is the parity check bit of P[2:0] P[3]=1 if the count of “1” within P[2:0] is odd; P[3]=0 if the count of “1” within P[2:0] is even.
11:10	X1[1:0]	XX	Don’t care. Recommend to fill in 00.
9:0	L[9:0]	N-1, N=Number of IC in series	Double check the number of IC in series

48-bit configuration data

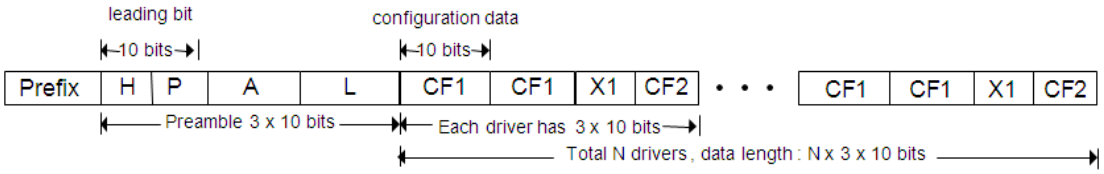
Bit	Definition	Value	Function
47:42	X2[5:0]	XXXXXX	Don’t care. Recommend to fill in 000000.
41:32	CF1[9:0]	0000000000~1111111111	10 bits data of configuration register bank 1 (CF1)
31:26	X2[5:0]	XXXXXX	Don’t care. Recommend to fill in 000000.

25:16	CF1[9:0]	0000000000~1111111111	Double check the data of configuration register bank 1 (CF1). It should be the same as bit[41:32], otherwise the data will not be written into register.
15:3	X3[12:0]	XXXXXXXXXXXXX	Don't care. Recommend to fill in 0000000000000.
2:0	CF2[2:0]	000~111	3 bits data of configuration register bank 2 (CF2)

The configuration data of the last IC is sent first, followed by the previous ICs, and the first IC's configuration data is sent in the end of the packet.

10-bit Configuration Data

For 10-bit configuration data, each word is 10 bits. Each MBI6020 needs 3 words (3x10=30 bits) for the configuration data. Prior to the configuration data, there is a 30-bit preamble. MBI6020 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

30-bit preamble

Bit	Definition	Value	Function
29:24	H[5:0]	110111	The header of 10-bit configuration data
23:20	P[3:0]	0000~1111	P[0] is the parity check bit of L[9:0]. P[0]=1 if the count of "1" within L[9:0] is odd; P[0]=0 if the count of "1" within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of "1" within A[9:0] is odd; P[1]=0 if the count of "1" within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of "1" within H[5:0] is odd; P[2]=0 if the count of "1" within H[5:0] is even. P[3] is the parity check bit of P[2:0] P[3]=1 if the count of "1" within P[2:0] is odd; P[3]=0 if the count of "1" within P[2:0] is even.
19:10	A[9:0]	0000000000	Address. Always send 10'b 0000000000
9:0	L[9:0]	N-1. N=Number of IC in series	Set the number of IC in series

30-bit configuration data

Bit	Definition	Value	Function
29:20	CF1[9:0]	0000000000~1111111111	10 bits data of configuration register bank 1 (CF1)
19:10	CF1[9:0]	0000000000~1111111111	Double check the data of configuration register bank 1(CF1). It should be the same as bit[29:20]; otherwise, the data will not be written into register.
9:3	X4[6:0]	XXXXXXX	Don't care. Recommend to fill in 0000000
2:0	CF2[2:0]	000~111	3 bits data of configuration register bank 2 (CF2)

The configuration data of the last IC is sent first, followed by the previous ICs, and the first IC's configuration data is sent in the end of the packet.

Gray Scale Control

MBI6020 provides two gray scale modes: 16-bit gray scale mode and 10-bit gray scale mode. MBI6020 specifically adopts S-PWM technology in 16-bit gray scale mode to scramble the 16-bit PWM to 64 segments, so that the visual refresh rate can be increased. For example, with S-PWM, the default PWM clock frequency is 10MHz (the frequency of internal oscillator/2), and therefore, the visual refresh rate of 16-bit gray scale mode will be increased to: 10MHz/65536x64=9,766Hz

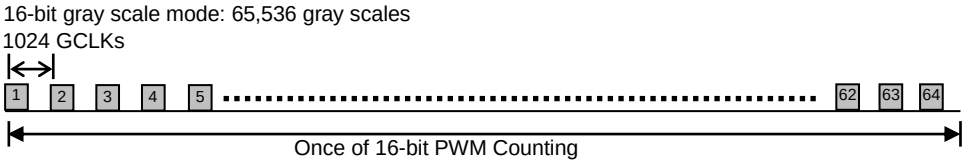
On the other hand, MBI6020 provides 10-bit gray scale mode by traditional PWM. In 16-bit gray scale mode, MBI6020 achieves 65,536 gray scales for each LED, and in 10-bit gray scale mode, MBI6020 achieves 1,024 gray scales.

MBI6020 continuously repeats the PWM cycle and turns on the output ports according to the image data until the next image data is correctly recognized. Once the next input data is correctly recognized, MBI6020 will stop the present PWM cycle and restart a new PWM cycle to show the new data immediately.

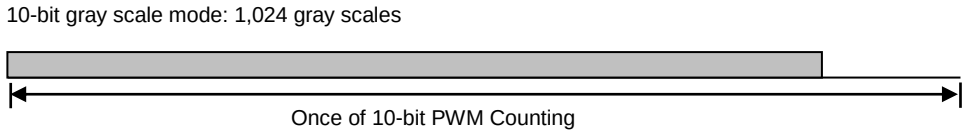
PWM counting by S-PWM or conventional PWM algorithm

With S-PWM technology, the total PWM cycles can be broken down into 64 segments.

16-bit Gray Scale Mode with S-PWM



10-bit Gray Scale Mode with Conventional PWM



Example of 16-bit Gray Scale Data:

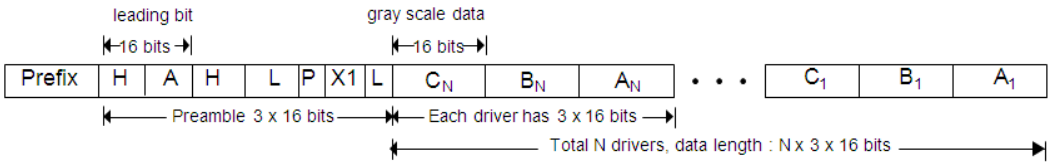
Gray scale data	The ratio of output turn-on time in a PWM cycle
0	$0/2^{16}$
1	$1/2^{16}$
2	$2/2^{16}$
⋮	⋮
65535	$65535/2^{16}$

Example of 10-bit Gray Scale Data:

Gray scale data	The ratio of output turn-on time in a PWM cycle
0	$0/2^{10}$
1	$1/2^{10}$
2	$2/2^{10}$
⋮	⋮
1023	$1023/2^{10}$

16-bit Gray Scale Data

For 16-bit gray scale data, each word is 16 bits. Each MBI6020 needs 3 words (3x16=48 bits) for the gray scale data of $\overline{OUTC}$, $\overline{OUTB}$ and $\overline{OUTA}$. Prior to the gray scale data, there is a 48-bit preamble. MBI6020 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

48-bit preamble

Bit	Definition	Value	Function
47:42	H[5:0]	111111	The header of 16-bit gray scale data
41:32	A[9:0]	0000000000	Address. Always send 10'b 0000000000
31:26	H[5:0]	111111	Double check the header
25:16	L[9:0]	N -1. N=Number of IC in series	Set the number of IC in series
15:12	P[3:0]	0000~1111	P[0] is the parity check bit of L[9:0] P[0]=1 if the count of "1" within L[9:0] is odd; P[0]=0 if the count of "1" within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of "1" within A[9:0] is odd; P[1]=0 if the count of "1" within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of "1" within H[5:0] is odd; P[2]=0 if the count of "1" within H[5:0] is even. P[3] is the parity check bit of P[2:0] P[3]=1 if the count of "1" within P[2:0] is odd; P[3]=0 if the count of "1" within P[2:0] is even.
11:10	X1[1:0]	XX	Don't care. Recommend to fill in 00.
9:0	L[9:0]	N-1. N=Number of IC in series	Double check the number of IC in series

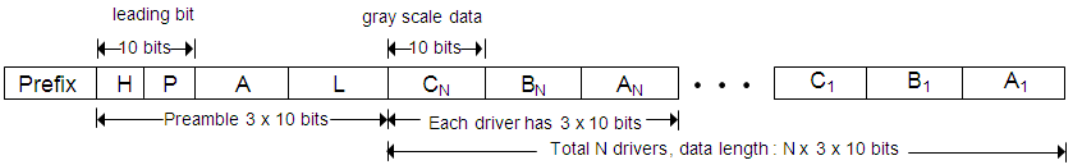
48-bit gray scale data

Bit	Definition	Value	Function
47:32	C_N[15:0]	0000000000000000~1111111111111111	16 bits gray scale data of the nth $\overline{OUTC}$ The ratio of $\overline{OUTC}$ turn-on time will be $C_N[15:0]/2^{16}$.
31:16	B_N[15:0]	0000000000000000~1111111111111111	16 bits gray scale data of the nth $\overline{OUTB}$ The ratio of $\overline{OUTB}$ turn-on time will be $B_N[15:0]/2^{16}$.
15:0	A_N[15:0]	0000000000000000~1111111111111111	16 bits gray scale data of the nth $\overline{OUTA}$ The ratio of $\overline{OUTA}$ turn-on time will be $A_N[15:0]/2^{16}$.

The gray scale data of the last IC is sent first, followed by the previous ICs, and the first IC's gray scale data is sent in the end of the packet.

10-bit Gray Scale Data

For 10-bit gray scale data, each word is 10 bits. Each MBI6020 needs 3 words (3x10=30 bits) for the gray scale data of $\overline{OUTC}$, $\overline{OUTB}$ and $\overline{OUTA}$. Prior to the gray scale data, there is a 30-bit preamble. MBI6020 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

30-bit preamble

Bit	Definition	Value	Function
29:24	H[5:0]	101011	The header of 10-bit gray scale data
23:20	P[3:0]	0000~1111	P[0] is the parity check bit of L[9:0]. P[0]=1 if the count of "1" within L[9:0] is odd; P[0]=0 if the count of "1" within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of "1" within A[9:0] is odd; P[1]=0 if the count of "1" within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of "1" within H[5:0] is odd; P[2]=0 if the count of "1" within H[5:0] is even. P[3] is the parity check bit of P[2:0] P[3]=1 if the count of "1" within P[2:0] is odd; P[3]=0 if the count of "1" within P[2:0] is even.
19:10	A[9:0]	0000000000	Address. Always send 10'b 0000000000
9:0	L[9:0]	N-1. N=Number of IC in series	Set the number of IC in series

30-bit gray scale data

Bit	Definition	Value	Function
29:20	C_N[9:0]	0000000000~1111111111	10 bits gray scale data of the nth $\overline{OUTC}$ The ratio of $\overline{OUTC}$ turn-on time will be $C_N[9:0]/2^{10}$.
19:10	B_N[9:0]	0000000000~1111111111	10 bits gray scale data of the nth $\overline{OUTB}$ The ratio of $\overline{OUTB}$ turn-on time will be $B_N[9:0]/2^{10}$.
9:0	A_N[9:0]	0000000000~1111111111	10 bits gray scale data of the nth $\overline{OUTA}$ The ratio of $\overline{OUTA}$ turn-on time will be $A_N[9:0]/2^{10}$.

The gray scale data of the last IC is sent first, followed by the previous ICs, and the first IC's gray scale data is sent in the end of the packet.

Dot Correction Control

MBI6020 also provides 8-bit or 6-bit dot correction control in 16-bit or 10-bit gray scale mode respectively. Dot correction control helps calibrate LED brightness and reduces the loading of calculation in controllers. In addition, designed with S-PWM technology, MBI6020 operates dot correction without sacrificing the visual refresh rate.

For valid dot correction control, users have to program dot correction data before sending gray scale data.

16-bit gray scale data with 8-bit dot correction data

The following is the equation for the duty cycle of output in 16-bit gray scale mode. For 8-bit dot correction, the default value of dot correction data is 255.

$$\text{The duty cycle of output (\%)} = \frac{\text{16-bit gray scale data} \times \frac{(\text{8-bit dot correction data} + 1)}{256}}{65{,}536} \times 100\%$$

According to the above equation, the following table shows the examples:

Dot correction data	The ratio of output turn-on time
0	1/256 x gray scale data
1	2/256 x gray scale data
2	3/256 x gray scale data
. . .	. . .
255	256/256 x gray scale data

10-bit gray scale with 6-bit dot correction data

The following is the equation for the duty cycle of output in 10-bit gray scale mode. For 6-bit dot correction, the default value of dot correction data is 63.

$$\text{The duty cycle of output (\%)} = \frac{\text{10-bit gray scale data} \times \frac{(\text{6-bit dot correction data} + 1)}{64}}{1{,}024} \times 100\%$$

According to the above equation, the following table shows the examples:

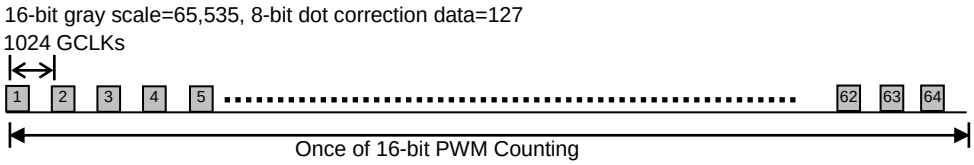
Dot correction data	The ratio of output turn-on time
0	1/64 x gray scale data
1	2/64 x gray scale data
2	3/64 x gray scale data
. . .	. . .
63	64/64 x gray scale data

The algorithm of PWM counting with dot correction data

When adopting 8-bit dot correction in 16-bit gray scale mode, MBI6020 multiplies the 16-bit gray scale data and the 10-bit dot correction data and truncates the product to 16 bits, then uses the corrected 16-bit data to generate PWM output by S-PWM technology. The built-in multiplier facilitates to keep high visual refresh rate.

The chart below illustrates the effect of the built-in multiplier and S-PWM.
Assume:
the 16-bit gray scale data=65,535,
8-bit dot correction data=127 (50%),
then the 16-bit PWM output period is scrambled into 64 segments,
each segment has ~50% duty ratio.

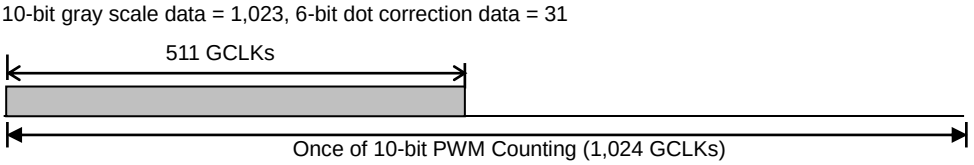
16-bit Gray Scale Data with 8-bit Dot Correction Data



When adopting 6-bit dot correction in 10-bit gray scale mode, MBI6020 multiplies the 10-bit gray scale data and the 6-bit dot correction data and truncates the product to 10 bits, then uses the corrected 10-bit data to generate PWM output by S-PWM technology. The built-in multiplier facilitates to keep high visual refresh rate.

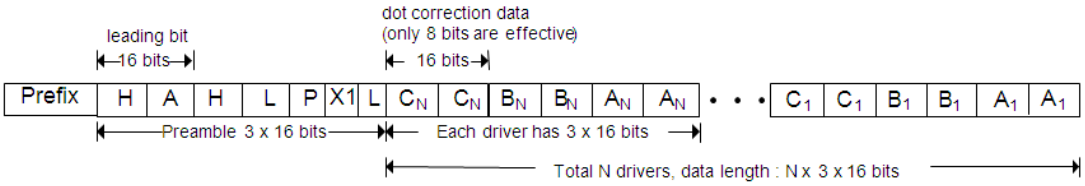
The chart below shows the PWM output.
Assume:
the 10-bit grayscale data=1023,
6-bit dot correction data=31 (50%).
the output duty ratio=511/1024(~50%).
the output duty cycle=1024 GCLKs.

10 Gray Scale Data with 6-bit Dot Correction Data



8-bit Dot Correction Data

For 8-bit dot correction data, each word is 16 bits. Each MBI6020 needs 3 words (3x16=48 bits) for the dot correction data of $\overline{OUTC}$, $\overline{OUTB}$ and $\overline{OUTA}$. However, each dot correction data has only 8 bits, and the first 8 bits of each word are checking bits of dot correction. Prior to the dot correction data, there is a 48-bit preamble. MBI6020 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

48-bit preamble

Bit	Definition	Value	Function
47:42	H[5:0]	110011	The header of 8-bit dot correction data
41:32	A[9:0]	0000000000	Address. Always send 10'b 0000000000
31:26	H[5:0]	110011	Double check the header
25:16	L[9:0]	N-1. N=Number of IC in series	Set the number of IC in series
15:12	P[3:0]	0000~1111	P[0] is the parity check bit of L[9:0]. P[0]=1 if the count of "1" within L[9:0] is odd; P[0]=0 if the count of "1" within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of "1" within A[9:0] is odd; P[1]=0 if the count of "1" within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of "1" within H[5:0] is odd; P[2]=0 if the count of "1" within H[5:0] is even. P[3] is the parity check bit of P[2:0] P[3]=1 if the count of "1" within P[2:0] is odd; P[3]=0 if the count of "1" within P[2:0] is even.
11:10	X1[1:0]	XX	Don't care. Recommend to fill in 00.
9:0	L[9:0]	N-1. N=Number of IC in series	Double check the number of IC in series

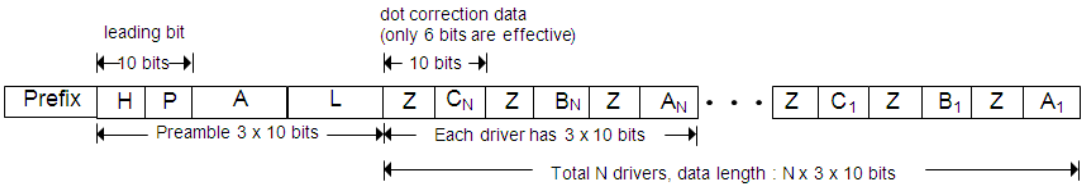
48-bit dot correction data

Bit	Definition	Value	Function
47:40	C_N[7:0]	00000000~11111111	Double check the dot correction data of $\overline{OUTC}$. It should be the same as bit [39:32]; otherwise, the dot correction data will not be latched.
39:32	C_N[7:0]	00000000~11111111	8 bits, dot correction data of $\overline{OUTC}$ The ratio of $\overline{OUTC}$ turn-on time will be (C_N[7:0]+1)/256 x gray scale data C_N.
31:24	B_N[7:0]	00000000~11111111	Double check the dot correction data of $\overline{OUTB}$. It should be the same as bit[23:16]; otherwise, the dot correction data will not be latched.
23:16	B_N[7:0]	00000000~11111111	8 bits, dot correction data for $\overline{OUTB}$ The ratio of $\overline{OUTB}$ turn-on time will be (B_N[7:0]+1)/256 x gray scale data B_N.
15:8	A_N[7:0]	00000000~11111111	Double check the dot correction data of $\overline{OUTA}$.It should be the same as bit[7:0]; otherwise, the dot correction data will not be latched.
7:0	A_N[7:0]	00000000~11111111	8 bits, dot correction data for $\overline{OUTA}$ The ratio of $\overline{OUTA}$ turn-on time will be (A_N[7:0]+1)/256 x gray scale data A_N.

The dot correction data of the last IC is sent first, followed by the previous ICs, and the first IC's dot correction data is sent in the end of the packet.

6-bit Dot Correction Data

For 6-bit dot correction data, each word is 10 bits. Each MBI6020 needs 3 words (3x10=30 bits) for the dot correction data of $\overline{OUTC}$, $\overline{OUTB}$ and $\overline{OUTA}$. Each dot correction data has 6 bits. Prior to the dot correction data, there is a 30-bit preamble. MBI6020 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

30-bits preamble

Bit	Definition	Value	Function
29:24	H[5:0]	100111	The header of 6-bit dot correction data
23:20	P[3:0]	0000~1111	P[0] is the parity check bit of L[9:0]. P[0]=1 if the count of "1" within L[9:0] is odd; P[0]=0 if the count of "1" within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of "1" within A[9:0] is odd; P[1]=0 if the count of "1" within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of "1" within H[5:0] is odd; P[2]=0 if the count of "1" within H[5:0] is even. P[3] is the parity check bit of P[2:0] P[3]=1 if the count of "1" within P[2:0] is odd; P[3]=0 if the count of "1" within P[2:0] is even.
19:10	A[9:0]	0000000000	Address. Always send 10'b 0000000000
9:0	L[9:0]	N-1. N=Number of IC in series	Set the number of IC in series

30-bit dot correction data

Bit	Definition	Value	Function
29:26	Z[3:0]	0000	Check bits of C_N[5:0]. Please send 4b'0000; otherwise, the dot correction data will not be latched.
25:20	C_N[5:0]	000000~111111	6 bits dot correction data for $\overline{OUTC}$ The ratio of $\overline{OUTC}$ turn-on time will be (C_N[5:0]+1)/64 x gray scale data C_N.
19:16	Z[3:0]	0000	Check bits of B_N[5:0]. Please send 4b'0000; otherwise, the dot correction data will not be latched.
15:10	B_N[5:0]	000000~111111	6 bits dot correction data for $\overline{OUTB}$ The ratio of $\overline{OUTB}$ turn-on time will be (B_N[5:0]+1)/64 x gray scale data B_N.
9:6	Z[3:0]	0000	Check bits of A_N[5:0]. Please send 4b'0000; otherwise, the dot correction data will not be latched.
5:0	A_N[5:0]	000000~111111	6 bits dot correction data for $\overline{OUTA}$

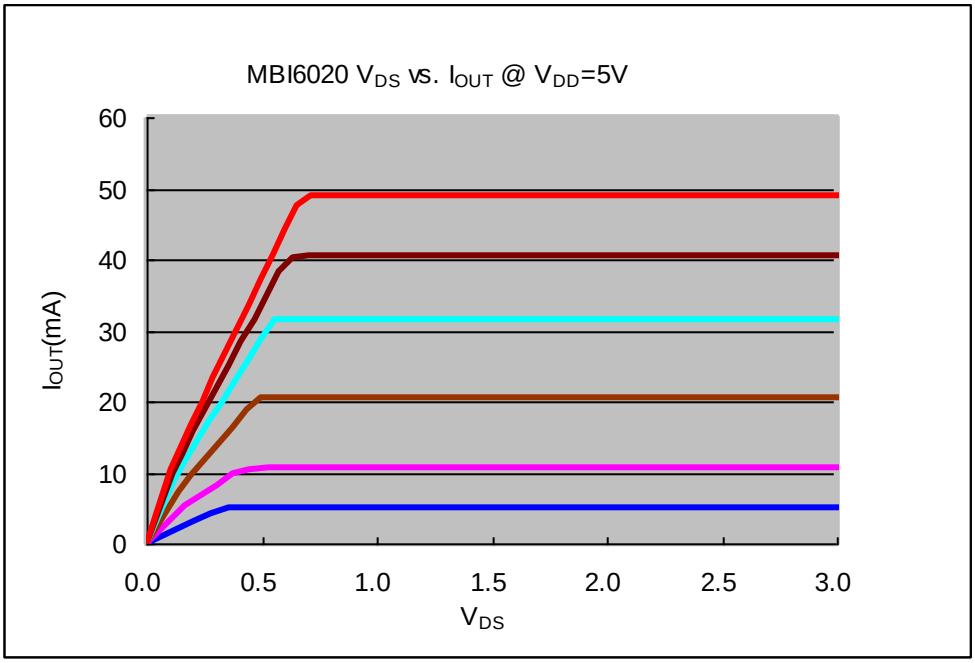
			The ratio of $\overline{OUTA}$ turn-on time will be (A_N[5:0]+1)/64 x gray scale data A_N.

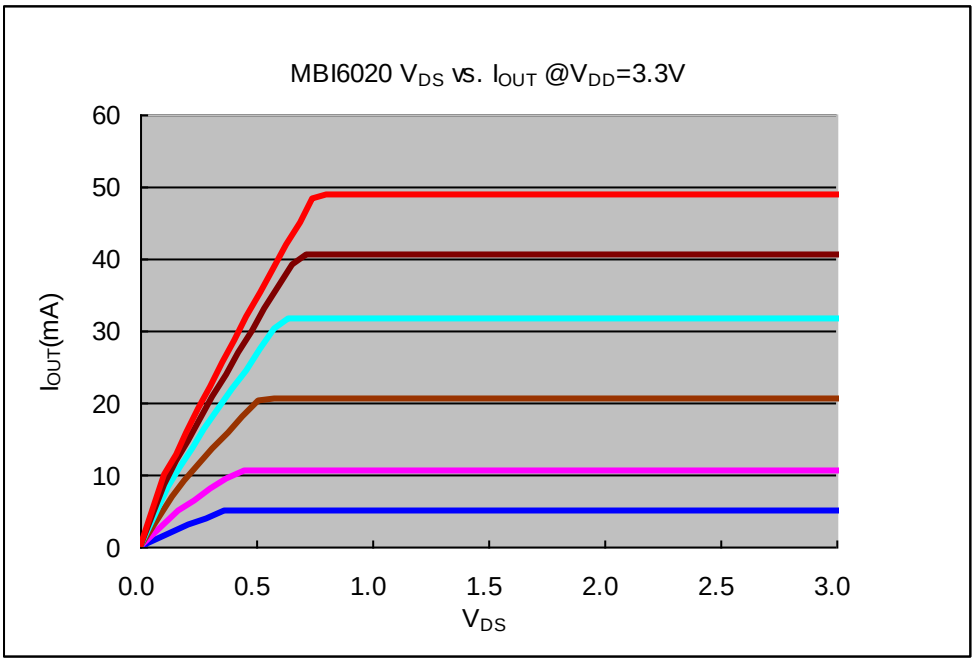
The dot correction data of the last IC is sent first, followed by the previous ICs, and the first IC's dot correction data is sent in the end of the packet.

Constant Current

1) MBI6020 performs excellent current skew: the maximum current variation between channels is less than ±3%, and that between ICs is less than ±6%.

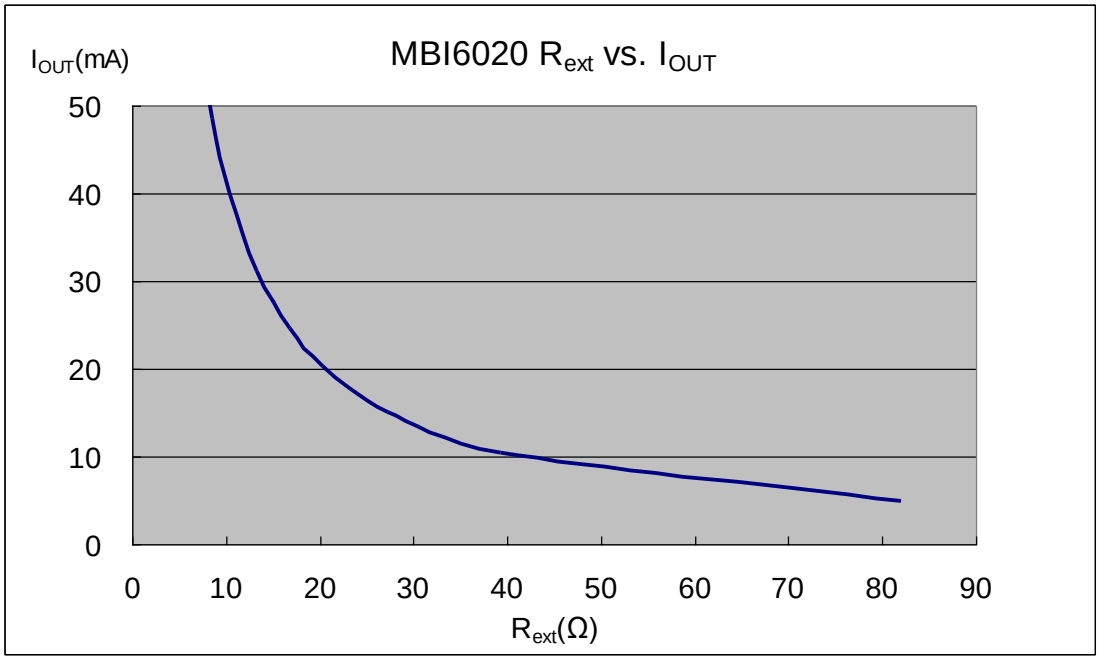
2) In addition, in the saturation region, the output current keeps constant when the output voltage (V_{DS}) is changed. This characteristic guarantees the LED show the same brightness regardless of the variations of LED forward voltages (V_F).





Adjusting Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. The relationship between I_{OUT} and R_{ext} is shown in the following figure.



The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. When output channels are turned on, V_{REXT} is around 0.41V. The relationship between I_{OUT} and R_{ext} is shown in the following figure.

Also, the output current can be calculated from the equation:

$I_{OUTA}=V_{REXT}/R_{extA}$

$I_{OUTB}=V_{REXT}/R_{extB}$

$I_{OUTC}=V_{REXT}/R_{extC}$

Where R_{extA}, R_{extB}, and R_{extC} are the resistances of the external resistors connected to R-EXTA, R-EXTB, R-EXTC terminals.

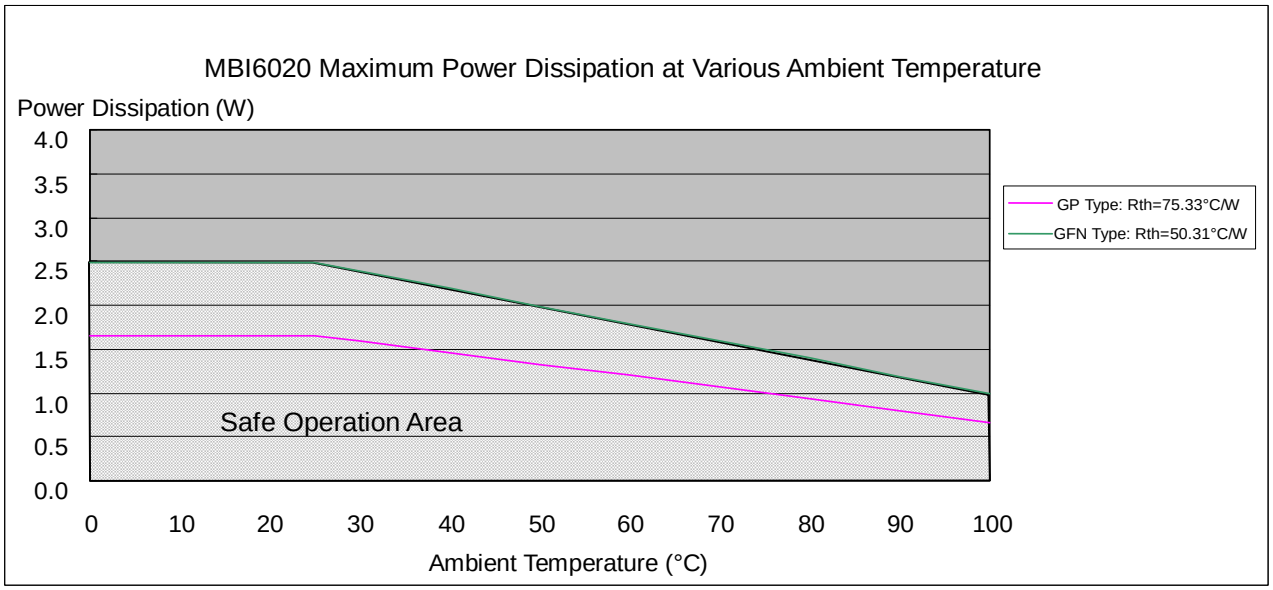
Package Power Dissipation (P_D)

The maximum power dissipation, $P_D(max)=(T_{j,max}–T_a)/R_{th(j-a)}$, decreases as the ambient temperature increases.

The power dissipation (P_D) of MBI6020 is calculated by the equation:

$P_D=(V_{DD}xI_{DD})+[I_{OUTA}x(V_{DSA}–V_{REXTA})]+[I_{OUTB}x(V_{DSB}–V_{REXTB})]+[I_{OUTC}x(V_{DSC}–V_{REXTC})]$

Please refer to the following figure to design within the safe operation area.



Load Supply Voltage (V_{LED})

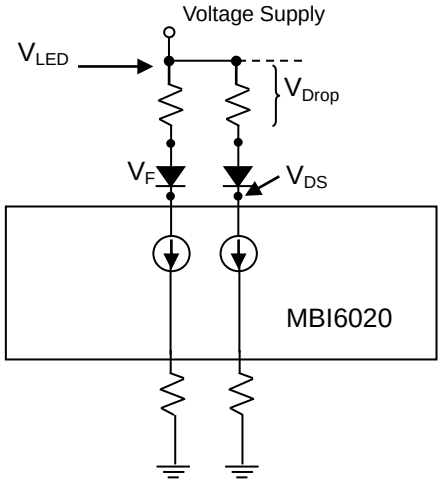
The design of V_{LED} should fulfill two targets:

1. Less power consumption and heat
2. Sufficiently headroom for the LED and driver IC to operate in the constant current region.

From the figure below, $V_{DS}=V_{LED}–V_F$, which V_{LED} is the supply voltage of LED. $P_{D\ (act)}$ will be greater than $P_{D\ (max)}$, if V_{DS} drops too much voltage on the driver. In this case, it is recommended to use the lowest possible supply voltage or to set an external resistor to reduce the by V_{DROP}.

$V_{DS}=(V_{LED}–V_F)–V_{DROP}$

Please refer to the following figure for the application of the resister.

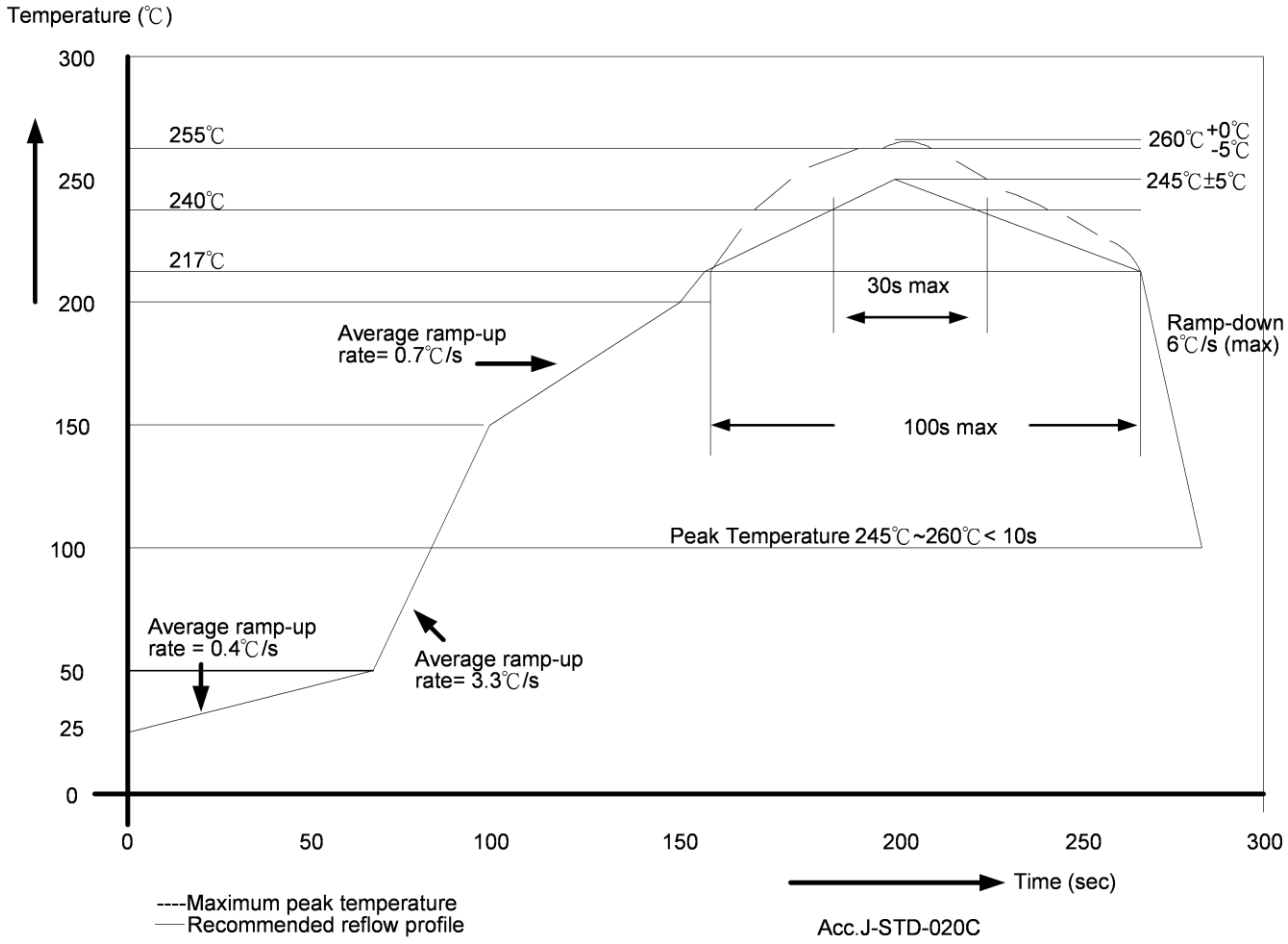


Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, please refer to ***"Application Note for 8-bit and 16-bit LED Drivers-Overshoot"***.

Soldering Process of “Pb-free” Package Plating*

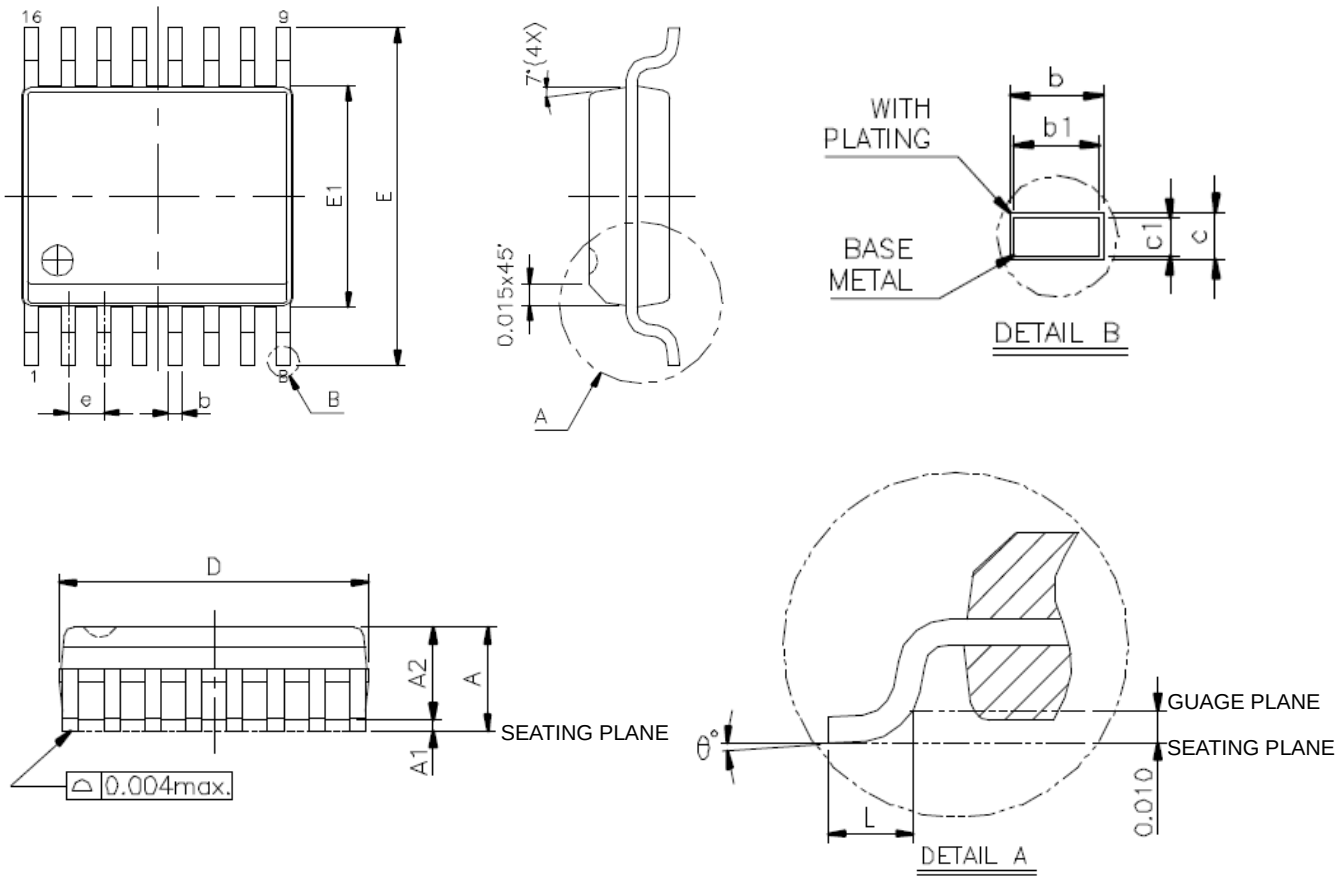
Macroblock has defined "Pb-Free" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.



Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

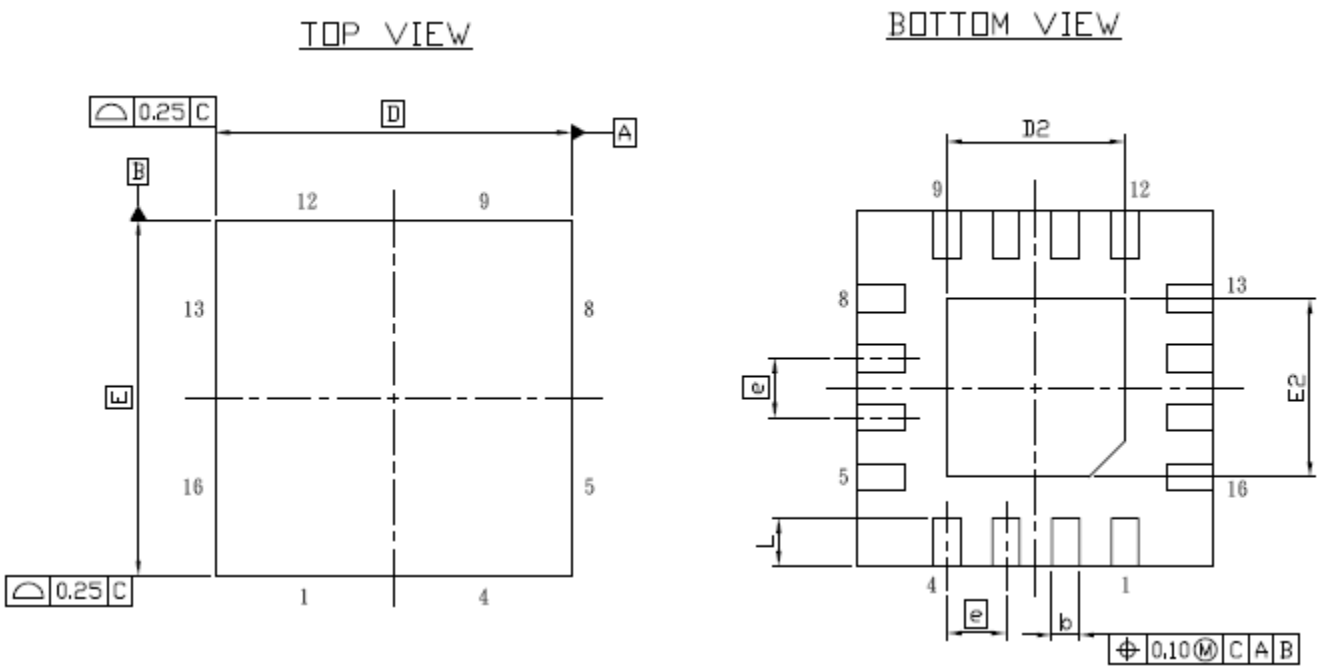
*Note: For details, please refer to Macroblock’s “Policy on Pb-free & Green Package”.

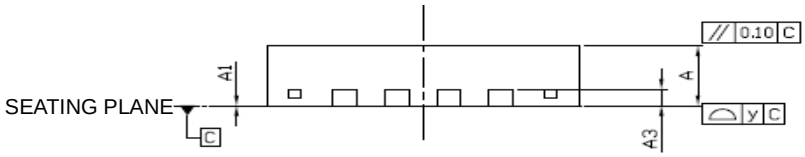
Package Outline



SYMBOLS	Dimensions shown in inchs			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	—	0.069	1.346	—	1.753
A1	0.004	—	0.010	0.102	—	0.254
A2	0.049	—	0.059	1.245	—	1.499
b	0.008	—	0.012	0.203	—	0.305
b1	0.008	0.010	0.011	0.203	0.254	0.279
c	0.007	—	0.010	0.178	—	0.254
c1	0.007	0.008	0.009	0.178	0.203	0.229
D	0.189	0.193	0.197	4.801	4.902	5.004
E1	0.150	0.154	0.157	3.810	3.912	3.988
E	0.228	0.236	0.244	5.791	5.994	6.198
L	0.016	—	0.050	0.406	—	1.270
e	0.025 BASIC			0.635 BASIC		
θ°	0	—	8	0	—	8

MBI6020GP Outline Drawing





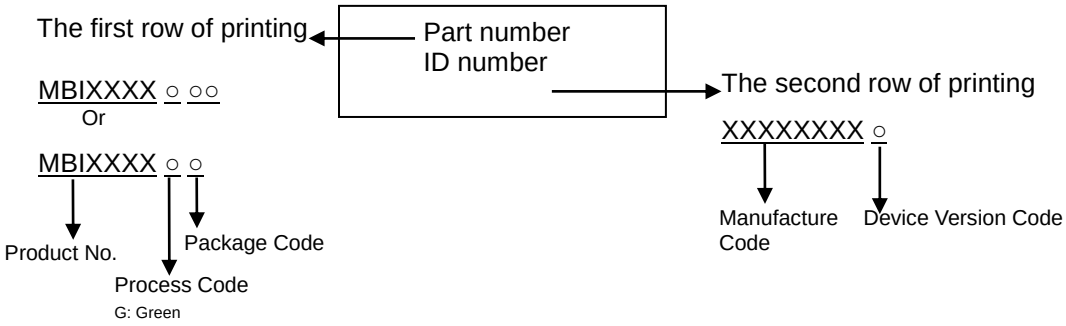
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.203 REF			8.00 REF		
b	0.18	0.23	0.30	7.09	9.06	11.81
D	2.90	3.00	3.10	114.17	118.11	122.05
D2	1.40	1.50	1.60	55.12	59.06	62.99
E	2.90	3.00	3.10	114.17	118.11	122.05
E2	1.40	1.50	1.60	55.12	59.06	62.99
e	0.50 BSC			19.69 BSC		
L	0.30	0.40	0.50	11.81	15.75	19.69
y	0.08			3.15		

MBI6020GFN Outline Drawing

Note 1: The unit for the outline drawing is mm.

Note 2: Please use the maximum dimensions for the thermal pad layout. To avoid the short circuit risk, the vias or circuit traces shall not pass through the maximum area of thermal pad.

Product Top Mark Information



Product Revision History

Datasheet version	Device Version Code
V1.00	A
V1.01	A
V2.00	B
VA.00	B

Product Ordering Information

Part Number	RoHS Compliant Package Type	Weight (g)
MBI6020GP	SSOP16L-150-0.64	0.067g
MBI6020GFN	QFN16L-3*3-0.5	0.038g

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