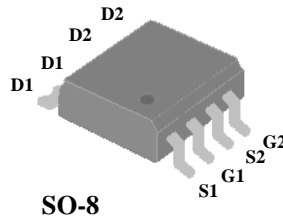


- ▼ Simple Drive Requirement
- ▼ Lower Gate Charge
- ▼ Fast Switching Performance
- ▼ RoHS Compliant & Halogen-Free

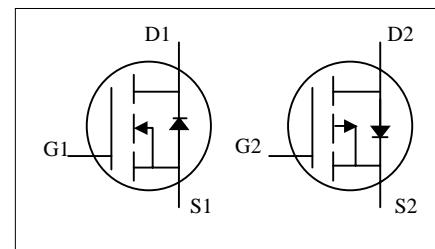


N-CH	$BV_{DSS}$	30V
	$R_{DS(ON)}$	18m $\Omega$
	$I_D$	8.2A
P-CH	$BV_{DSS}$	-30V
	$R_{DS(ON)}$	29m $\Omega$
	$I_D$	-6.6A

## Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



## Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
$V_{DS}$	Drain-Source Voltage	30	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D@T_A=25^\circ C$	Continuous Drain Current <sup>3</sup>	8.2	-6.6	A
$I_D@T_A=70^\circ C$	Continuous Drain Current <sup>3</sup>	6.6	-5.3	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	30	-30	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	2		W
$T_{STG}$	Storage Temperature Range	-55 to 150		$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150		$^\circ C$

## Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	62.5	$^\circ C/W$


**N-CH Electrical Characteristics @ $T_j=25^{\circ}\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=8A$	-	-	18	m $\Omega$
		$V_{GS}=4.5V, I_D=5A$	-	-	35	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10V, I_D=8A$	-	14	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=30V, V_{GS}=0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=8A$	-	6	9.6	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=15V$	-	1.5	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	3.5	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=15V$	-	6	-	ns
$t_r$	Rise Time	$I_D=1A$	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	15	-	ns
$t_f$	Fall Time	$R_D=15\Omega$	-	3.5	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	370	590	pF
$C_{oss}$	Output Capacitance	$V_{DS}=25V$	-	90	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	75	-	pF
$R_g$	Gate Resistance	$f=1.0\text{MHz}$	-	1.5	-	$\Omega$

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=1.7A, V_{GS}=0V$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time <sup>2</sup>	$I_S=8A, V_{GS}=0V,$	-	18	-	ns
$Q_{rr}$	Reverse Recovery Charge	$dI/dt=100A/\mu s$	-	9	-	nC

**P-CH Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-6A$	-	-	29	m $\Omega$
		$V_{GS}=-4.5V, I_D=-4A$	-	-	45	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-	-3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=-10V, I_D=-6A$	-	14	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=+20V, V_{DS}=0V$	-	-	+100	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=-6A$	-	12	19.2	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=-15V$	-	3	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	6.3	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=-15V$	-	10.5	-	ns
$t_r$	Rise Time	$I_D=-1A$	-	6.5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=-10V$	-	32	-	ns
$t_f$	Fall Time	$R_D=15\Omega$	-	17	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	965	1540	pF
$C_{oss}$	Output Capacitance	$V_{DS}=-25V$	-	165	-	pF
$C_{riss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	145	-	pF
$R_g$	Gate Resistance	$f=1.0\text{MHz}$	-	6	-	$\Omega$

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=-1.7A, V_{GS}=0V$	-	-	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_S=-6A, V_{GS}=0V,$	-	23	-	ns
$Q_{rr}$	Reverse Recovery Charge	$dI/dt=100A/\mu s$	-	15	-	nC

**Notes:**

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board ; 135 °C/W when mounted on Min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

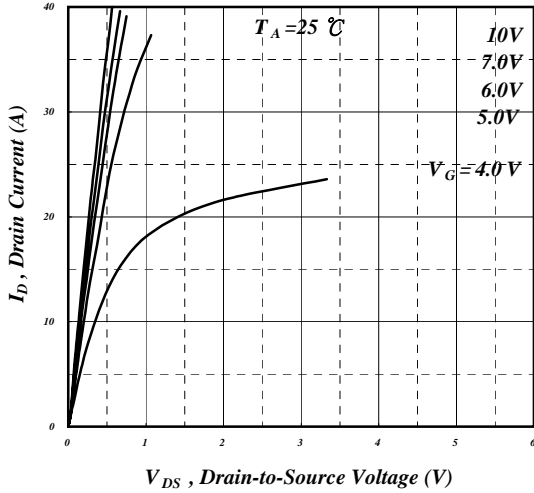
USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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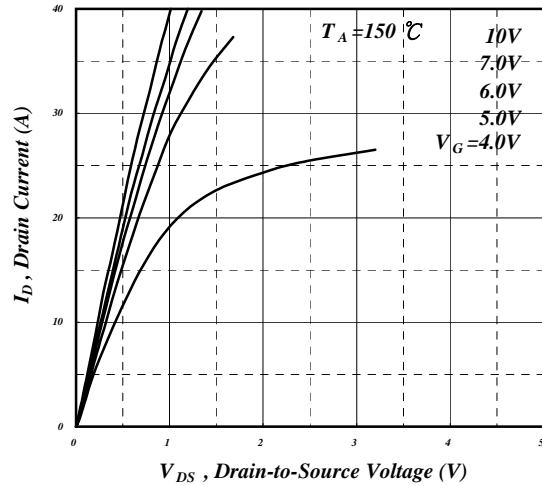
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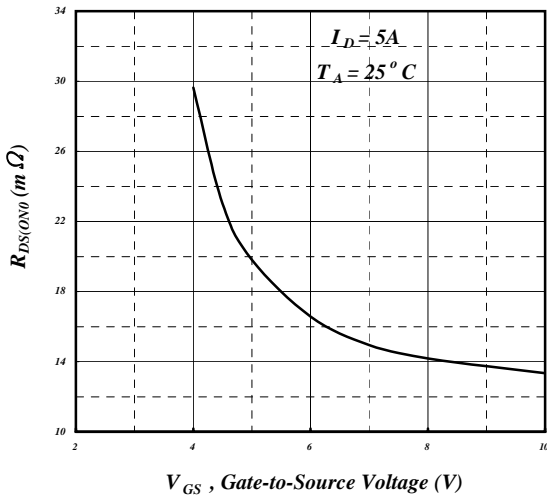
## N-Channel



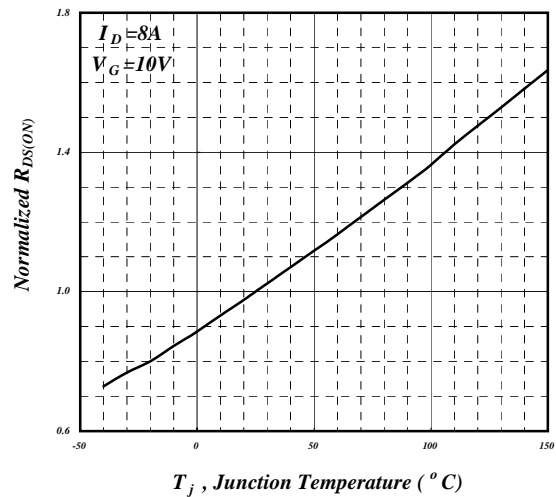
**Fig 1. Typical Output Characteristics**



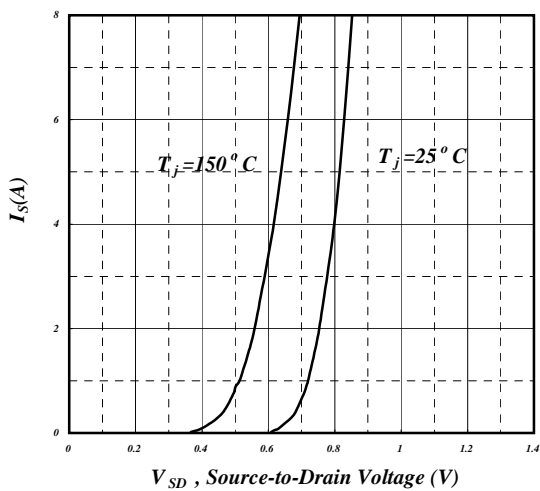
**Fig 2. Typical Output Characteristics**



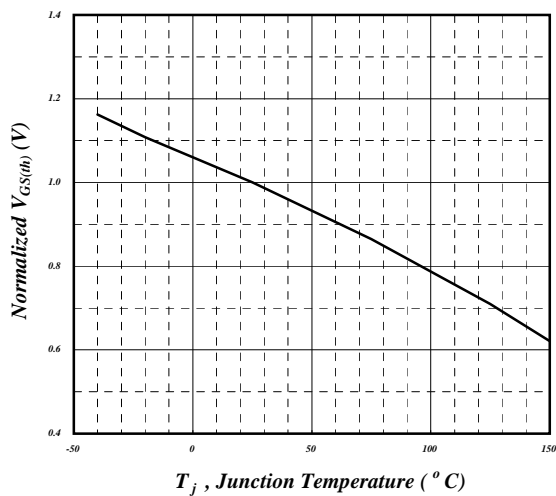
**Fig 3. On-Resistance v.s. Gate Voltage**



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**



**Fig 5. Forward Characteristic of Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**



N-Channel

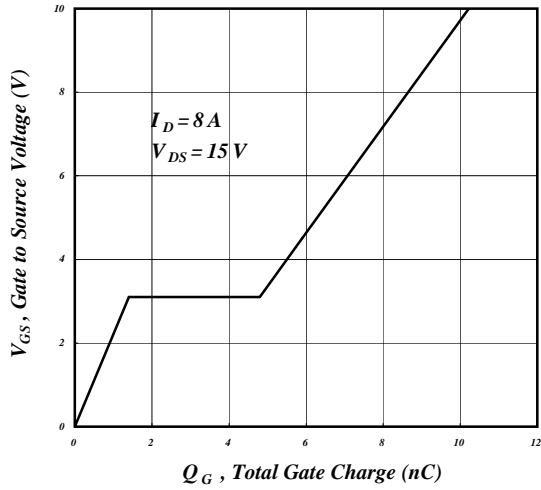


Fig 7. Gate Charge Characteristics

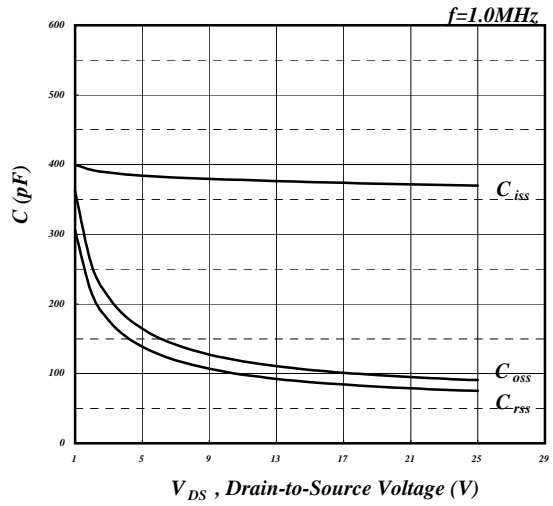


Fig 8. Typical Capacitance Characteristics

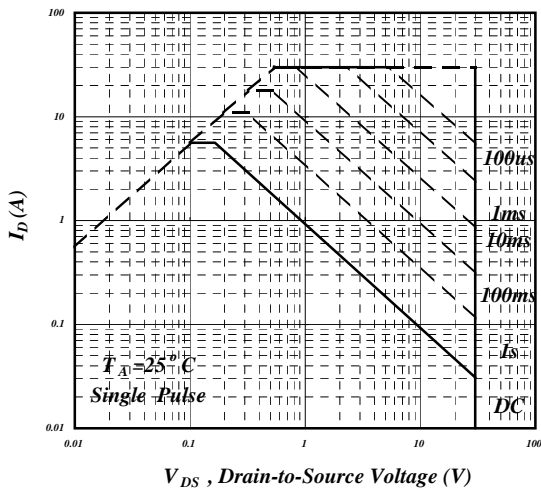


Fig 9. Maximum Safe Operating Area

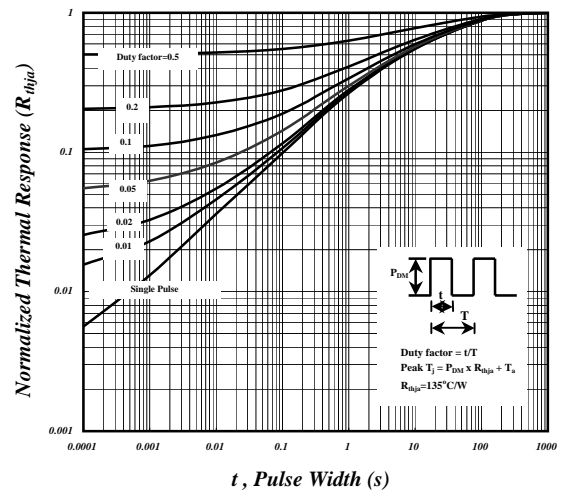


Fig 10. Effective Transient Thermal Impedance

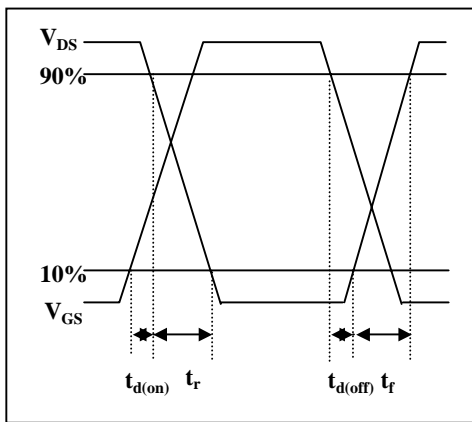


Fig 11. Switching Time Waveform

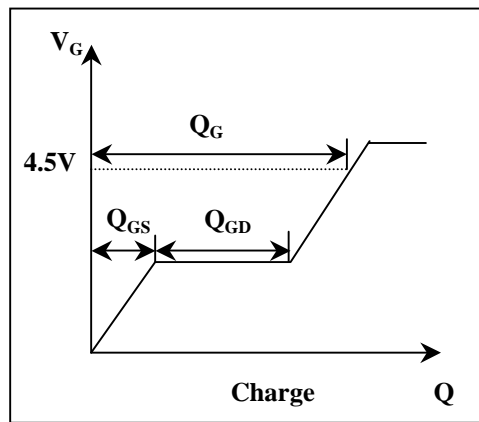


Fig 12. Gate Charge Waveform



# AP4503BGM-HF

## P-Channel

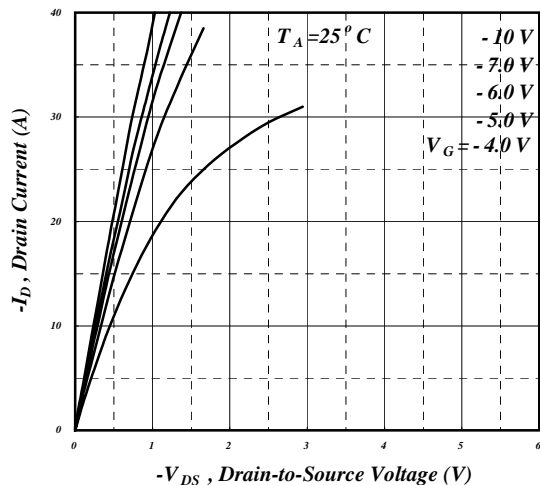


Fig 1. Typical Output Characteristics

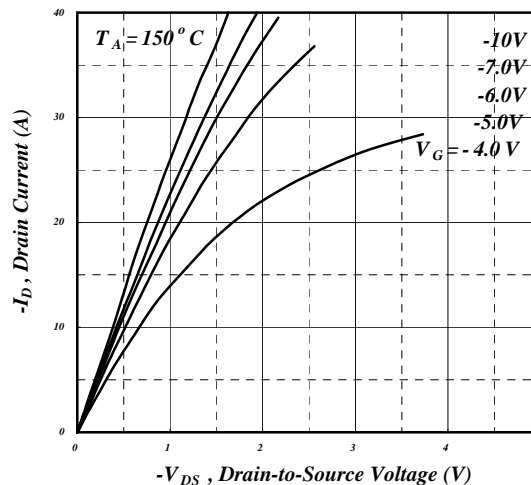


Fig 2. Typical Output Characteristics

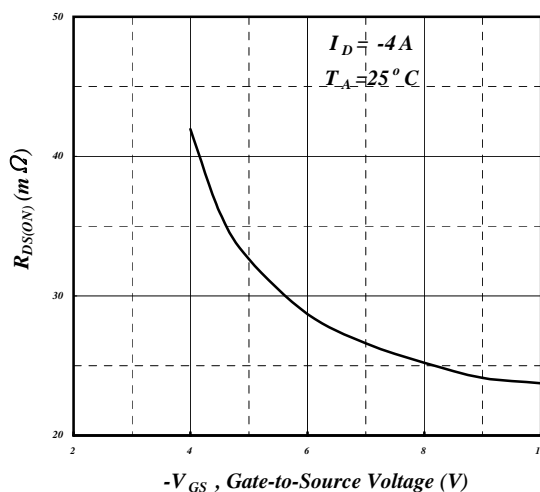


Fig 3. On-Resistance v.s. Gate Voltage

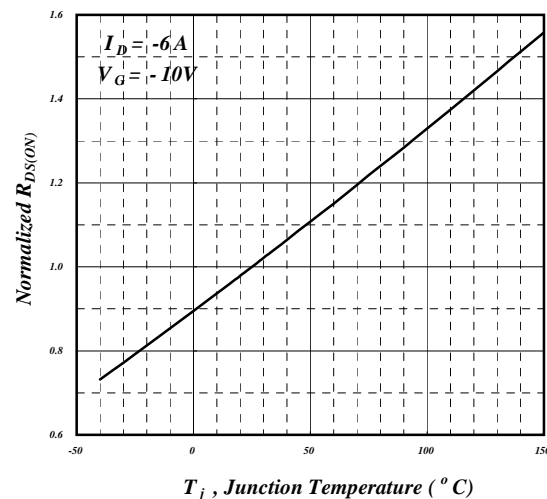


Fig 4. Normalized On-Resistance v.s. Junction Temperature

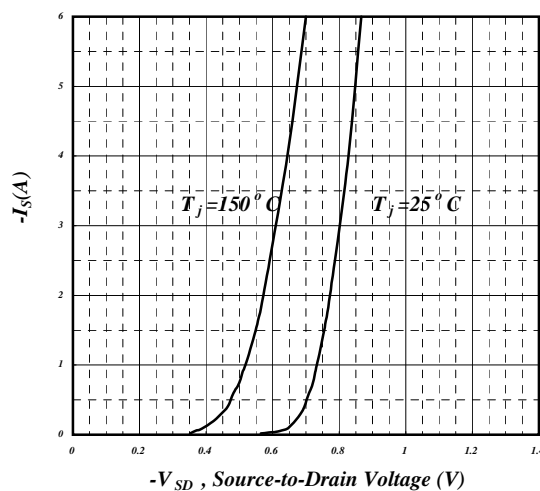


Fig 5. Forward Characteristic of Reverse Diode

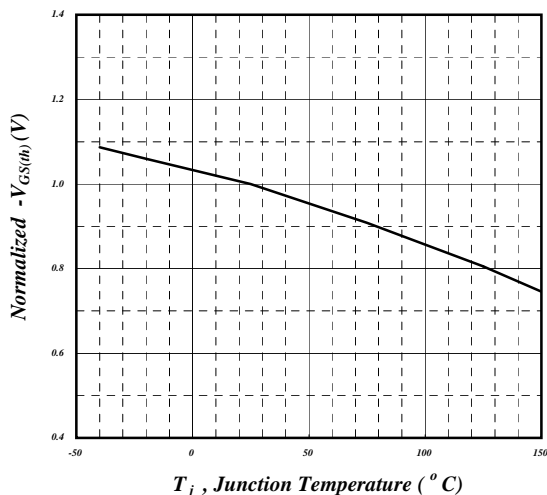


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



P-Channel

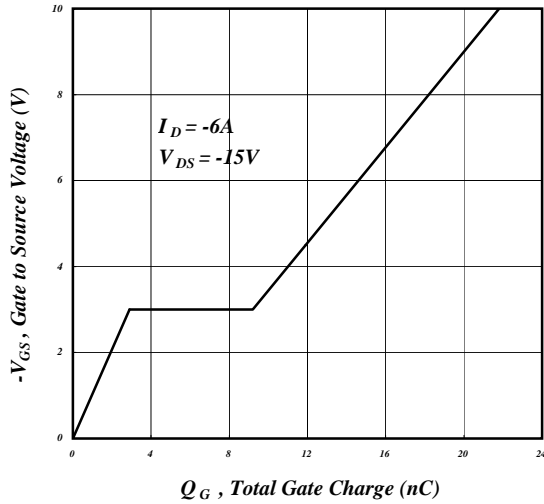


Fig 7. Gate Charge Characteristics

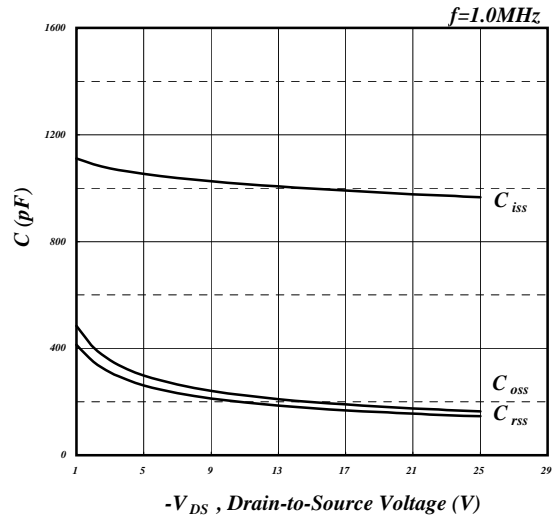


Fig 8. Typical Capacitance Characteristics

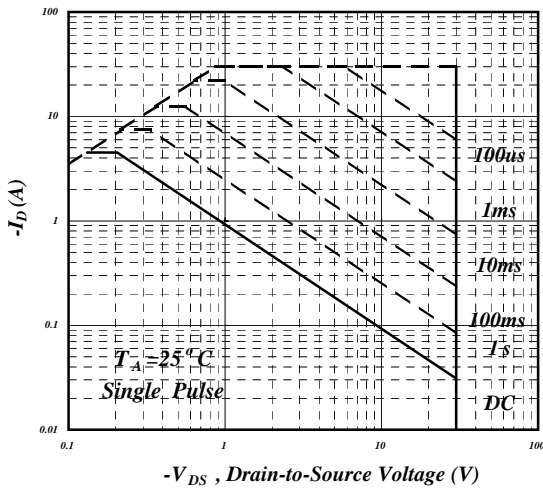


Fig 9. Maximum Safe Operating Area

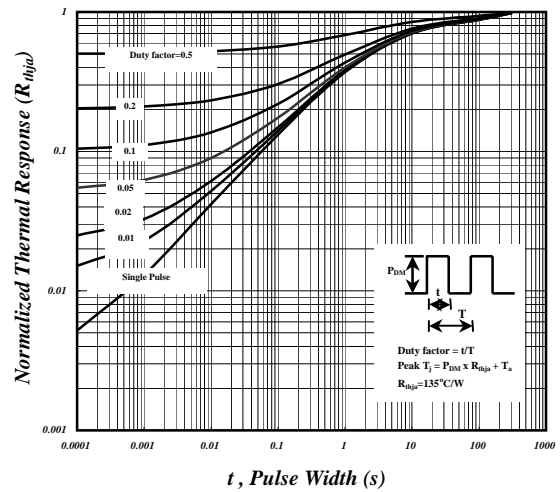


Fig 10. Effective Transient Thermal Impedance

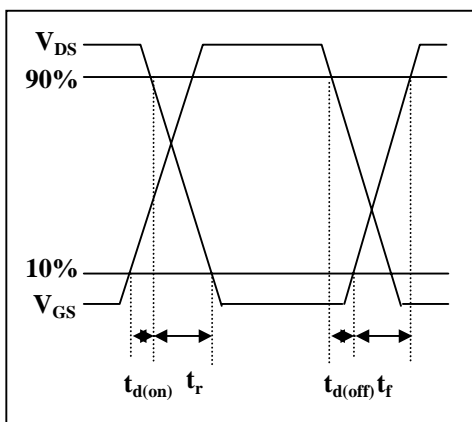


Fig 11. Switching Time Waveform

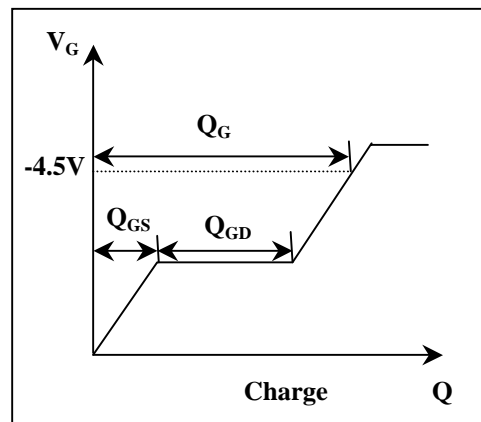


Fig 12. Gate Charge Waveform