HOPERF

CMT2119B

+20dBm High-power Sub-1GHz RF Transmitter

Characteristic

- Frequency range: 127 to 1020 MHz
- Modulation mode: OOK, (G) FSK and (G) MSK
- Data Rate: 0.5 to 300 kbps
- Voltage range: 1.8 to 3.6 V
- Emission current: 23 mA @ 13 dBm, 433.92 MHz, FSK
  72 mA @ 20 dBm, 433.92 MHz, FSK
- Supports Auto Tx mode
- Sleep current
- 300 nA (Deep sleep)
- 800 nA (Automatic operation)
- 3-wire SPI Interface
- Supports pass-through and packet modes
- Configurable packet handler and 64-Byte FIFO
- No Return to Zero, Manchester, Data Whitening encoding and decoding
- Support forward error correction
- 16-pin QFN3x3 package

Description

CMT2119B is an OOK, (G)FSK radio frequency transmitter with a maximum output power of 20dBm, high performance, and suitable for various wireless applications in the 127 to 1020MHz range.

It is part of CMOSTEK's NextGenRF™ radio frequency product line, which includes complete transmitters, receivers, and transceivers. The product line includes complete transmitters, receivers and transceivers. CMT2119B is highly integrated, simplifying the peripheral components required in system design. It has a transmission power of up to +20dBm,

which improves the link performance of applications. It supports multiple data packet formats and encoding/decoding methods, enabling it to flexibly meet the requirements of various applications for different data packet formats and encodings. And encoding and decoding mode,

so that it can flexibly meet the requirements of various applications for different data. In addition, CMT2119B also supports functions such as 64-byte Tx FIFO, abundant GPIO and interrupt configurations, Auto Tx operating mode, low-voltage detection, power-on reset, low-frequency clock output, and manual fast frequency hopping, making application design more flexible and enabling differentiated product design. CMT2119B operates at 1.8V to 3.6V.

It consumes only 23mA of transmit current when the output power is +13dBm, and 77mA of transmit current when the output power is +20dBm.

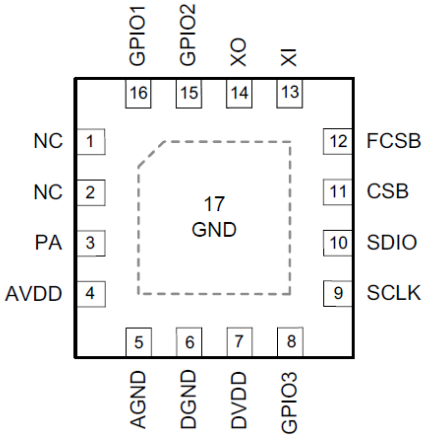
Applications

- Home security and building automation
- ISM band data communication
- Industrial Monitoring and Control
- Remote control and security system
- Remote Key Entry
- Wireless sensor node
- Tag reader/writer

Ordering Information

Part number	Frequency	Package	Minimum order quantity
CMT2119B-EQR	433.92MHz	QFN16	3,000 pcs
More ordering information: see chapter 9			

QFN16 (3X3)



CMT2119B Top View

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1 Electrical Characteristics

VDD = 3.3 V, TOP = 25 °C, FRF = 433.92 MHz. Unless otherwise stated, all results were tested on the evaluation version of CMT2119B-EM.

1.1 Recommended Operating Conditions

Table 1. Recommended operating conditions

Parameter	Symbo	Condition	Min	Typ	Max	Unit
Operating supply voltage	V_{DD}		1.8		3.6	V
Operating temperature	T_{OP}		-40		85	℃
Supply voltage slope			1			mV/us

1.2 Absolute Maximum Rating

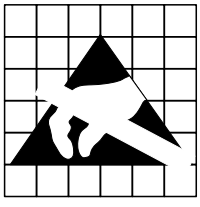
Table 2. Absolute Maximum Rating[1]

Parameter	Symbol	Condition	Minimum	Maximum	Unit
Power supply voltage	V_{DD}		-0.3	3.6	V
Interface voltage	V_{IN}		-0.3	3.6	V
Junction temperature	T_J		-40	125	℃
Storage temperature	T_{STG}		-50	150	℃
Welding temperature	T_{SDR}	Continue at least 30 seconds		255	℃
ESD level[2]		Human body model (HBM)	-2	2	kV
Latch current		@ 85℃	-100	100	mA

Remarks:

[1]. Exceeding the "absolute maximum ratings" may cause permanent damage to the device. This value is the pressure rating and does not mean that the device's function will be affected under this pressure condition. However, prolonged exposure to the absolute maximum rating conditions may affect the reliability of the device.

[2]. CMT2119B is a high-performance radio frequency integrated circuit. The operation and assembly of this chip should only be carried out on a workbench with good ESD protection.



Warning! ESD-sensitive components. When operating on the chip, attention should be paid to taking ESD prevention measures to avoid degradation of the chip's performance or loss of functionality.

1.3 Power Consumption

Table 3. Power Consumption Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Sleep current	I_{SLEEP}	Sleep mode, sleep counter is off		300		nA
		Sleep mode, sleep counter is on		800		nA
Standby current	$I_{Standby}$	Crystal oscillator is on		1.45		mA
TFS current	I_{TFS}	433 MHz		5.6		mA
		868 MHz		5.9		mA
		915 MHz		5.9		mA
TX current	I_{Tx}	FSK, 433 MHz, +20 dBm		72		mA
		FSK, 433 MHz, +13 dBm		23		mA
		FSK, 433 MHz, +10 dBm		18		mA
		FSK, 433 MHz, -10 dBm		8		mA
		FSK, 868 MHz, +20 dBm		87		mA
		FSK, 868 MHz, +13 dBm		27		mA
		FSK, 868 MHz, +10 dBm		19		mA
		FSK, 868 MHz, -10 dBm		8		mA
		FSK, 915 MHz, +20 dBm		70		mA
		FSK, 915 MHz, +13 dBm		28		mA
		FSK, 915 MHz, +10 dBm		19		mA
		FSK, 915 MHz, -10 dBm		8		mA

1.4 Receiver

Table 4. Receiver Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output power	P_{OUT}	Different frequency bands require specific peripheral materials	-20		+20	dBm
Output power step	P_{STEP}			1		dB
GFSK Gaussian filter coefficient	BT		0.3	0.5	1.0	-
Changes in output power at	$P_{OUT-TOP}$	Temperature from -40 to +85℃		1		dB
Transmit spurious radiation		P_{OUT} = +13 dBm，433MHz，FRF < 1 GHz				
		1 GHz to 12.75 GHz, including harmonics			-36	dBm
F_{RF} = Harmonic output with 433 MHz	$H2_{433}$	2 time harmonics, +20 dBm P_{OUT}		-46		dBm
	$H3_{433}$	3 time harmonics, +20 dBm P_{OUT}		-50		dBm
F_{RF} = Harmonic output with 868 MHz	$H2_{868}$	2 time harmonics, +20 dBm P_{OUT}		-43		dBm
	$H3_{868}$	3 time harmonics, +20 dBm P_{OUT}		-52		dBm
F_{RF} = Harmonic output with 915 MHz	$H2_{915}$	2 time harmonics, +20 dBm P_{OUT}		-48		dBm
	$H3_{915}$	3 time harmonics, +20 dBm P_{OUT}		-53		dBm

Parameter	Symbol	Condition	Min	Typ	Max	Unit
F_{RF} = Harmonic output with 433 MHz	$H2_{433}$	2 time harmonics, +13 dBm P_{OUT}		-52		dBm
	$H3_{433}$	3 time harmonics, +13 dBm P_{OUT}		-52		dBm
F_{RF} = Harmonic output with 868 MHz	$H2_{868}$	2 time harmonics, +13 dBm P_{OUT}		-52		dBm
	$H3_{868}$	3 time harmonics, +13 dBm P_{OUT}		-52		dBm
F_{RF} = Harmonic output with 915 MHz	$H2_{915}$	2 time harmonics, +13 dBm P_{OUT}		-52		dBm
	$H3_{915}$	3 time harmonics, +13 dBm P_{OUT}		-52		dBm

1.5 Stabilization Time

Table 5. Stabilization Time

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Stabilization time	T_{SLP-TX}	From Sleep to TX		1000		us
	T_{STB-TX}	From Standby to TX		300		us
	T_{TFS-TX}	From TFS to TX		10		us

1.6 Frequency Synthesizer

Table 6. Frequency Synthesizer Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Frequency Range	F_{RF}	Requires different matching networks	760		1020	MHz
			380		510	MHz
			190		340	MHz
			127		170	MHz
Synthesizer frequency	F_{RES}			25		Hz
Frequency tuning time	t_{TUNE}			150		us
Phase Noise @ 433 MHz	PN_{433}	10 kHz Frequency offset		-94		dBc/Hz
		100 kHz Frequency offset		-99		dBc/Hz
		500 kHz Frequency offset		-118		dBc/Hz
		1 MHz Frequency offset		-127		dBc/Hz
		10 MHz Frequency offset		-134		dBc/Hz
Phase Noise @ 868 MHz	PN_{868}	10 kHz Frequency offset		-92		dBc/Hz
		100 kHz Frequency offset		-95		dBc/Hz
		500 kHz Frequency offset		-114		dBc/Hz
		1 MHz Frequency offset		-121		dBc/Hz
		10 MHz Frequency offset		-130		dBc/Hz
Phase Noise @ 915 MHz	PN_{915}	10 kHz Frequency offset		-89		dBc/Hz
		100 kHz Frequency offset		-92		dBc/Hz
		500 kHz Frequency offset		-111		dBc/Hz
		1 MHz Frequency offset		-121		dBc/Hz
		10 MHz Frequency offset		-130		dBc/Hz

1.7 Low Voltage Detection

Table 7. Low Voltage Detection Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low voltage detection	LBD_{RES}			50		mV

1.8 Crystal

Table 8. Crystal Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Crystal frequency[1]	F_{XTAL}			26		MHz
Crystal frequency tolerance[2]	ppm			20		ppm
Load capacitance	C_{LOAD}			15		pF
Crystal equivalent resistance	Rm			60		Ω
Crystal start time[3]	t_{XTAL}			800		us

Remark:

[1]. The CMT2119B can directly use an external reference clock to drive the XI pin through a coupling capacitor. The peak-to-peak value of the external clock signal is required to be between 0.3V and 0.7V.

[2]. The value includes (1) Initial error; (2) Crystal load; (3) Aging; (4) Changes with temperature. The acceptable crystal frequency error is limited by the receiver's bandwidth and the radio frequency deviation between the matched transmitter.

[3]. This parameter is largely related to crystals.

1.9 Low Frequency Oscillator

Table 9. Low Frequency Oscillator Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Calibration	F_{LPOSC}			32		kHz
Frequency		After calibration		1		%
Temperature				-0.02		%/°C
Supply voltage				+0.5		%/V
Initial	$t_{LPOSC-CAL}$			4		ms

Remark:

[1]. The low-frequency oscillator is automatically calibrated to the crystal oscillator frequency during the PUP phase and is calibrated periodically during this phase.

[2]. The drift of frequency with temperature change after calibration.

[3]. The calibrated frequency drifts as the power supply voltage changes.

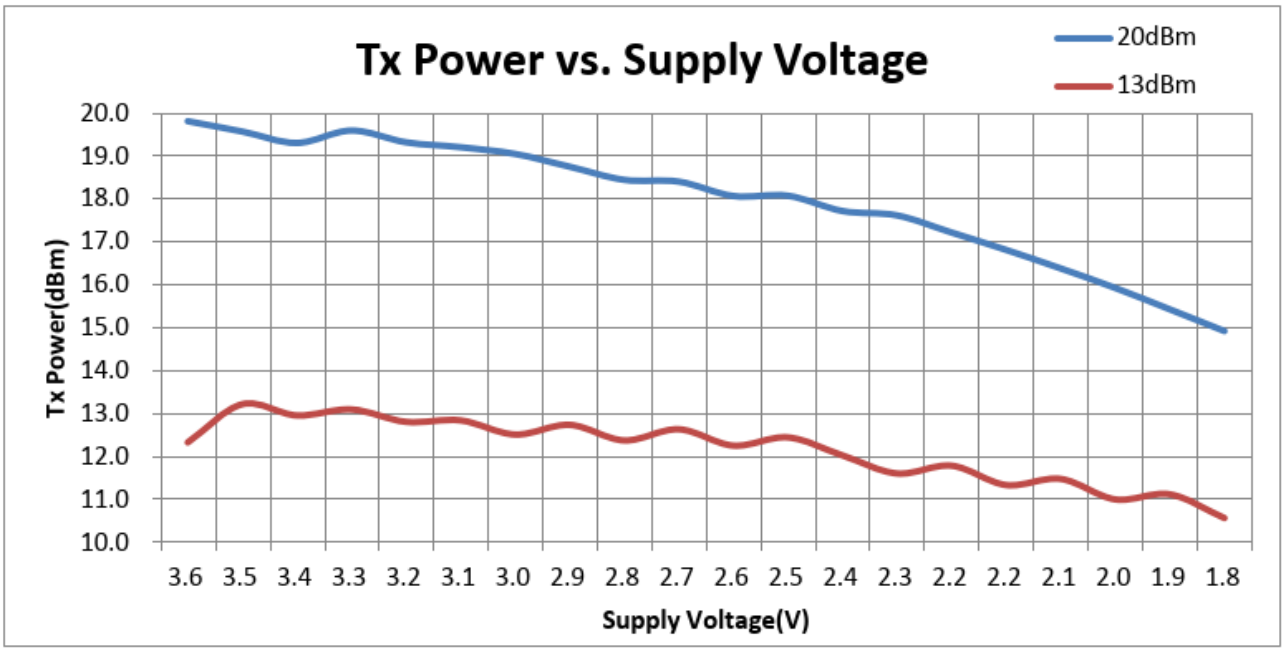
1.10 Digital Interface

Table 10. Digital Interface Specifications

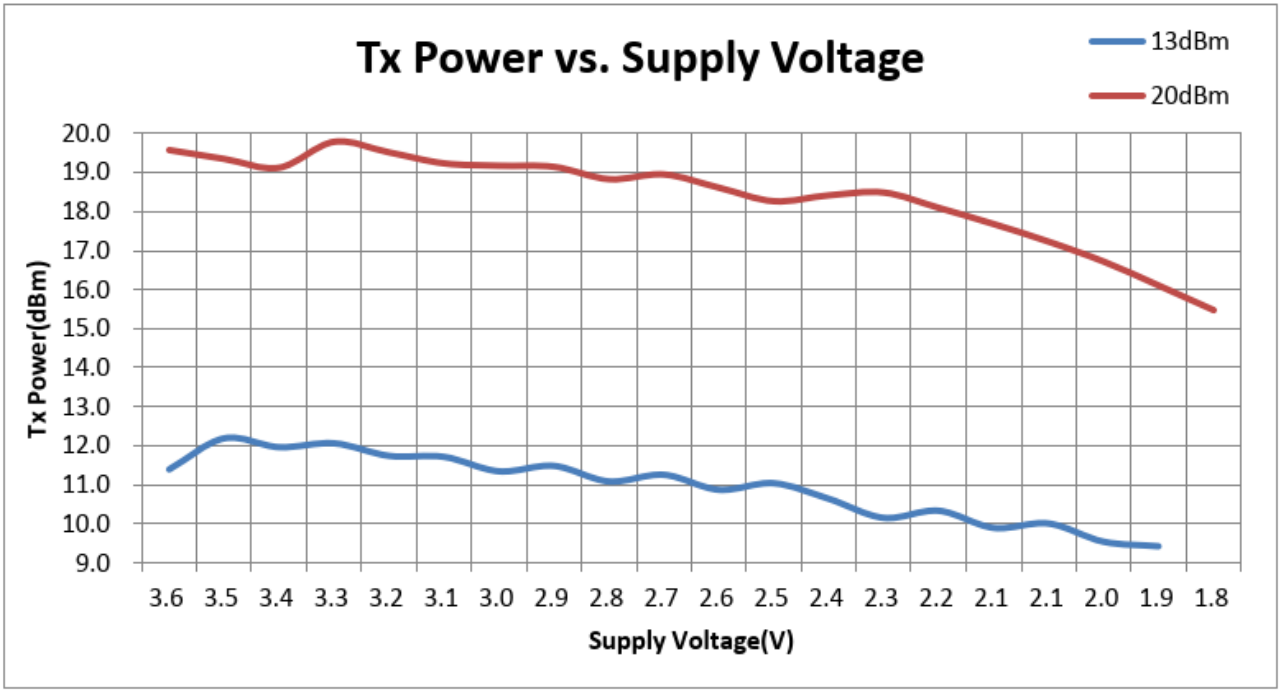
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Digital signal inputs high	V_{IH}		0.8			V_{DD}
Digital signal inputs low level	V_{IL}				0.2	V_{DD}
Digital signal outputs high	V_{OH}	@ I_{OH} = -0.5 mA	Vdd-0. 4			V
Digital signal outputs low	V_{OL}	@ I_{OL}= 0.5 mA			0.4	V
SCL Frequency	F_{SCL}				5	MHz
SCL is high time	T_{CH}		50			ns
SCL is low time	T_{CL}		50			ns
SCL rising edge time	T_{CR}		50			ns
SCL falling edge time	T_{CF}		50			ns

1.11 Typical Parameter Chart

1.11.1 Transmit Power vs. Supply Voltage Curve

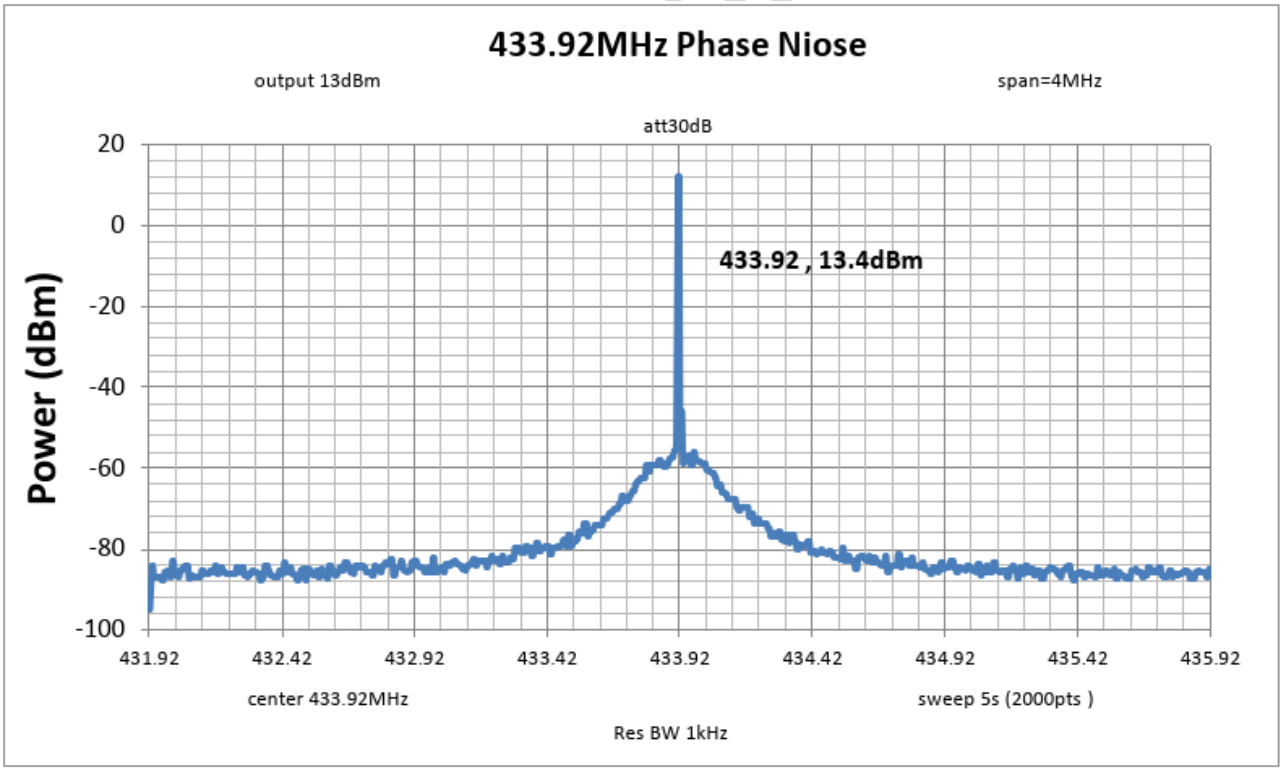


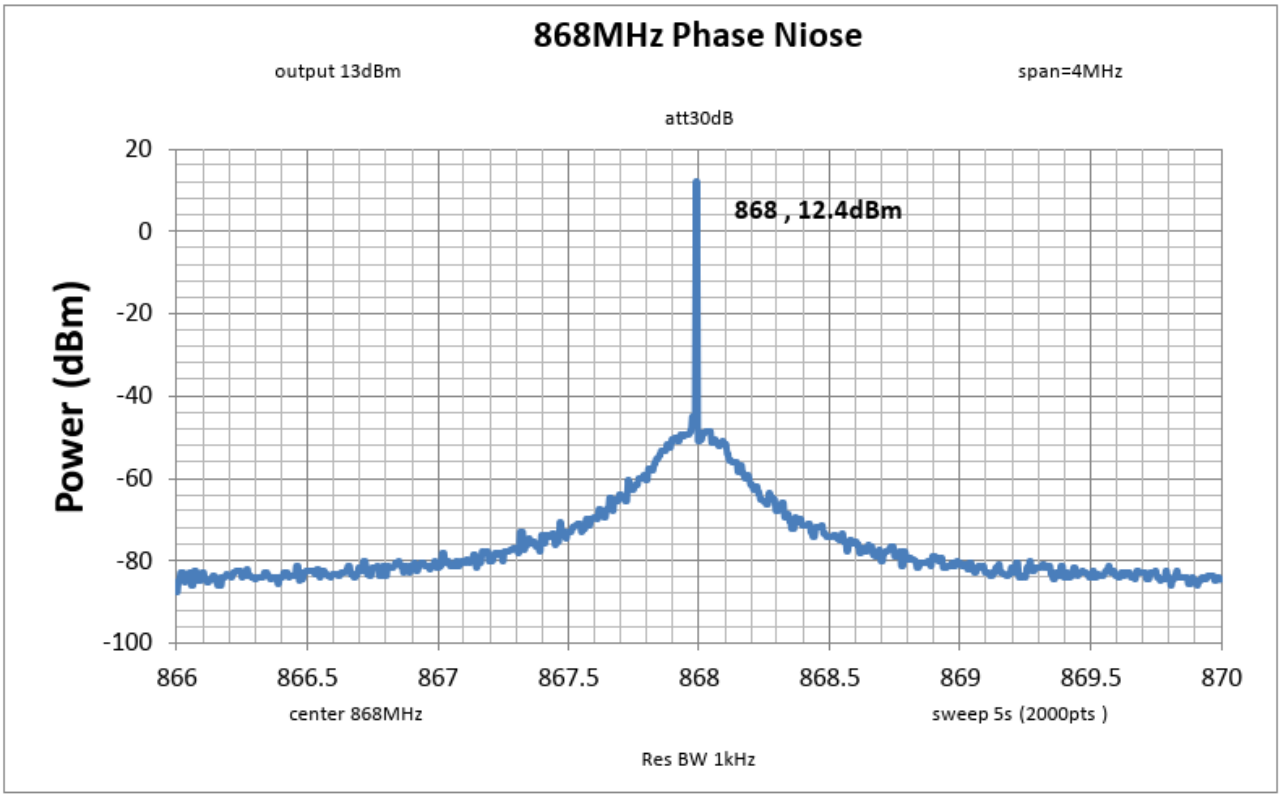
Test conditions: Freq = 434 MHz, 20 dBm/13 dBm matching network



Test conditions: Freq = 868 MHz, 20 dBm/13 dBm Matching network

1.11.2 Transmit Phase Noise





2 Pin Description

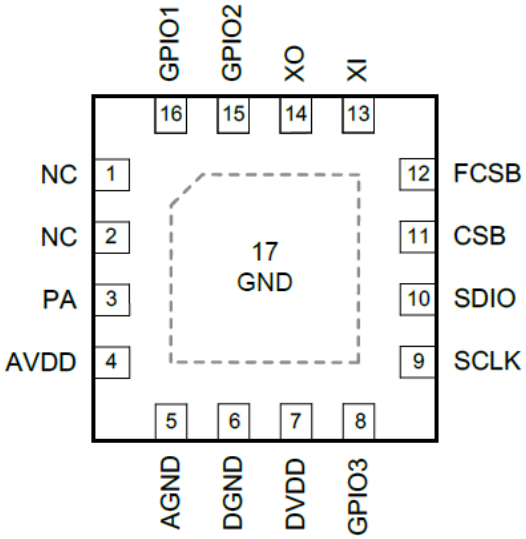


Figure 1. CMT2119B Pin Arrangement

Table 11. CMT2119B Pin Description

Pin number	Name	I/O	Function description
1	NC	-	hanging

2	NC	-	hanging
3	PA	O	PA Output
4	AVDD	IO	Analog VDD
5	AGND	IO	Analog GND
6	DGND	IO	Digital GND
7	DVDD	IO	Digital VDD
8[1]	GPIO3	IO	Can be configured as: CLKO，INT2，DCLK (TX)
9	SCLK	I	The clock of SPI
10	SDIO	IO	SPI data input and output
11	CSB	I	Chip select for SPI access to registers
12	FCSB	I	Chip select for SPI accessing FIFO
13	XI	I	Crystal circuit input
14	XO	O	Crystal circuit output
15[1]	GPIO2	IO	Can be configured as: INT1，INT2，DCLK (TX)
16[2]	GPIO1	IO	Can be configured as: DIN，INT1，INT2，DCLK (TX)
17	GND	I	Analog GND, must be grounded

Remarks:

[1]. INT1 and INT2 refer to two interrupt functions; DCLK (TX) is the modulation data rate synchronization clock, which switches automatically when switching in TX mode.

[2]. DIN is the external modulation data input port in pass-through mode, and only the GPIO1 pin has this function.

3 Typical Application Schematic

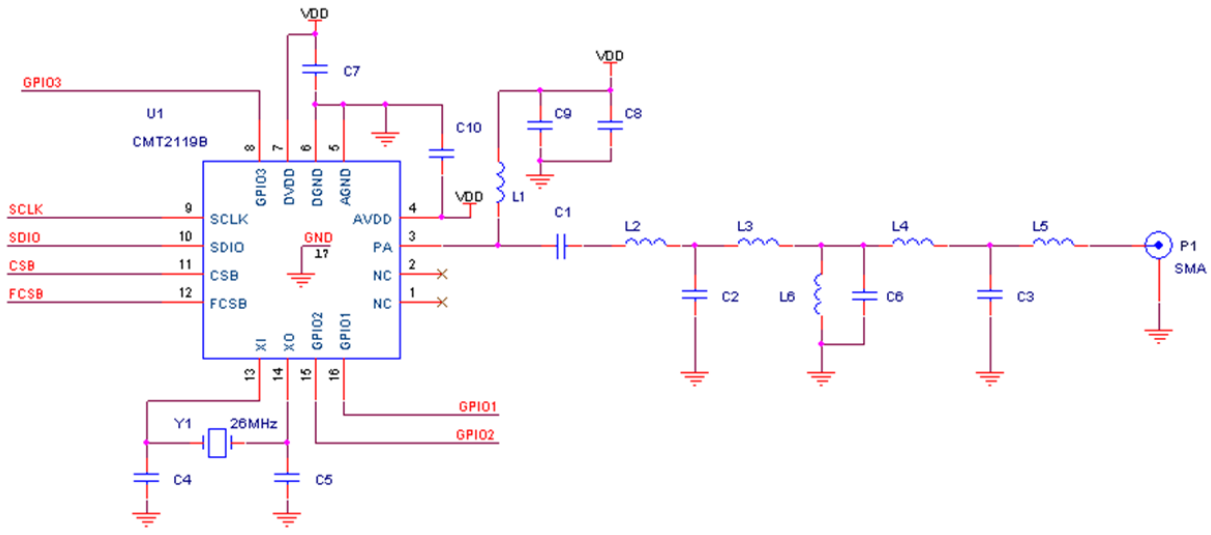


Figure 2. Typical Application Schematic

Table 12. Bill of Materials for Typical Applications

Signal	Description	Component value			Unit	Suppliers
		433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
C1	± 5%, 0603 NP0, 50 V	15	18	18	pF	-
C2	± 5%, 0603 NP0, 50 V	3	3.6	3.6	pF	-
C3	± 5%, 0603 NP0, 50 V	6.2	3.3	3.3	pF	-
C4	± 5%, 0603 NP0, 50 V	27	27	27	pF	-
C5	± 5%, 0603 NP0, 50 V	27	27	27	pF	-
C6	± 5%, 0603 NP0, 50 V	4.7	2	1.8	pF	-
C7	± 5%, 0603 NP0, 50 V	0.1			uF	-
C8	± 5%, 0603 NP0, 50 V	4.7			uF	-
C9	± 5%, 0603 NP0, 50 V	470			pF	-
C10	± 5%, 0603 NP0, 50 V	0.1			uF	-
L1	±5%, 0603 laminated chip inductor	180	100	100	nH	Sunlord SDCL
L2	±5%, 0603 Laminated patch inductors,	22	12	12	nH	Sunlord SDCL
L3	±5%, 0603 laminated chip inductor	Capacitanc	15	15	nH	Sunlord SDCL
L4	±5%, 0603 laminated chip inductor	33	6.2	6.2	nH	Sunlord SDCL
L5	±5%, 0603 laminated chip inductor	33	6.2	6.2	nH	Sunlord SDCL
L6	±5%, 0603 laminated chip inductor	27	15	15	nH	Sunlord SDCL
Y1	± 10 ppm, SMD 32 * 25 mm	26			MHz	EPSON
U1	CMT2119B, +20 dBm high-power Sub-1GHz transmitter	-			-	CMOSTEK

4 Functional Description

CMT2119B is a high-performance transmitting chip suitable for applications in the 127 to 1020 MHz range, supporting OOK, (G)FSK, and (G)MSK modulation modes. This product belongs to the CMOSTEK NextGenRF™ series, which includes a complete range of products such as transmitters, receivers, and transceivers. The internal system block diagram of CMT2119B is shown in the following figure.

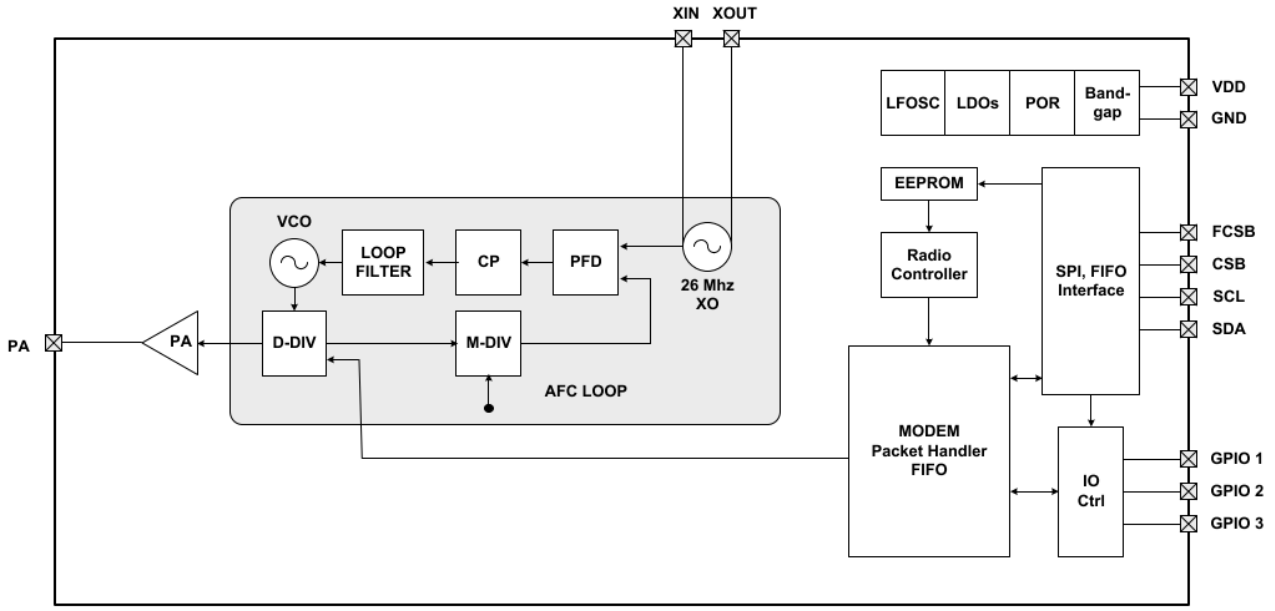


Figure 4-1. Functional system block diagram

In the transmitter system, the digital circuit encodes and packages the data, and sends the processed data to the modulator (it can also be sent directly to the modulator without encoding and packaging). The modulator directly controls the PLL and PA, modulates the data using (G)FSK or OOK, and transmits it.

4.1 Transmitter

The CMT2119B transmitter is a transmitter based on direct radio frequency synthesis. Its carrier frequency is generated by a low-noise fractional-N frequency synthesizer.

The modulated data is transmitted by an efficient single-ended power amplifier (PA). The output power can be read and written via registers, and can be configured from -10dBm to +20dBm in 1dB steps.

When the PA is switched rapidly, the sudden change in its input impedance momentarily interferes with the output frequency of the VCO. This effect is called VCO pulling, which generates spectral spurs and glitches around the desired carrier. By slowly ramping the output power of the PA, the transient glitches of the PA can be minimized. The CMT2119B has a built-in mechanism for slow ramping up and down of the PA. When PA Ramp is enabled, the PA output power can slowly ramp up and down to the required amplitude at a set rate, so as to reduce unwanted spectral components.

According to different application requirements, users can design a PA matching network to optimize the transmission efficiency under the required output power. The typical application schematic diagram and the required BOM statement are the same as those in Chapter 3 "Typical Application Schematic Diagram". For more details on application schematics and layout guidelines, please refer to AN168 "CMT2119B Schematic and PCB Layout Design Guide".

The transmitter can operate in through mode and packet mode. In pass-through mode, the data to be transmitted is directly sent into the chip through the DIN pin of the chip and then transmitted immediately. In packet mode, data can be pre-loaded into the chip's FIFO in STBY, TFS, and Tx states, and then transmitted together with other packet elements.

4.2 Auxiliary Module

4.2.1 Crystal Oscillator

Crystal oscillators are used to provide a reference clock for phase-locked loops and a system clock for digital modules. The load capacitance depends on the crystal's specified CL parameter. The total load capacitance between XI and XO should be equal to CL to ensure that the crystal oscillates accurately at 26 MHz.

$$C_L = \frac{1}{1/C11 + 1/C12} + C_{par} + 2.5pF$$

C9 and C10 are the load capacitances connected to both ends of the crystal respectively, and Cpar is the parasitic capacitance of the PCB. The differential equivalent of the 5pF capacitor added inside the chip is 2.5pF. The equivalent series resistance of the crystal should be within the specified range to ensure reliable oscillation of the crystal. It is also possible to replace the conventional crystal with an external signal source connected to the XI pin. The peak-to-peak value of this clock signal is recommended to be between 300mV and 700mV, and it is capacitively coupled to the XI pin.

4.2.2 Sleep Timer

The CMT2119B integrates a sleep timer driven by a 32 kHz low power oscillator (LPOSC). When this function is enabled, the timer periodically wakes the chip from sleep mode. When the chip operates in periodic mode, the sleep time can be configured from 0.03125 ms to 41,922,560 ms. Since the frequency of the low-power oscillator drifts with changes in temperature and voltage, it will be automatically calibrated during the power-up phase and will be calibrated periodically. These calibrations will keep the frequency tolerance of the oscillator within ±1%.

4.2.3 Low Voltage Detection

The chip is equipped with a low-voltage detection function. This detection is performed every time the chip is tuned to a certain frequency. Frequency tuning is performed whenever the chip transitions from SLEEP/STBY state to TFS/TX state. The detection result can be read through the LBD _ VALUE register.

If LBD_STOP_EN is set to 1, when the power supply voltage is detected to be lower than the preset value, the chip will stop at the LOW_VDD stage (CHIP_MODE_STA<3:0> = 1000, Addr = 0x61) and wait for the MCU to send a command via SPI to switch the chip to SLEEP or Standby mode.

4.2.4 Fast Manual Frequency Hopping

In applications that require multiple channels, users do not need to configure complex registers every time they change the frequency. Instead, they only need to configure one register based on the base frequency to achieve this.

FREQ= Basic frequency point + 2.5=2.5kHz × FH_OFFSET < 7:0> × FH_CHANNEL < 7:0 >

Generally speaking, users can first set FH_OFFSET<7:0> (Addr=0x64) during the power-on initialization

configuration phase, and then continuously modify FH_CHANNEL<7:0> (Addr=0x63) in the application to switch channels.

4.2.5 Power On Reset (POR)

The power-on reset circuit helps detect power supply changes and generates corresponding reset signals to reset the entire CMT2119B system. After POR, the MCU needs to reinitialize the CMT2119B. There are two situations that will cause the POR to reset.

The first scenario is when the power supply voltage drops to 0.3V (+/-20%), the POR changes from reset to 0, and then when the power supply voltage rises to 1.45V (+/-20%) at a rate greater than 1V/ms, the POR changes from 0 to 1. As shown in the following figure:

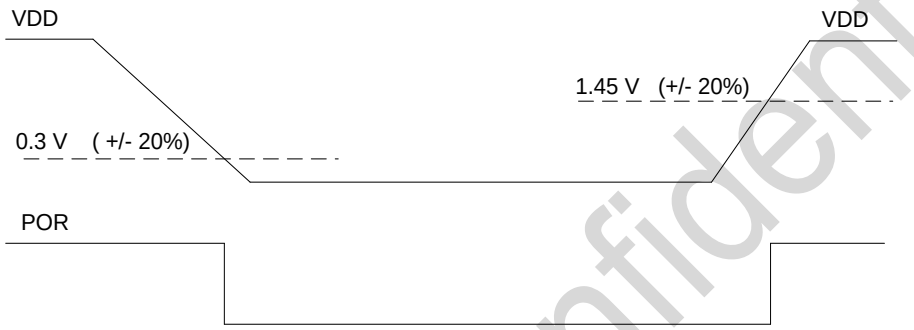


Figure 4-2. POR Reset Caused by Supply Voltage Drop

The second situation is that a brief power supply mutation causes the POR to generate a reset. The triggering condition is that VDD drops sharply by 0.9V (+/-20%) within less than 2us. Note that it monitors the drop amplitude of VDD, not the absolute value of VDD. As shown in the following figure:

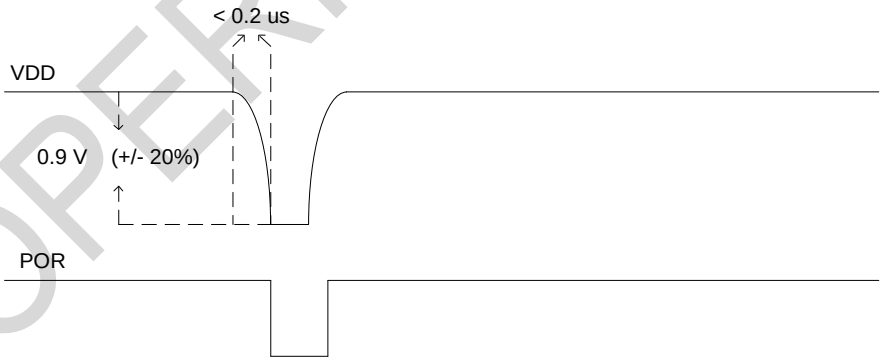


Figure 4-3. The Rapid Drop of the Supply Voltage Causes the POR to Reset

5 Chip operation

5.1 SPI interface

Communication between the MCU and the chip is carried out through a 4-wire SPI interface.

Low-efficiency CSB means that the MCU needs to access the chip's registers. A low-effective FCSB means that the MCU needs to access the FIFO of the chip. CSB and FCSB cannot be low at the same time. SCLK is the serial port clock. For MCUs and chips, data is always transmitted on the falling edge of the SCLK and sampled on the rising edge. SDIO is a bi-directional data pin. Addresses and data are always sent starting from the MSB.

When accessing a register, an R/W (read/write) bit needs to be sent, followed by a 7-bit register address. Before sending it to the R/W bit, the MCU must pull CSB low for at least half an SCLK cycle. After sending the last SCLK falling edge, the MCU must wait for at least half an SCLK cycle before pulling CSB high again.

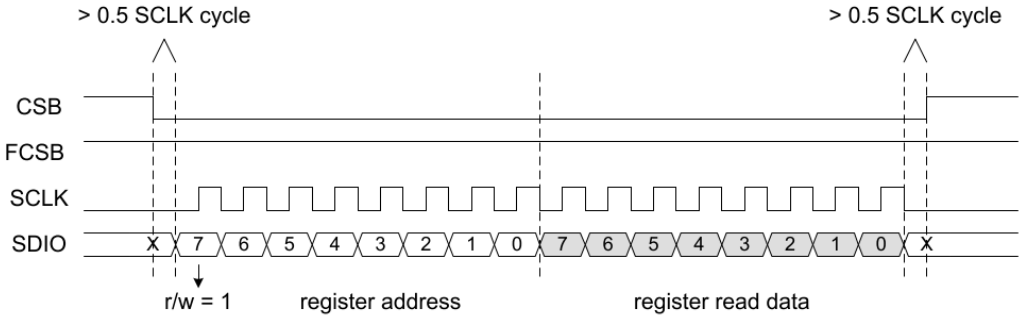


Figure 5-1. SPI Read Register Timing Sequence

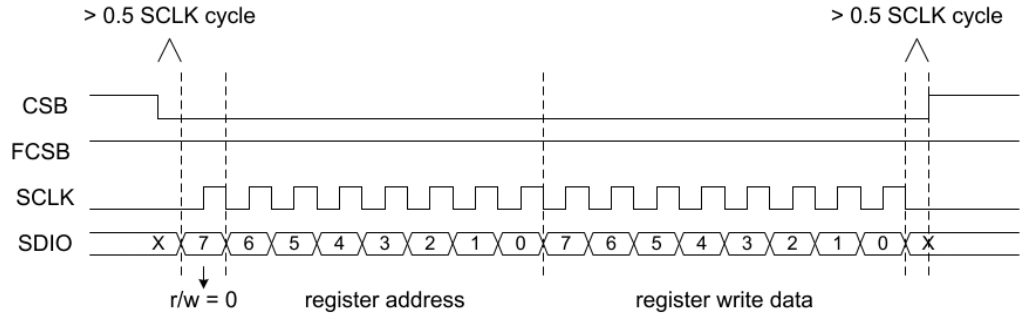


Figure 5-2. SPI Write Register Timing Sequence

5.2 FIFO

The FIFO is used to store data to be transmitted in Tx mode. The FIFO can be read through the SPI interface. The user can clear the FIFO by setting the FIFO_CLR_TX (Addr = 0x6C) bit. Moreover, users can repeatedly transmit the previously entered data by setting FIFO_RESTORE without having to re-enter the data.

By setting the register FIFO_MERGE_EN (Addr=0x69), users can choose to use different FIFO depths of only 32 bytes or 64 bytes. When the FIFO is 64 bytes, it means that the maximum number of bytes that can be stored in the chip is 64 bytes.

5.2.1 FIFO Read Operation

When reading data from the FIFO, each time a byte is read, the internal read pointer automatically increments by 1. The MCU must pull FCSB low for one SCLK cycle to release the rising edge of the first SCLK. After issuing the last SCLK falling edge, the MCU must wait for at least 2 us before pulling the

FCSB back to high. Moreover, before reading the next byte of the FIFO, the FCSB needs to be pulled high for at least 4 us. It enables the chip to generate corresponding FIFO interrupts according to the current situation.

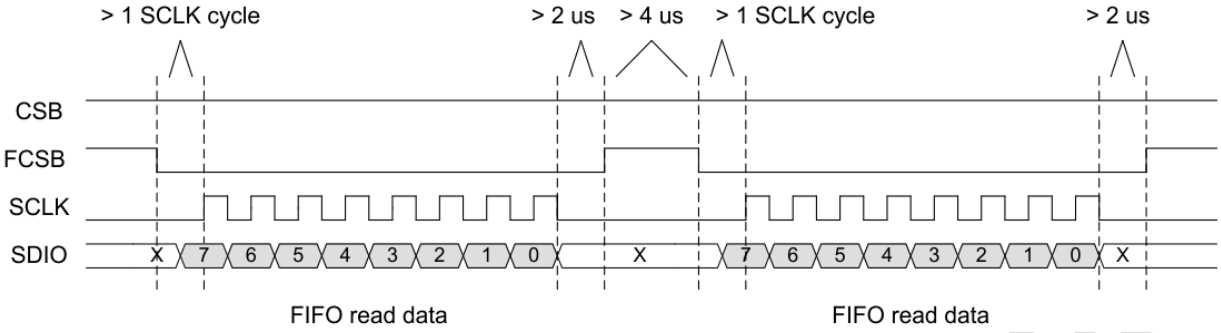
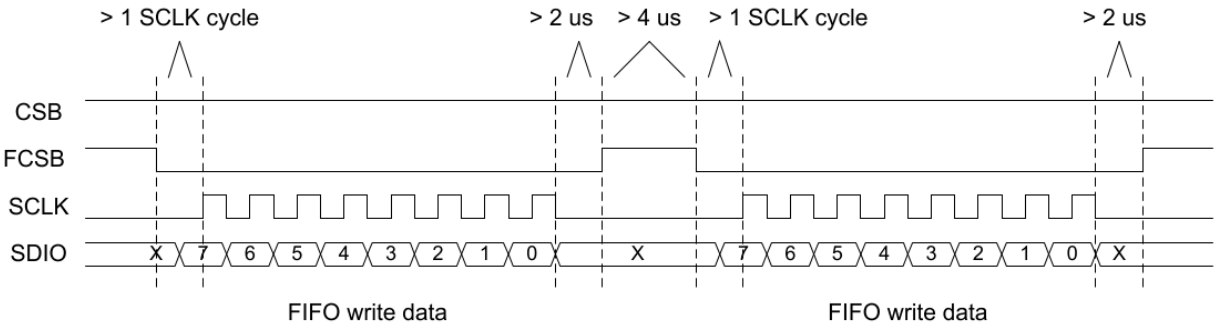


Figure 6. SPI Read FIFO Timing Sequence

5.2.2 FIFO Write Operation

When writing to a FIFO, each time a byte is written, the internal read pointer automatically increments by 1. Data on SDIO is sampled on the rising edge of SCLK. The MCU must pull FCSB low for one SCLK cycle to release the rising edge of the first SCLK. After sending the last SCLK falling edge, the MCU must wait for at least 2us before pulling FCSB back to a high level. Moreover, before writing the next byte into the FIFO, FCSB needs to be pulled high for at least 4 us. It enables the chip to generate corresponding FIFO interrupts according to the current situation.



5.2.3 FIFO-related Interrupts

CMT2119B provides abundant FIFO-related interrupt sources, which serve as an auxiliary means for the efficient operation of the chip. The timing sequence of Tx-related FIFO interrupts is shown in the following figure.

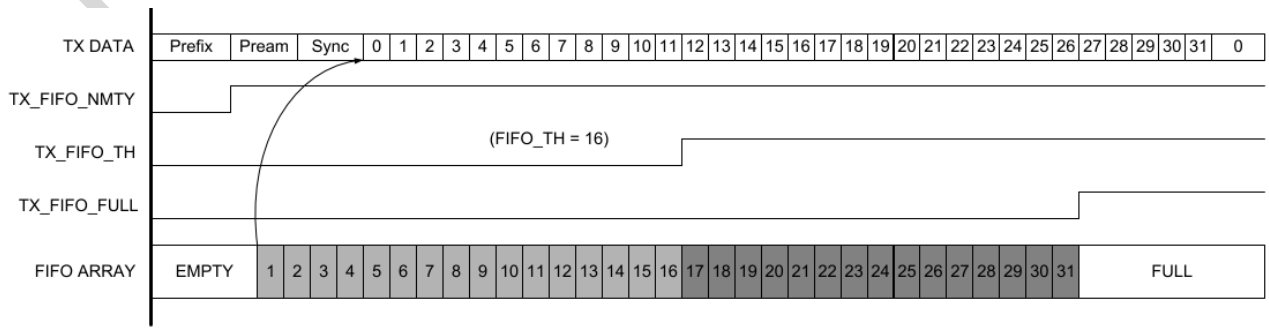


Figure 8. Schematic Diagram of TX FIFO Interrupt Timing

5.3 Working Status, Timing and Power Consumption

5.3.1 Startup Sequence

After the chip is powered on at VDD, it usually takes about 1ms for the POR to be released. After the POR is released, the crystal will also start, with a default startup time of Nms, which depends on the crystal's own characteristics. After startup, the system must wait for the crystal to stabilize before it can start working. The default stabilization time is 2.48 ms, which can be modified later by writing to XTAL_STB_TIME <2:0> (Addr=0x0E). Before the crystal stabilizes, the chip will remain in the IDLE state. After the crystal stabilizes, the chip will exit IDLE and start calibrating each module. After the chip completes calibration, it will stay in SLEEP mode, waiting for the user to perform initial configuration. At any time, as long as a reset is performed, the chip will return to IDLE and restart the power-on process.

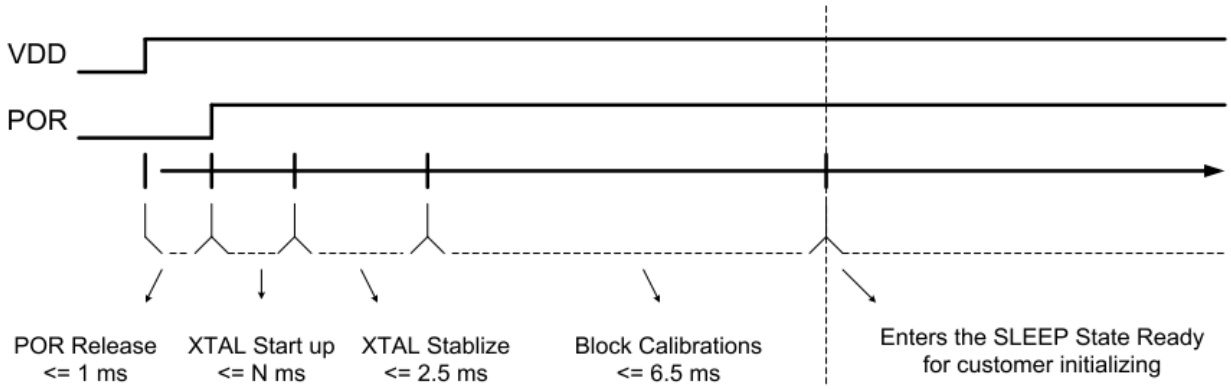


Figure 9. Power-on Sequence

After calibration is completed, the chip enters SLEEP mode. From this point on, the MCU can switch the chip to different operating states by setting the register HIP_MODE_SWT<7:0> (Addr=0x60).

5.3.2 Working Status

CMT2119B has a total of 5 working states: IDLE, SLEEP, STBY, TFS and TX, as listed in the following table.

Table 13. CMT2119B Status and Module Enable Table

Status	Binary code	Command Switching	Open Module	Optional enabled module
IDLE	0000	soft_rst	SPI, POR	None
SLEEP	0001	go_sleep	SPI, POR, FIFO	LFOSC, Sleep Timer
STBY	0010	go_stby	SPI, POR, XTAL, FIFO	CLKO
TFS	0100	go_tfs	SPI, POR, XTAL, PLL, FIFO	CLKO
TX	0110	go_tx	SPI, POR, XTAL, PLL, PA, FIFO	CLKO

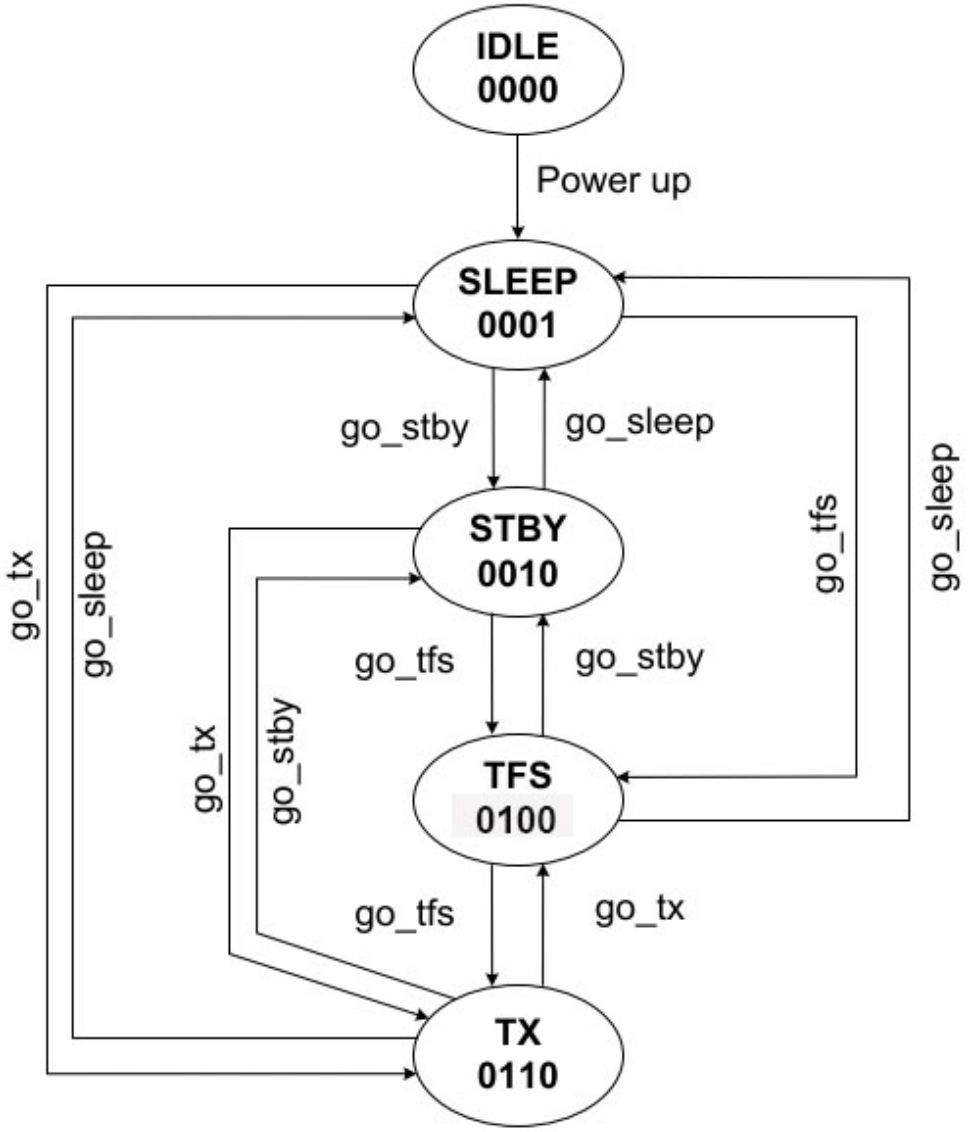


Figure 10. State Switching Diagram

- SLEEP Status

The power consumption of the chip under SLEEP state is the lowest, and almost all modules are turned off. SPI is enabled. The registers in the configuration area and control area 1 can be accessed. The content previously filled in the FIFO will remain unchanged, but the FIFO cannot be operated on. If the user has enabled the timed wake-up function, then LFOSC and the sleep counter will be activated and start working. The time required to switch from IDLE to SLEEP is the power-on process time introduced above. Switching from any other state to SLEEP will be completed immediately.

- STBY state

In STBY mode, the crystal is turned on, the LDO of the digital circuit is also turned on, the current will increase slightly, and the FIFO can be operated. Users can choose whether to output CLKO (system clock) to the GPIOn pin. Since the crystal is turned on, the time required to switch from STBY to emission is shorter than that of SLEEP. Switching from SLEEP to STBY can only be completed after

waiting for the crystal to turn on and stabilize. Switching from other states to STBY will be completed immediately.

- TFS state

TFS is a transitional state before switching to TX. Except that the RF module of the transmitter is turned off, all other modules are turned on, and the current will be larger than that in STBY. Switching from STBY to TFS takes approximately 350us for PLL calibration and stabilization. Switching from SLEEP to TFS requires additional time for crystal startup and stabilization. Switching from other states to TFS will be completed immediately.

- TX State

All modules related to transmitters in TX will be turned on. Switching from TFS to TX only takes 20us. Switching from STBY to TX requires adding a 350us PLL calibration and stabilization time. Switching from SLEEP to TX requires adding time for the crystal to start up and stabilize.

5.4 Working State, Timing and Power Consumption

CMT2119B has 3 GPIOs, each of which can be configured as different inputs or outputs; CMT2119B has 2 interrupt ports, which can be configured to different GPIO outputs.

Table 14. CMT2119B GPIO

Pin	Pin	I/O	Function
16	GPIO1	IO	Can be configured as: DIN, INT1, INT2, DCLK (TX)
15	GPIO2	IO	Can be configured as: INT1, INT2, DCLK (TX)
8	GPIO3	IO	Can be configured as: CLKO, INT2, DCLK (TX)

The interrupt mapping table is given below. The mappings of INT1 and INT2 are the same, and the following explanation will take INT1 as an example.

Table 15. CMT2119B Interrupt Mapping

Name	INT1_SEL	Description	Cleaning
TX _ ACTIVE	00001	Indicates the interrupts that are ready to enter TX and have already	Auto
SL_TMO	01000	An interrupt indicating that the SLEEP counter has timed out	by MCU
TX_DONE	01010	Interrupt indicating TX completion	by MCU
TX_FIFO_NMTY	10000	An interrupt indicating that the TX FIFO is not empty	Auto
TX_FIFO_TH	10001	An interrupt indicating that the unread content in the TX FIFO exceeds	Auto
TX_FIFO_FULL	10010	Interrupt indicating that TX FIFO is full	Auto
STATE_IS_STBY	10011	An interrupt indicating that the current state is STBY	Auto
STATE_IS_FS	10100	An interrupt indicating that the current state is TFS	Auto
STATE_IS_TX	10110	An interrupt indicating that the current state is TX	Auto
LBD	10111	An interrupt indicating that low voltage detection is active (VDD is	Auto

By default, interrupts are 1 active-high. However, by setting the bit of the register INT_POLAR with address 0x666 to 1, all interrupts can be changed to 0 active-low. Taking INT1 as an example again, the control and selection diagram of all interrupt sources is drawn below. For control and mapping, INT1 and INT2 are the same.

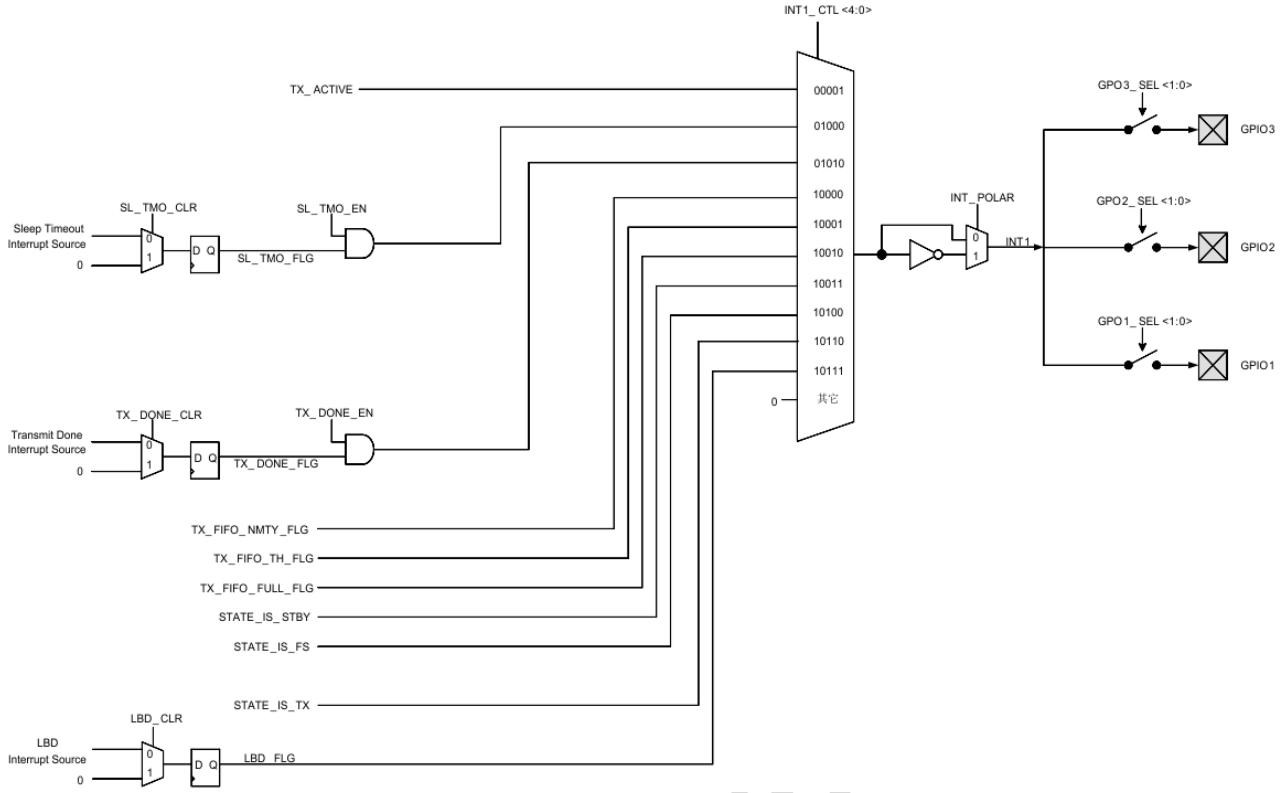


Figure 11. CMT2119B INT1 Interrupt Mapping

6 Data Packet and Packet Processor

6.1 Packet Format

CMT2119B adopts a relatively typical and flexible packet format, which can be divided into three types: variable packets (with Length before Node ID), variable packets (with Length after Node ID), and fixed packets. They are respectively expressed as follows:

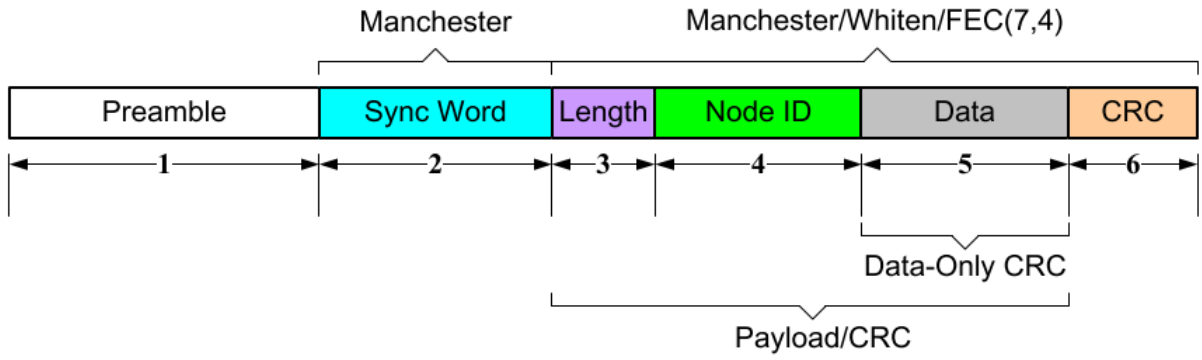


Figure 12. Variable packet (Length in front of Node ID)

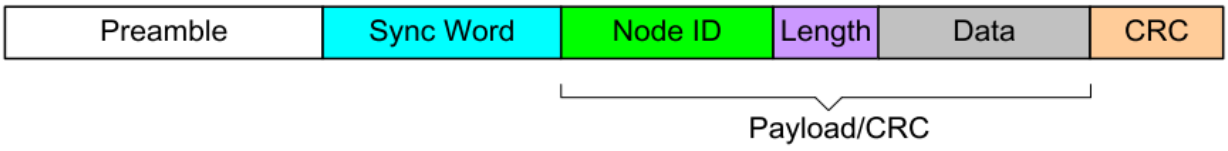


Figure 13. Variable packet (Length after Node ID)

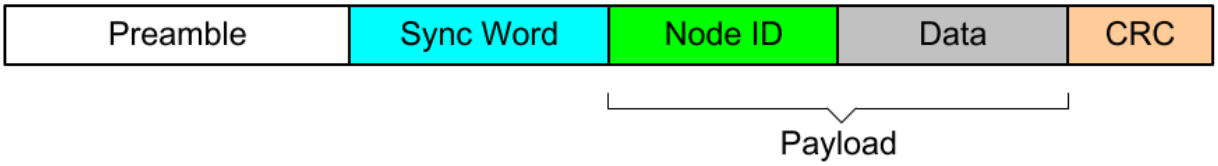


Figure 14. Fixed packet

6.2 Data Mode

Data Mode refers to the mode in which the external MCU inputs and transmits data. CMT2119B supports pass-through mode and packet mode. The differences are as follows.

- Direct-direct mode, FIFO does not work
- Packet-packet mode, supports all package format configurations, work in FIFO

6.2.1 Direct Mode

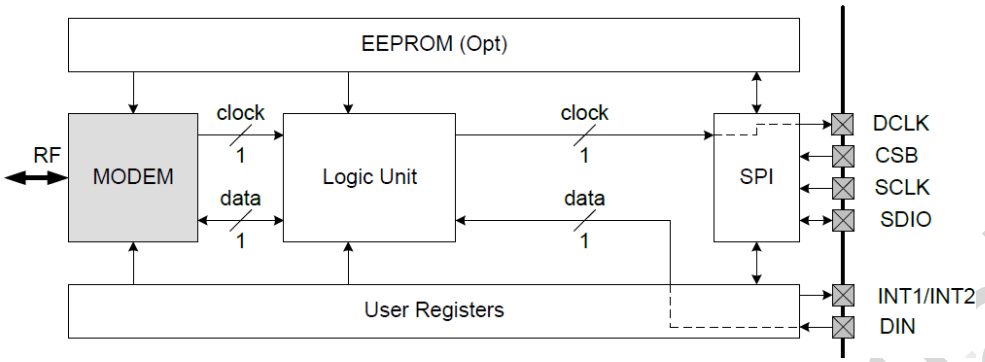


Figure 15. Data Path in Direct Mode

In direct mode, the data to be transmitted is directly sent into the chip by the external MCU through the chip's DIN, and the data rate can be specified by the MCU as long as it is within the chip's usage specifications. However, if the GFSK modulation method is used, it is necessary to configure the data rate of the chip in advance, and the data rate transmitted by the MCU must be within the specified tolerance range. The typical working sequence of Tx in pass-through mode is as follows.

1. Drive the DIN, that is, the GPIO1 pin, with a logic 0 or 1. (The system defaults the GPIO1 pin to the DIN function, and only the GPIO1 pin has the DIN function.) Maintain registers TX_DIN_EN and TX_DIN_SEL (Addr = 0x69) at the default value of 0.

2. Send the go _ tx command, and the chip starts sending the data on the DIN.

3. Continuously send data to DIN, and the data will be sent out immediately.

4. Send the go_sleep/go_stby/go_tfs command to save power.

6.2.2 Packet Mode

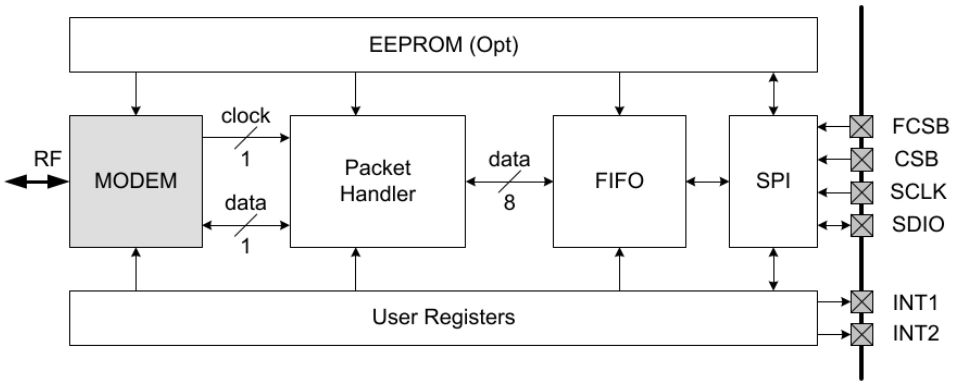


Figure 16. Data Path in Packet Mode

In packet mode, the MCU can pre-fill data into the FIFO when in STBY and TFS states, or write data into the FIFO while the chip is sending data, or a combination of the above two methods. The Tx working sequence of a typical packet pattern is as follows.

1. Configure GPIO via CUS_IO_SEL (Addr = 0x65).

2. Send the go_stby/go_tfs command when there is data that needs to be preloaded into the FIFO.

3. Send go _ tx command.

4. Write data into the FIFO in the corresponding interrupt state.

5. Send a go_sleep/go_stby/go_tfs command to save power.

7 Automatic Operation Mode

CMT2119B configures relevant registers to make the Tx of the chip work in automatic operation mode to save chip power consumption. It can be divided into the following three modes:

1. Automatically exit TX

2. Automatic SLEEP wake up and automatically exit TX

3. Fully automatic transmission

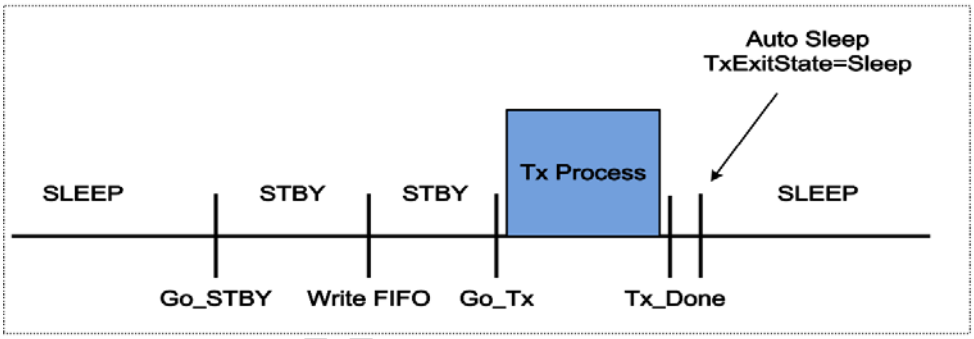


Figure 17. Automatic Exit Tx

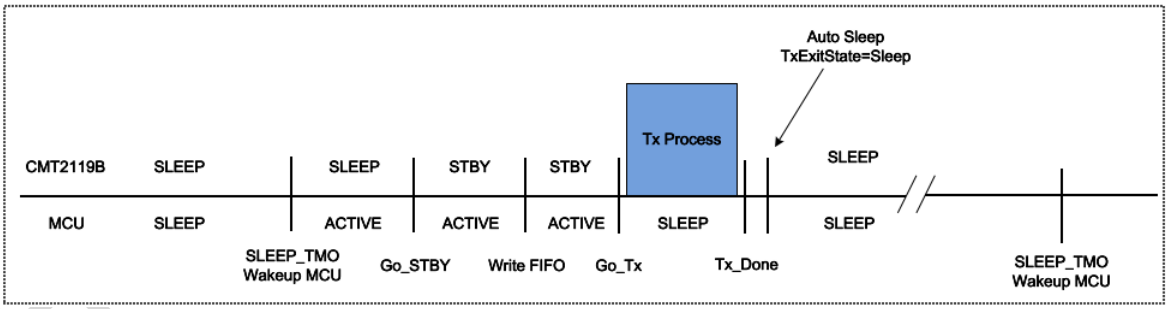


Figure 18. Automatic Sleep Wakeup, Automatic Exit Tx

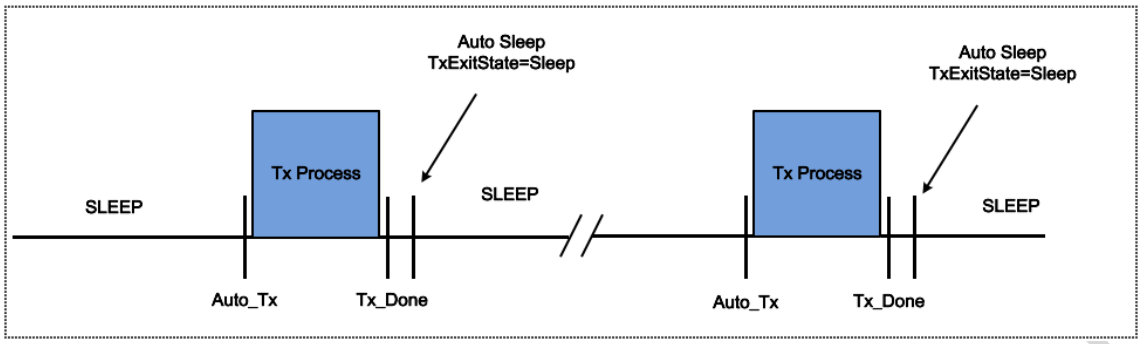


Figure 19. Fully Automatic Transmission

(the contents of fully automatic transmission need to be pre-filled, and this is the content for each transmission)

8 User Register

The following is a list of registers. For the specific usage of the registers, please refer to AN167 CMT2119B Quick Start Guide. Among these register partitions, except for Control Zone 2, which cannot be accessed under SLEEP mode, all others can be accessed under SLEEP mode.

Table 16. Register Partition

Address Range	Name		RFPDK	Remark
0x00 ~ 0x0B	Configuration area (The configuration values in this area can be exported through the Export function of the RFPDK software)	Internal parameter area	CMT Bank	Exported by RFPDK, it is not recommended for customers to modify.
0x0C ~ 0x17		System Operation Area	System Bank	This area is mainly involved in Duty Cycle working configuration.
0x18 ~ 0x1F		Frequency configuration area	Frequency Bank	This area is for configuring the transmission operating frequency.
0x20 ~ 0x37		Data rate area	Data Rate Bank	This area is the associated communication rate

0x38 ~ 0x54		Baseband region	Baseband Bank	This area mainly involves data packet structures (which includes encoding formats, message structures, verification, error correction, synchronization words, etc.)
0x55 ~ 0x5F		Transmission parameter area	TX Bank	This area is mainly involved in the parts of transmit frequency offset and transmit power.
0x60 ~ 0x6A	Control Zone 1 (configured according to MCU requirements, not generated by RFPDK)		-	Working status, frequency hopping configuration, GPIO Configuration, interrupt source switches, etc.;
0x6B ~ 0x71	Control Zone 2 (configured according to MCU requirements, not generated by RFPDK)		-	Interrupt source flag, FIFO Control, RSSI Measurement, etc

8.1 CMT Area

The CMT area mainly stores product-related information and other functional registers, and contains some registers used internally in the chip.

Table 17. CMT Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	RW	CUS_CMT1	Users do not need to understand, directly use RFPDK to generate and import							
0x01	RW	CUS_CMT2								
0x02	RW	CUS_CMT3								
0x03	RW	CUS_CMT4								
0x04	RW	CUS_CMT5								
0x05	RW	CUS_CMT6								
0x06	RW	CUS_CMT7								
0x07	RW	CUS_CMT8								
0x08	RW	CUS_CMT9								
0x09	RW	CUS_CMT10								
0x0A	RW	CUS_CMT11								

0x0B	RW	CUS_RSSI

8.2 System Area

The system area mainly configures parameters related to the timer to implement the operation of the Duty Cycle mode.

Table 18. System Area

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	RW	CUS_SYS1	RESV							
0x0D	RW	CUS_SYS2	LFOSC_RECAL_EN	LFOSC_CAL1_EN	LFOSC_CAL2_EN	0	SLEEP_TIMER_EN	TX_DC_EN	0	DC_PAUSE
0x0E	RW	CUS_SYS3	SLEEP_BYPASS_EN	XTAL_STB_TIME [2:0]			TX_EXIT_STATE [1:0]		0	
0x0F	RW	CUS_SYS4	SLEEP_TIMER_M [7:0]							
0x10	RW	CUS_SYS5		SLEEP_TIMER_M [10:8]			SLEEP_TIMER_R [3:0]			
0x11	RW	CUS_SYS6	RESV							
0x12	RW	CUS_SYS7	RESV							
0x13	RW	CUS_SYS8	RESV							
0x14	RW	CUS_SYS9	RESV							
0x15	RW	CUS_SYS10	RESV							
0x16	RW	CUS_SYS11	RESV							
0x17	RW	CUS_SYS12	RESV		CLKOUT_EN	CLKOUT_DIV [4:0]				

8.3 Frequency Region

The frequency region mainly stores the registers that implement the frequency tuning function.

Table 19. Frequency Region

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x18	RW	CUS_RF1	Users do not need to understand, directly use RFPDK to generate and import							
0x19	RW	CUS_RF2								
0x1A	RW	CUS_RF3								
0x1B	RW	CUS_RF4								
0x1C	RW	CUS_RF5								
0x1D	RW	CUS_RF6								
0x1E	RW	CUS_RF7								
0x1F	RW	CUS_RF8								

8.4 Data Rate Area

The data rate area is stored in data rate-related, FSK-related and OOK-related registers.

Table 20. Data Rate Regions

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

0x20	RW	CUS_RF9	Users do not need to understand; directly generate and import by using RFPDK.
0x21	RW	CUS_RF10	
0x22	RW	CUS_RF11	
0x23	RW	CUS_RF12	
0x24	RW	CUS_FSK1	
0x25	RW	CUS_FSK2	
0x26	RW	CUS_FSK3	
0x27	RW	CUS_FSK4	
0x28	RW	CUS_FSK5	
0x29	RW	CUS_FSK6	
0x2A	RW	CUS_FSK7	
0x2B	RW	CUS_CDR1	
0x2C	RW	CUS_CDR2	
0x2D	RW	CUS_CDR3	
0x2E	RW	CUS_CDR4	
0x2F	RW	CUS_AGC1	
0x30	RW	CUS_AGC2	
0x31	RW	CUS_AGC3	
0x32	RW	CUS_AGC4	
0x33	RW	CUS_OOK1	
0x34	RW	CUS_OOK2	
0x35	RW	CUS_OOK3	
0x36	RW	CUS_OOK4	
0x37	RW	CUS_OOK5	

8.5 Data Rate Area

The baseband area stores registers related to packet format settings.

Table 21. Baseband Regions

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x38	RW	CUS_PKT1	RESV					PREAM_LENG_UNIT	DATA_MODE [1:0]	
0x39	RW	CUS_PKT2	TX_PREAM_SIZE [7:0]							
0x3A	RW	CUS_PKT3	TX_PREAM_SIZE [15:8]							
0x3B	RW	CUS_PKT4	PREAM_VALUE [7:0]							
0x3C	RW	CUS_PKT5	RESV	SYNC_TOL [2:0]			SYNC_SIZE [2:0]			SYNC_MAN_EN
0x3D	RW	CUS_PKT6	SYNC_VALUE [7:0]							
0x3E	RW	CUS_PKT7	SYNC_VALUE [15:8]							
0x3F	RW	CUS_PKT8	SYNC_VALUE [23:16]							
0x40	RW	CUS_PKT9	SYNC_VALUE [31:24]							
0x41	RW	CUS_PKT10	SYNC_VALUE [39:32]							
0x42	RW	CUS_PKT11	SYNC_VALUE [47:40]							
0x43	RW	CUS_PKT12	SYNC_VALUE [55:48]							
0x44	RW	CUS_PKT13	SYNC_VALUE [63:56]							
0x45	RW	CUS_PKT14	RESV	PAYLOAD_LENG [10:8]			AUTO_ACK_EN	NODE_LENG_POS_SEL	PAYLOAD_BIT_ORDER	PKT_TYPE
0x46	RW	CUS_PKT15	PAYLOAD_LENG [7:0]							
0x47	RW	CUS_PKT16	RESV	RESV	NODE_FREE_EN	NODE_ERR_MASK	NODE_SIZE [1:0]		NODE_DET_MODE [1:0]	
0x48	RW	CUS_PKT17	NODE_VALUE [7:0]							
0x49	RW	CUS_PKT18	NODE_VALUE [15:8]							
0x4A	RW	CUS_PKT19	NODE_VALUE [23:16]							
0x4B	RW	CUS_PKT20	NODE_VALUE [31:24]							
0x4C	RW	CUS_PKT21	FEC_TYPE	FEC_EN	CRC_BYTE_SWAP	CRC_BIT_INV	CRC_RANGE	CRC_TYPE [1:0]		CRC_EN
0x4D	RW	CUS_PKT22	CRC_SEED [7:0]							
0x4E	RW	CUS_PKT23	CRC_SEED [15:8]							
0x4F	RW	CUS_PKT24	CRC_BIT_ORDER	WHITEN_SEED [8]	WHITEN_SEED_TYPE	WHITEN_TYPE [1:0]		WHITEN_EN	MANCH_TYPE	MANCH_EN
0x50	RW	CUS_PKT25	WHITEN_SEED [7:0]							
0x51	RW	CUS_PKT26	RESV						TX_PREFIX_TYPE [1:0]	
0x52	RW	CUS_PKT27	TX_PKT_NUM [7:0]							
0x53	RW	CUS_PKT28	TX_PKT_GAP [7:0]							
0x54	RW	CUS_PKT29	FIFO_AUTO_RES_EN	FIFO_TH [6:0]						

8.6 Transmission Area

The transmit area stores registers related to transmit power, frequency offset and related registers.

Table 22. Transmission Area

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x55	RW	CUS_TX1	Users do not need to understand, directly use RFPDK to generate and import							
0x56	RW	CUS_TX2								
0x57	RW	CUS_TX3								
0x58	RW	CUS_TX4								
0x59	RW	CUS_TX5								
0x5A	RW	CUS_TX6								

0x5B	RW	CUS_TX7
0x5C	RW	CUS_TX8
0x5D	RW	CUS_TX9
0x5E	RW	CUS_TX10
0x5F	RW	CUS_LBD

8.7 Control Zone 1

Control Zone 1 stores registers for enabling various functional modules, function selection.

Table 23. Control Zone 1

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	RW	CUS_MODE_CTL	CHIP_MODE_SWT[7:0]							
0x61	RW	CUS_MODE_STA	RESV	RESV	RSTN_IN_EN	CFG_RETAIN	CHIP_MODE_STA[3:0]			
0x62	RW	CUS_EN_CTL	RESV	RESV	UNLOCK_STOP_EN	LBD_STOP_EN	RESV	RESV	RESV	RESV
0x63	RW	CUS_FREQ_CHNL	FH_CHANNEL[7:0]							
0x64	RW	CUS_FREQ_OFS	FH_OFFSET[7:0]							
0x65	RW	CUS_IO_SEL	GPIO4_SEL[1:0]		GPIO3_SEL[1:0]		GPIO2_SEL[1:0]		GPIO1_SEL[1:0]	
0x66	RW	CUS_INT1_CTL	RF_SWT1_EN	RF_SWT2_EN	INT_POLAR	INT1_SEL[4:0]				
0x67	RW	CUS_INT2_CTL	RESV	LFOSC_OUT_EN	TX_DIN_INV	INT2_SEL[4:0]				
0x68	RW	CUS_INT_EN	SL_TMO_EN	0	TX_DONE_EN	0	0	0	0	0
0x69	RW	CUS_FIFO_CTL	TX_DIN_EN	TX_DIN_SEL[1:0]		FIFO_AUTO_CLR_DIS	FIFO_TX_RD_EN	1	FIFO_MERGE_EN	SPI_FIFO_RD_WR_SEL
0x6A	W	CUS_INT_CLR1	RESV	RESV	SL_TMO_FLG	RESV	TX_DONE_FLG	TX_DONE_CLR	SL_TMO_CLR	RESV

8.8 Control Zone 2

Control area 1 stores registers related to flag bits and registers related to RSSI and LBD. Note that the registers in this area cannot be accessed in the SLEEP state.

Table 24. Control Zone 2

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x6B	W	CUS_INT_CLR2	RESV	RESV	LBD_CLR	RESV				
0x6C	W	CUS_FIFO_CLR						FIFO_RESTORE	0	FIFO_CLR_TX
0x6D	R	CUS_INT_FLAG	LBD_FLG	RESV						
0x6E	R	CUS_FIFO_FLAG	RESV					TX_FIFO_FULL_FLG	TX_FIFO_NMTY_FLG	TX_FIFO_TH_FLG
0x6F	R	CUS_RSSI_CODE	RESV							
0x70	R	CUS_RSSI_DBM	RESV							
0x71	R	CUS_LBD_RESULT	LBD_RESULT[7:0]							

9 Ordering information

Table 25. CMT2219B Ordering Information

Part number	Description	Package	Packaging	Operating	Minimum
CMT2119B-EQR[1]	CMT2119B, +20 dBm high power,Sub-1GHz Radio frequency transmitter	QFN16 (3x3)	Tape and reel packaging	1.8 to 3.6 V, -40 to 85℃	3000

Remark:

[1]. "E" stands for Extended Industrial Product Grade, and the temperature range it supports is from -40 to +85 °C. "Q" represents the package type of QFN16."R" represents the tape and reel packaging type, with a minimum order quantity (MOQ) of 3,000 pieces.

For more information about products, please visit www.hoperf.cn。

For inquiries on any product, please contact us. sales@hoperf.com

10 Package Information

The packaging information of CMT2119B is QFN16 (3x3) package and is shown in the following figure.

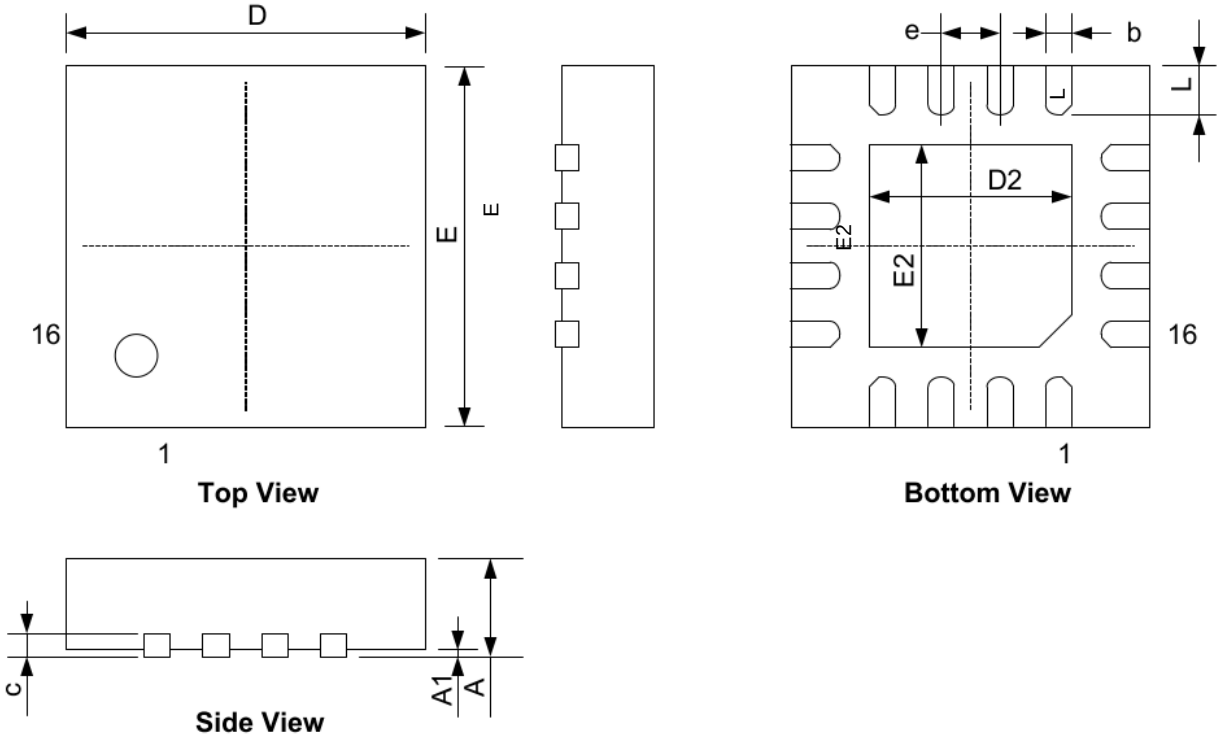


Figure 20. 16-Pin QFN 3x3 Package

Table 26. 16-Pin QFN 3x3 Package Dimensions

Symbol	Dimensions(millimeter)	
	Minimum	Maximum
A	0.7	0.8
A1	-	0.05
b	0.18	0.30
c	0.18	0.25
D	2.90	3.10
D2	1.55	1.75
e	0.50 BSC	
E	2.90	3.10
E2	1.55	1.75
L	0.35	0.45

11 Top Silk Printing

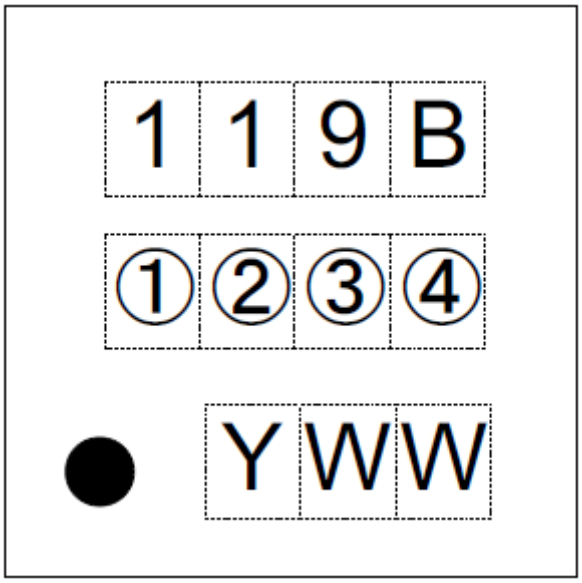


Figure 21. CMT2119B Top Silk Printing

Table 27. CMT2219B Top Silk Printing Description

Screen printing method	Laser
Pin 1 Mark	Circle diameter = 0.3 mm
Font Size	0.5 mm, Right-aligned
First line of silk screen	119B, represents model CMT2119B
Second silk screen	①②③④ Internal tracking code
Third line silk screen printing	Date code, assigned by the packaging factory, Y represents the last digit of the year, WW represents the workweek.

12 Document Change Record

Table 29. Document Change Record

Version No.	Chapter	Change Description	Date
Initial version	All	All chapters	2017-09-07
0.5	2，5.4	Modify the descriptions of GPIOX pins in Table 11 and Table 14, and delete the relevant content about GPIO2 and GPIO3 being multiplexed as DIN functions. When CMT2119B is used in direct mode, external modulation data can only be input through the GPIO1 pin.	2018-11-30
0.6	All	Delete reference document chapter	2024-04-03
0.7	4.2.5	Add a new section of 4.2.5 Power-On Reset (POR)	2025-03-12
	3	In the BOM table, modify the content in the L3 row (capacitor 15pF)	2025-09-04
0.8	5.3.2	Modify TFS to 0100	2025-10-29
	1.6	Modify the phase noise in the table at 868MHz with a 100 kHz frequency offset to -95	

13 Contact Information

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