

Dual P-Channel MOSFET

RC4805

■ Features

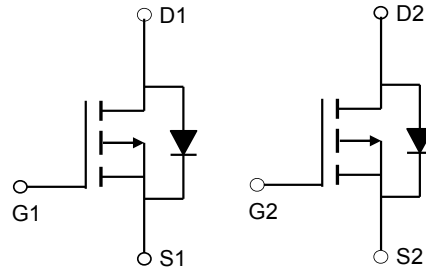
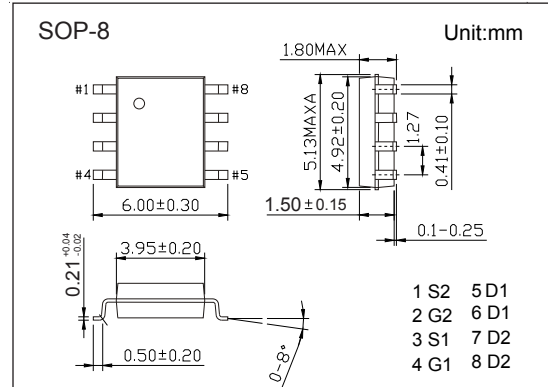
- $V_{DS} (V) = -30V$
- $I_D = -10A$
- $R_{DS(ON)} < 23m\Omega$ ($V_{GS} = -10V$)
- $R_{DS(ON)} < 34m\Omega$ ($V_{GS} = -4.5V$)

■ General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

■ Applications

- Battery protection
- Load switch
- Power management



■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V_{DS}	-30	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	$T_A=25^\circ C$ @ Steady State	-10
		$T_A=70^\circ C$ @ Steady State	-8
Pulsed Drain Current ^A	I_{DM}	-50	A
Total Power Dissipation @ $T_A=25^\circ C$	P_D	3.0	W
Thermal Resistance Junction-to-Ambient @ Steady State ^B	$R_{\theta JA}$	42	$^\circ C/W$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ C$

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■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V, T _C =25°C			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-1.0	-1.5	-2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -10V, I _D =-10A		19.5	23	mΩ
		V _{GS} = -4.5V, I _D =-5.0A		27.5	34	
Diode Forward Voltage	V _{SD}	I _S =-10A, V _{GS} =0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I _S				-10	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V, f=1MHZ		1500		pF
Output Capacitance	C _{oss}			178		
Reverse Transfer Capacitance	C _{rss}			146		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V, I _D =-6.0A		28.7		nC
Gate Source Charge	Q _{gs}			5.5		
Gate Drain Charge	Q _{gd}			5.4		
Reverse Recovery Charge	Q _{rr}	I _F = -9A, di/dt=500A/us		6.0		
Reverse Recovery Time	t _{rr}			14		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DS} =-15V, I _D =-6.0A, R _{GEN} =2.5Ω		10		ns
Turn-on Rise Time	t _r			44		
Turn-off Delay Time	t _{D(off)}			54		
Turn-off Fall Time	t _f			59		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R_{θJL} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

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Typical Performance Characteristics

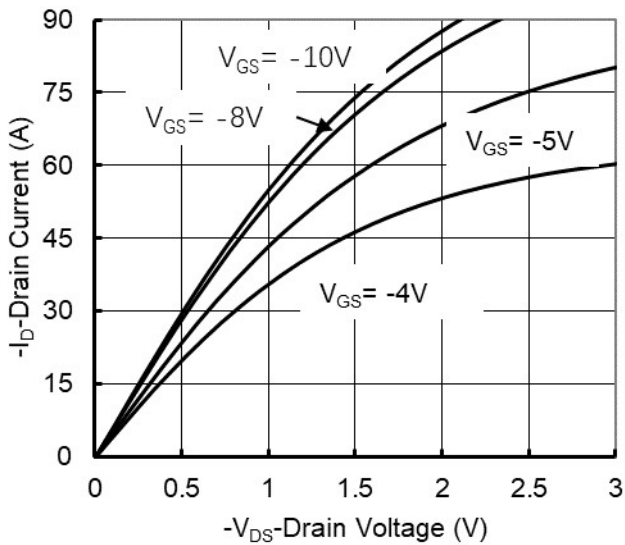


Figure 1. Output Characteristics

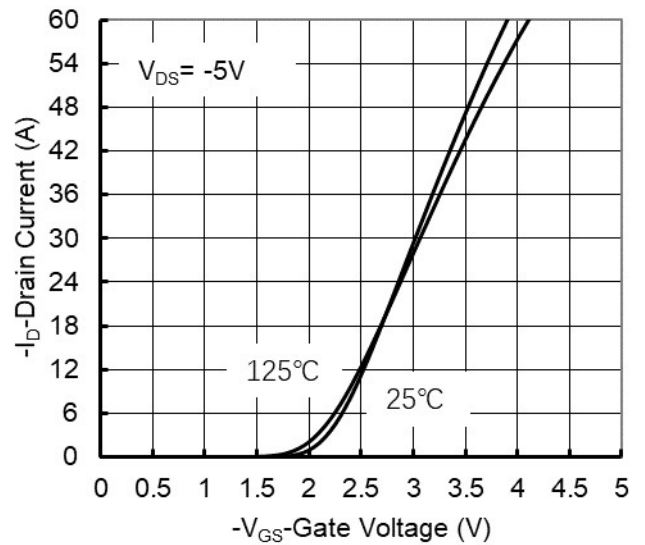


Figure 2. Transfer Characteristics

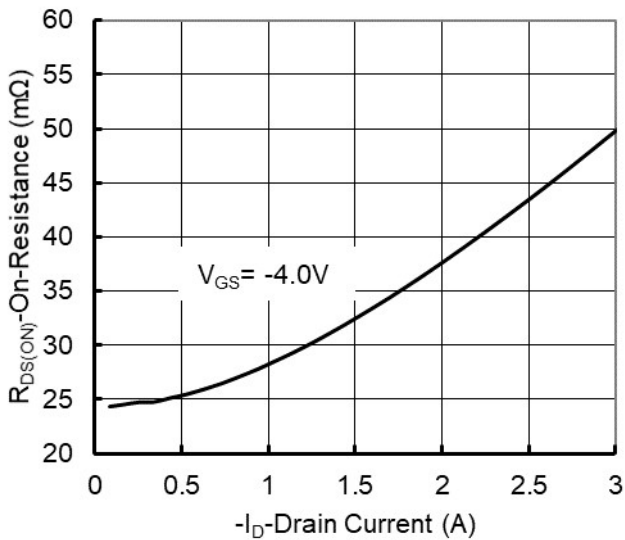


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

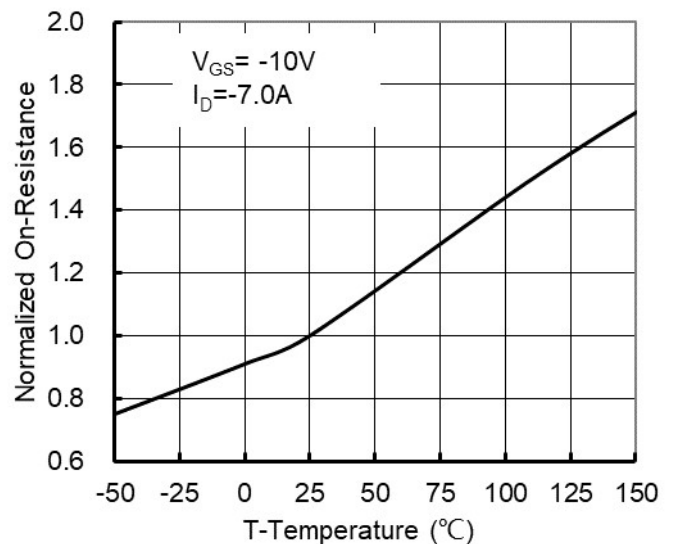


Figure 4. On-Resistance vs. Junction Temperature

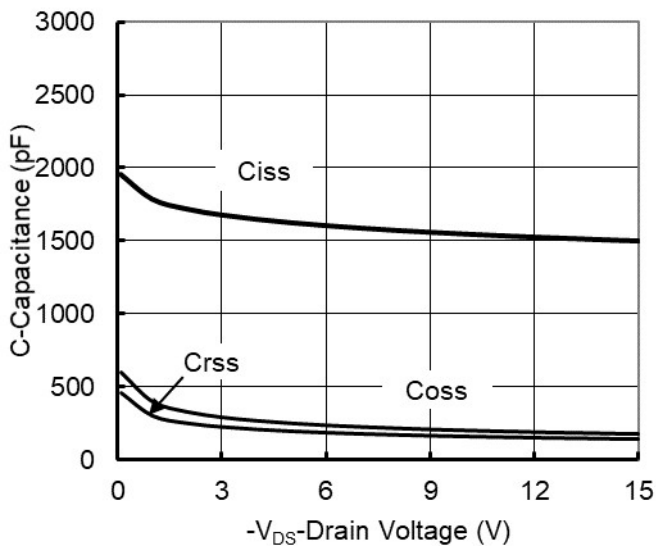


Figure 5. Capacitance Characteristics

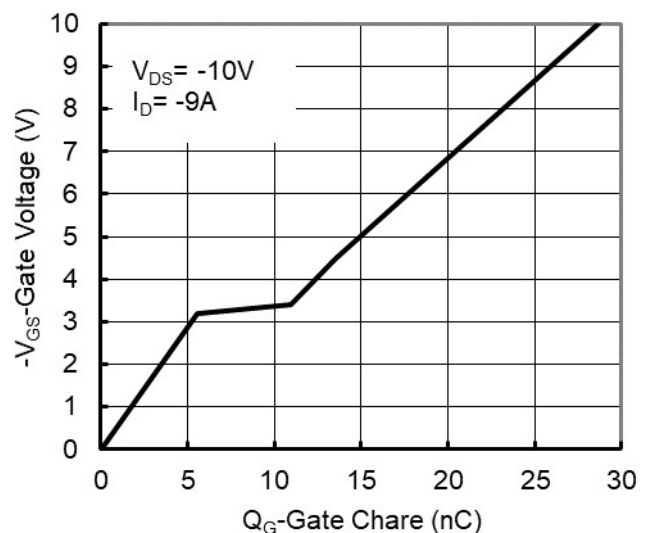


Figure 6. Gate Charge

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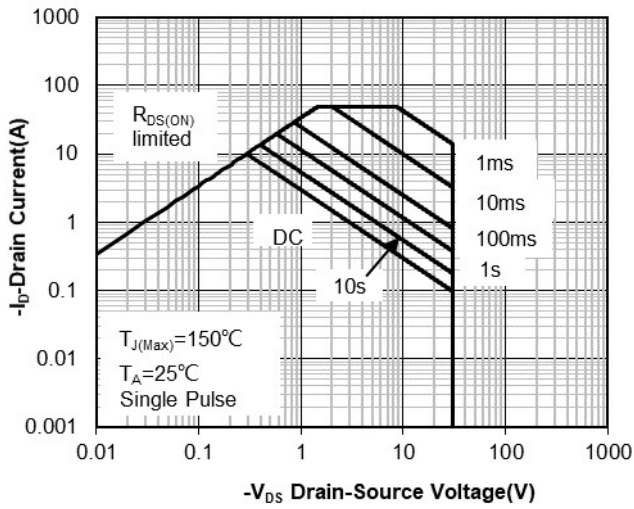


Figure 7. Safe Operation Area

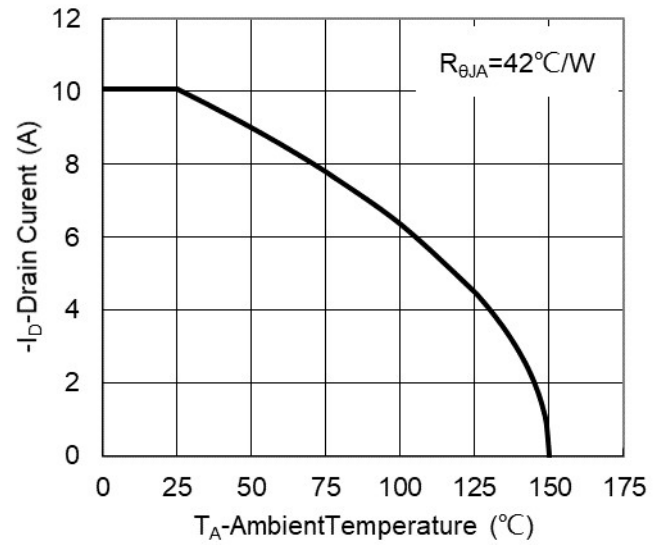


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

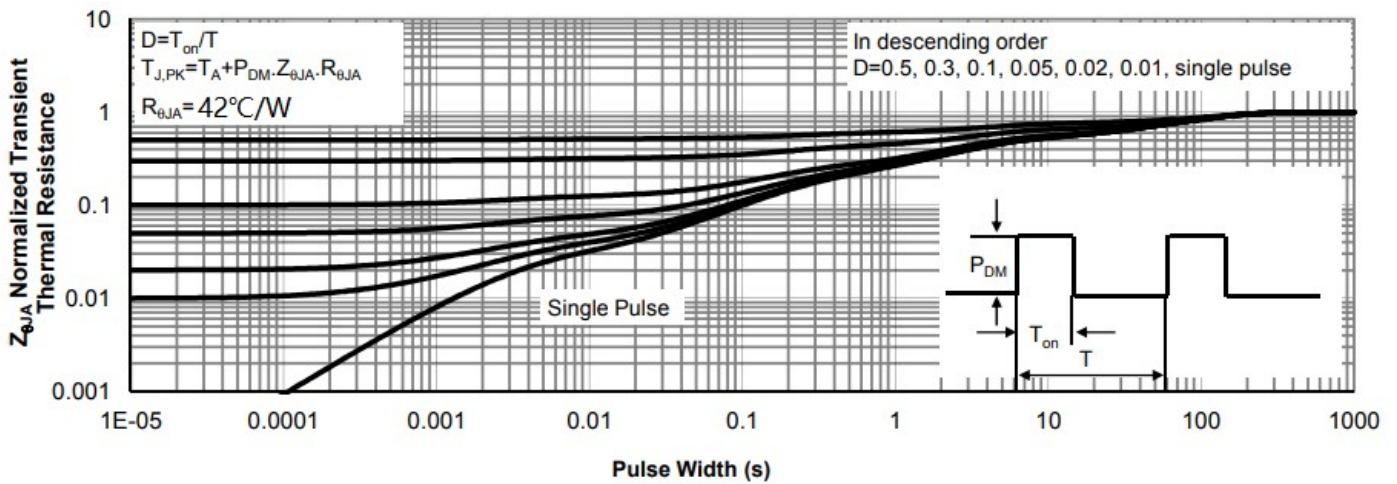
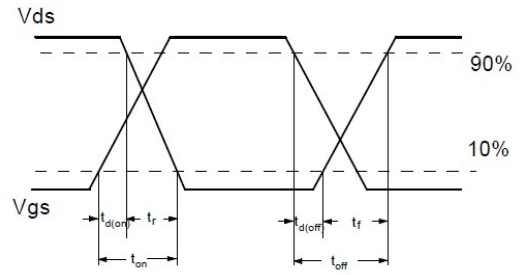
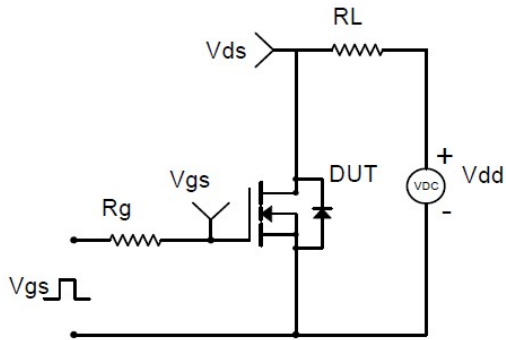
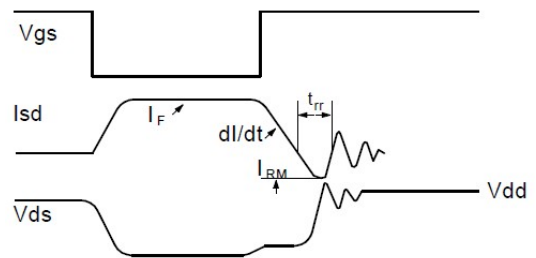
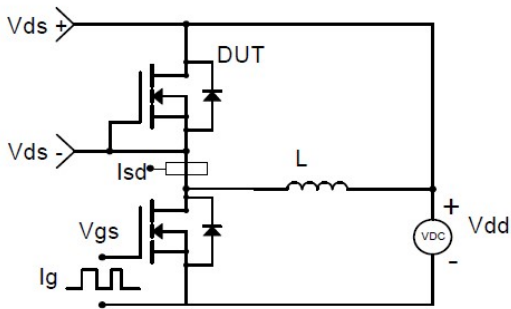


Figure 9. Normalized Maximum Transient Thermal Impedance

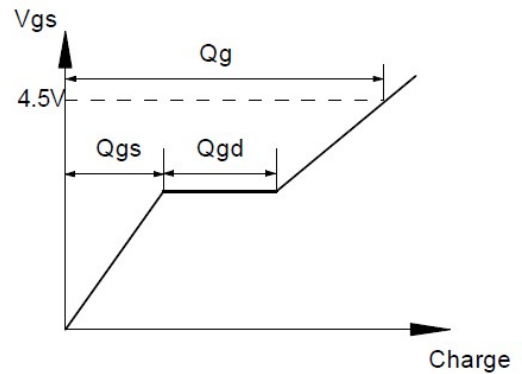
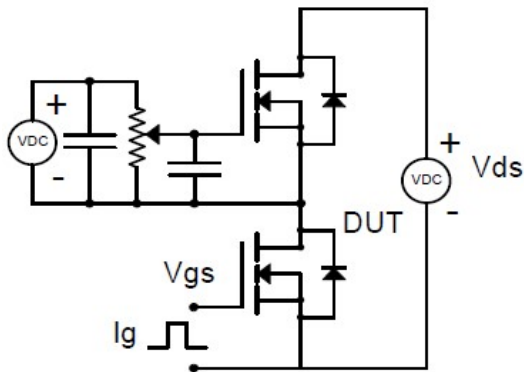
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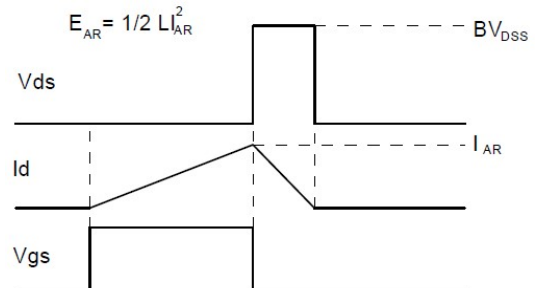
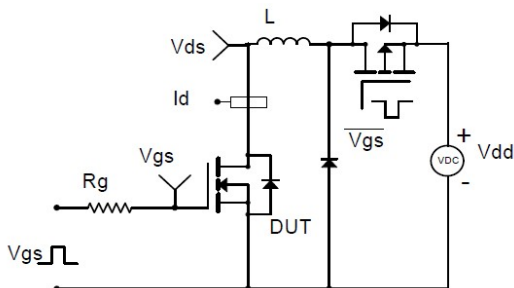
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms