

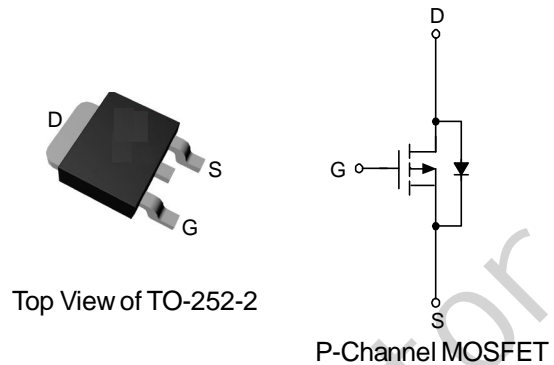
Features

- 40V/-60A,
 $R_{DS(ON)} = 11m\Omega$ (max.) @ $V_{GS} = -10V$
 $R_{DS(ON)} = 14m\Omega$ (max.) @ $V_{GS} = -4.5V$
- 100% UIS + R_g Tested
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Power Management in LCD TV Inverter.

Pin Description



Absolute Maximum Ratings ($T_A = 25^\circ C$ Unless Otherwise Noted)

Symbol	Parameter	Rating	Unit		
V_{DSS}	Drain-Source Voltage	-40	V		
V_{GSS}	Gate-Source Voltage	± 20			
I_D^a	Continuous Drain Current ($V_{GS} = -10V$)	$T_A = 25^\circ C$	A		
		$T_A = 70^\circ C$		-12	
I_{DP}^a	300 μs Pulsed Drain Current Tested	$T_A = 25^\circ C$		-62	
I_D^c	Continuous Drain Current ($V_{GS} = -10V$)	$T_C = 25^\circ C$		-44	
		$T_C = 100^\circ C$		-28	
I_{DP}^c	300 μs Pulsed Drain Current Tested	$T_C = 25^\circ C$		-176	
I_S^c	Diode Continuous Forward Current	-40			
I_{AS}^b	Avalanche Current, Single pulse	$L = 0.1mH$		-30	
		$L = 1mH$		-13	
E_{AS}^b	Avalanche Energy, Single pulse	$L = 0.1mH$		45	
		$L = 1mH$	84		
T_J	Maximum Junction Temperature	150	$^\circ C$		
T_{STG}	Storage Temperature Range	-55 to 150			
P_D^a	Maximum Power Dissipation	$T_A = 25^\circ C$	W		
		$T_A = 70^\circ C$		4.0	
P_D^c	Maximum Power Dissipation	$T_C = 25^\circ C$		50	
		$T_C = 100^\circ C$		20	
$R_{\theta JA}^a$	Thermal Resistance-Junction to Ambient	$t \leq 10s$		$^\circ C/W$	
		Steady State			50
$R_{\theta JC}^c$	Thermal Resistance-Junction to Case	Steady State			2.5

Note a : Surface Mounted on 1in² pad area, $t \leq 10sec$. $R_{\theta JA}$ steady state $t = 100s$.

Note b : UIS tested and pulse width limited by maximum junction temperature 150 $^\circ C$ (initial temperature $T_J = 25^\circ C$).

Note c : The power dissipation P_D is based on $T_{J(MAX)} = 150^\circ C$, and it is useful for reducing junction-to-case thermal resistance ($R_{\theta JC}$) when additional heat sink is used.

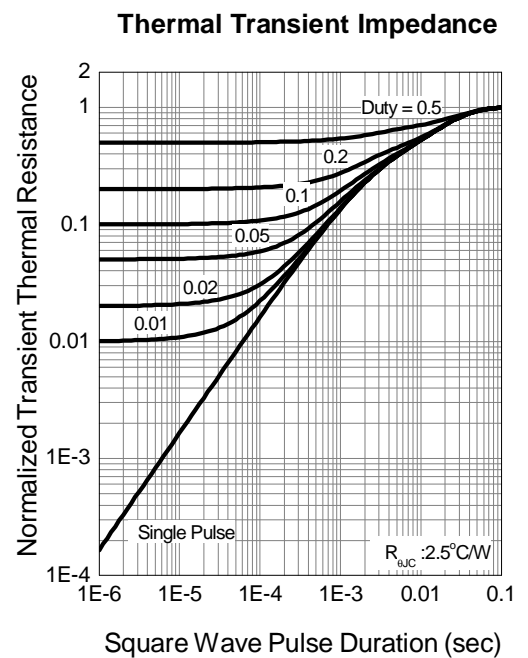
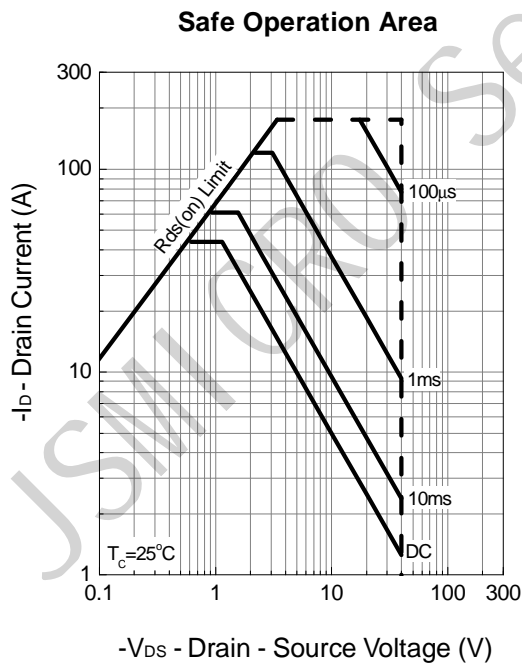
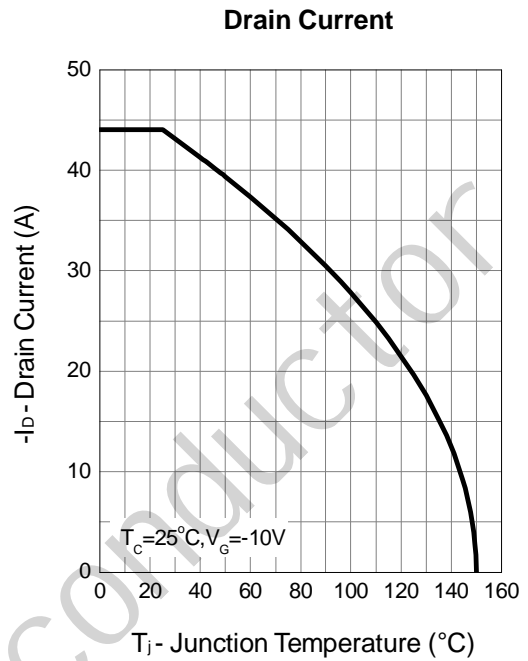
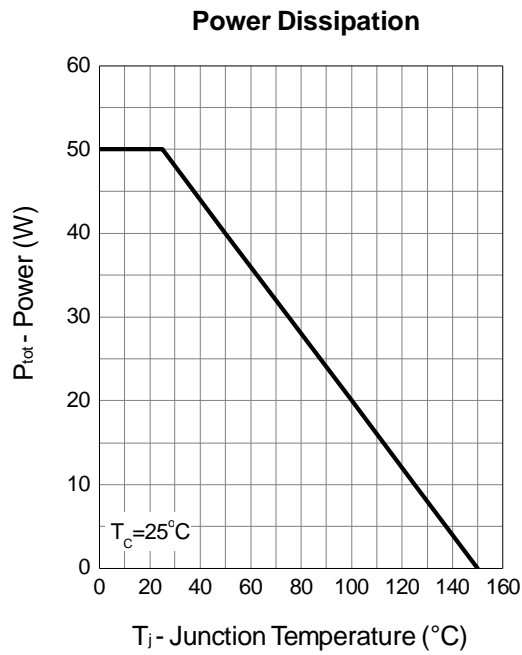
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=-250\mu A$	-40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-32V, V_{GS}=0V$	-	-	-1	μA
		$T_J=85^\circ\text{C}$	-	-	-30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=-250\mu A$	-1.4	-1.9	-2.4	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 25V, V_{DS}=0V$	-	-	± 100	nA
$R_{DS(ON)}^d$	Drain-Source On-state Resistance	$V_{GS}=-10V, I_{DS}=-15A$	-	11	15	$m\Omega$
		$V_{GS}=-4.5V, I_{DS}=-10A$	-	14	22	
Diode Characteristics						
V_{SD}^d	Diode Forward Voltage	$I_{SD}=-1A, V_{GS}=0V$	-	-0.75	-1	V
t_{rr}	Reverse Recovery Time	$I_{SD}=-15A,$	-	24	-	ns
Q_{rr}	Reverse Recovery Charge	$dI_{SD}/dt=100A/\mu s$	-	18	-	nC
Dynamic Characteristics^e						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$	-	2.3	5	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=-20V,$ Frequency=1.0MHz	-	1500	1950	pF
C_{oss}	Output Capacitance		-	235	-	
C_{rss}	Reverse Transfer Capacitance		-	180	-	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=-20V, R_L=20\Omega,$ $I_{DS}=-1A, V_{GEN}=-10V,$ $R_G=6\Omega$	-	14	25	ns
t_r	Turn-on Rise Time		-	12	22	
$t_{d(OFF)}$	Turn-off Delay Time		-	41	74	
t_f	Turn-off Fall Time		-	22	40	
Gate Charge Characteristics^e						
Q_g	Total Gate Charge	$V_{DS}=-20V, V_{GS}=-10V,$ $I_{DS}=-15A$	-	32	45	nC
Q_{gs}	Gate-Source Charge		-	5.2	-	
Q_{gd}	Gate-Drain Charge		-	8	-	

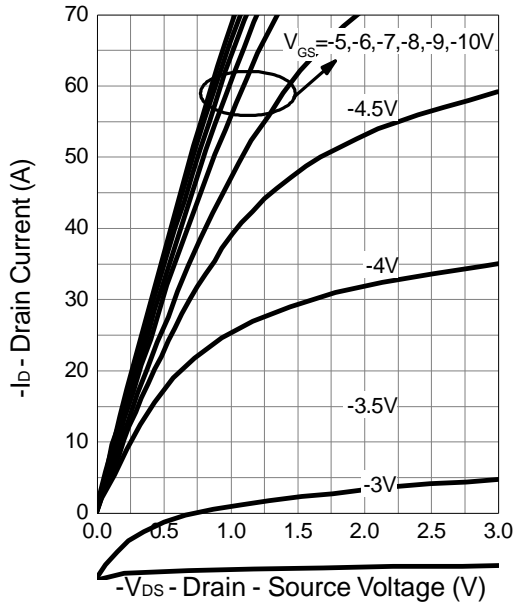
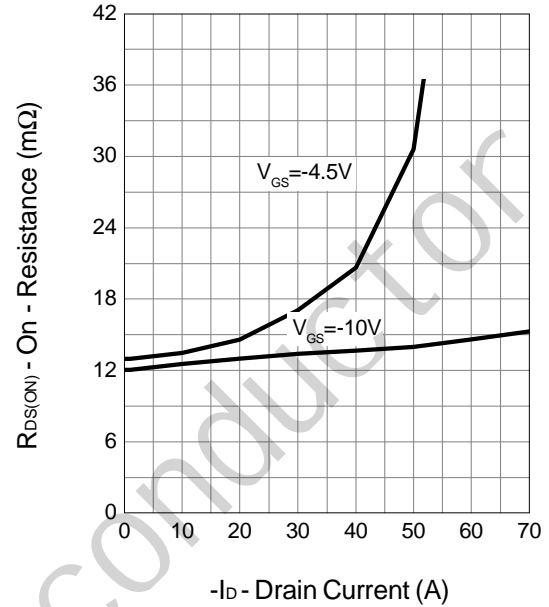
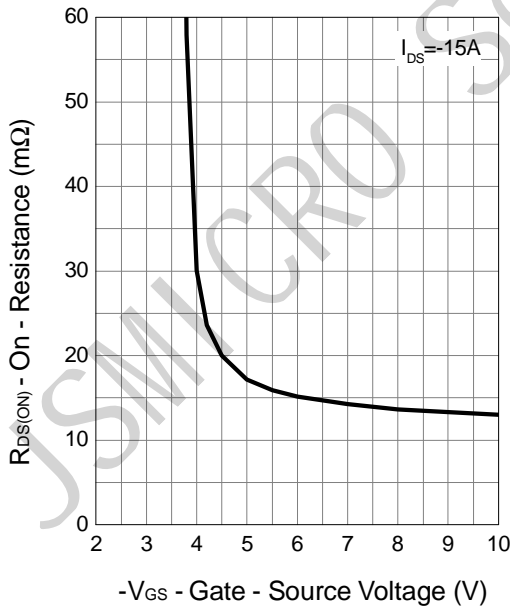
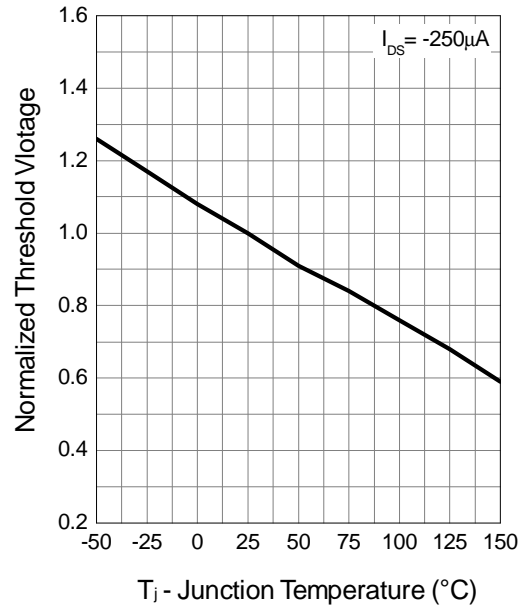
Note d : Pulse test ; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Note e : Guaranteed by design, not subject to production testing.

Typical Characteristics

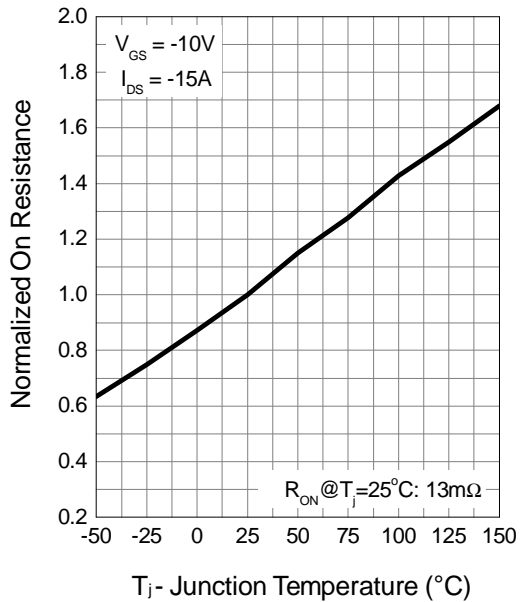


Typical Characteristics (Cont.)

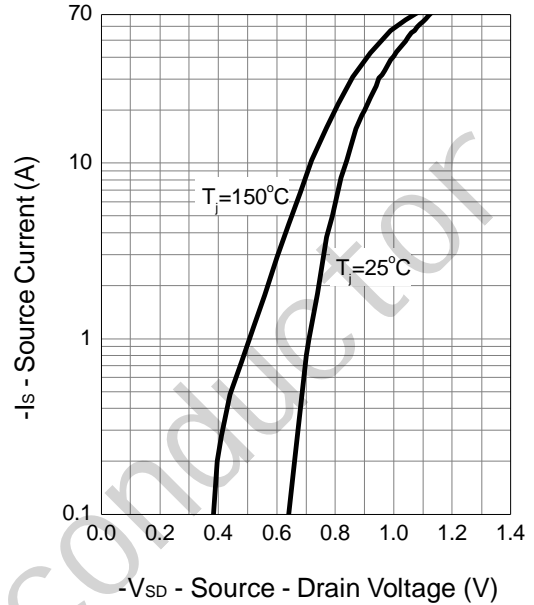
Output Characteristics

Drain-Source On Resistance

Gate-Source On Resistance

Gate Threshold Voltage


Typical Characteristics (Cont.)

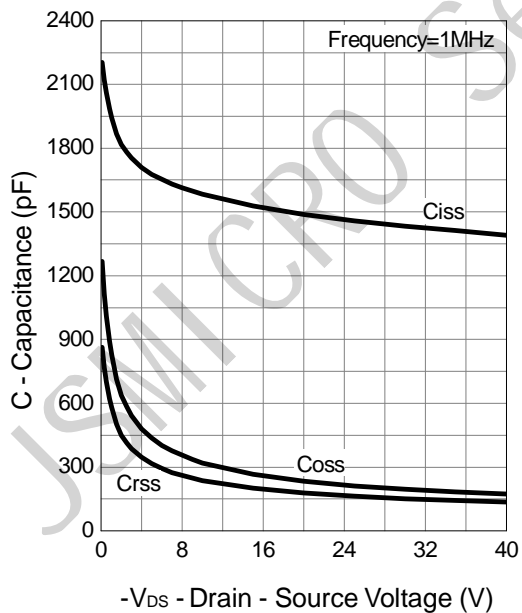
Drain-Source On Resistance



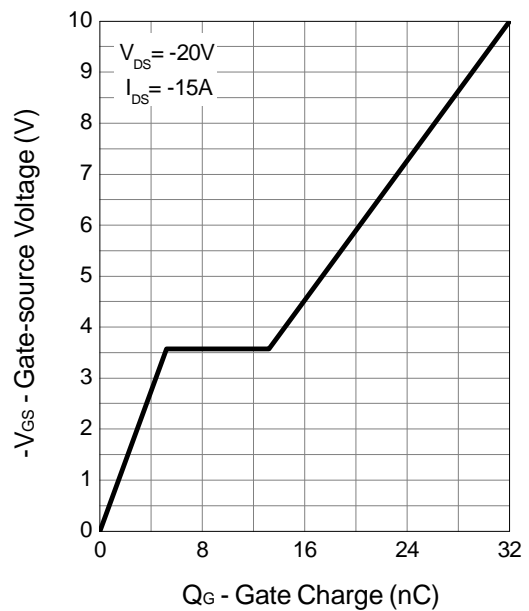
Source-Drain Diode Forward



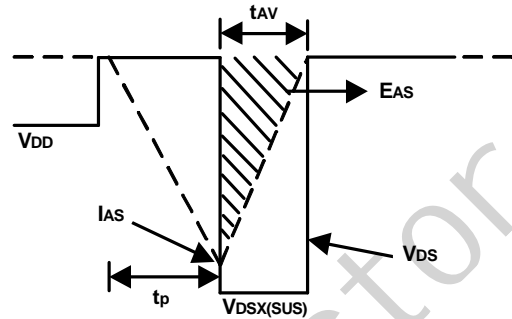
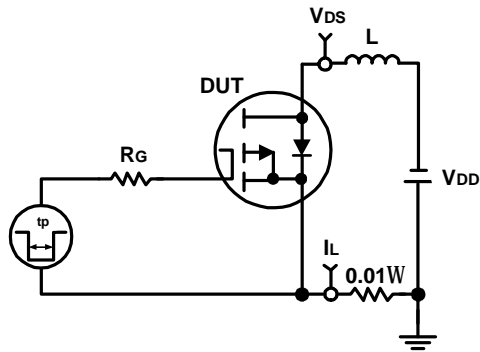
Capacitance



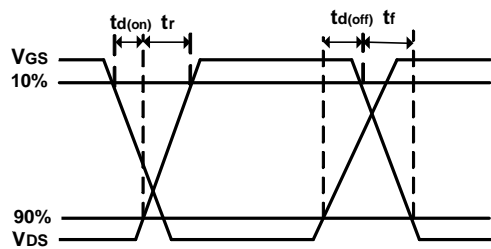
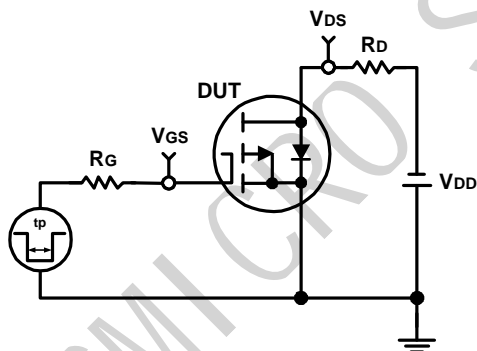
Gate Charge



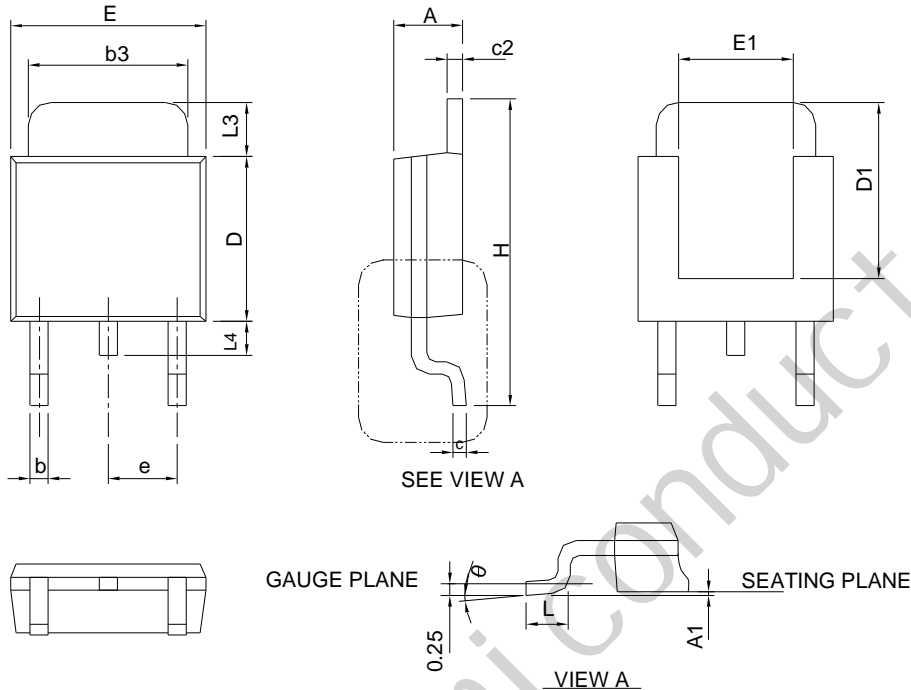
Avalanche Test Circuit and Waveforms



Switching Time Test Circuit and Waveforms

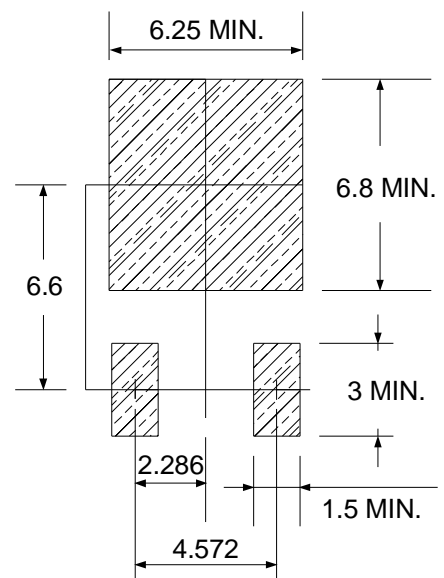


Package Information



SYMBOL	TO-252-2			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	-	0.13	-	0.005
b	0.50	0.89	0.020	0.035
b3	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.33	6.22	0.210	0.245
D1	4.57	6.00	0.180	0.236
E	6.35	6.73	0.250	0.265
E1	3.81	6.00	0.150	0.236
e	2.29 BSC		0.090 BSC	
H	9.40	10.41	0.370	0.410
L	0.90	1.78	0.035	0.070
L3	0.89	2.03	0.035	0.080
L4	-	1.02	-	0.040
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



UNIT: mm

Note : Follow JEDEC TO-252 .