AOD603A

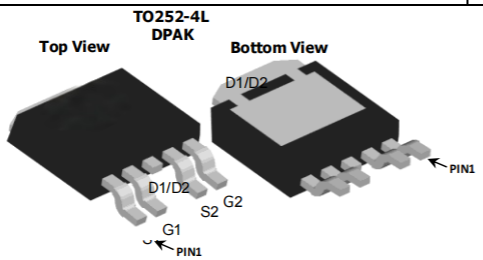
60V Complementary MOSFET

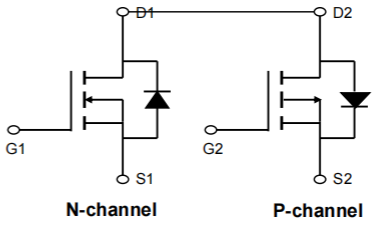
General Description

The AOD603A uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

Product Summary

N-Channel	P-Channel
V_{DS}= 60V	-60V
I_D= 13A (V_{GS}=10V, silicon limit)	-13A (V_{GS}=-10V, silicon limit)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 60mΩ (V_{GS}=10V)	< 115mΩ (V_{GS}=-10V)
< 85mΩ (V_{GS}=4.5V)	< 150mΩ (V_{GS}=-4.5V)
100% UIS Tested	100% UIS Tested
100% R_g Tested	100% R_g Tested





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max N-channel	Max P-channel	Units
Drain-Source Voltage		V_{DS}	60	-60	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C=25°C (silicon limit)	I_D	13.6	-13.4	A
	T_C=25°C [G]		12	-12	
	T_C=100°C		9.5	-9.5	
Pulsed Drain Current [C]		I_{DM}	30	-30	
Continuous Drain Current	T_A=25°C	I_{DSM}	3.5	-3	A
	T_A=70°C		3	-2.5	
Avalanche Current [C]		I_{AS}, I_{AR}	19	25	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	18	31	mJ
Power Dissipation [B]	T_C=25°C	P_D	27	42.5	W
	T_C=100°C		13.5	21.5	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2	2	W
	T_A=70°C		1.3	1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	-55 to 175	°C

Thermal Characteristics

Parameter N-channel		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	19	23	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		50	60	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	4	5.5	°C/W
Parameter P-channel		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	19	23	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		50	60	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.5	3.5	°C/W

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1	2.4	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=12A		47	60	mΩ
		T_J=125°C		90	110	
		V_{GS}=4.5V, I_D=8A		67	85	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=12A		22		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.74	1	V
I_S	Maximum Body-Diode Continuous Current [G]				12	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz		450		pF
C_{oss}	Output Capacitance			61		pF
C_{rss}	Reverse Transfer Capacitance			27		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.6	1.35	2	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=12A		7.5	12	nC
Q_g(4.5V)	Total Gate Charge			3.8	7	nC
Q_{gs}	Gate Source Charge			1.2		nC
Q_{gd}	Gate Drain Charge			1.9		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=30V, R_L=2.5Ω, R_{GEN}=3Ω		4.2		ns
t_r	Turn-On Rise Time			3.4		ns
$t_{D(off)}$	Turn-Off DelayTime			16		ns
t_f	Turn-Off Fall Time			2		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=12A, dI/dt=100A/µs		27		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=12A, dI/dt=100A/µs		30		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

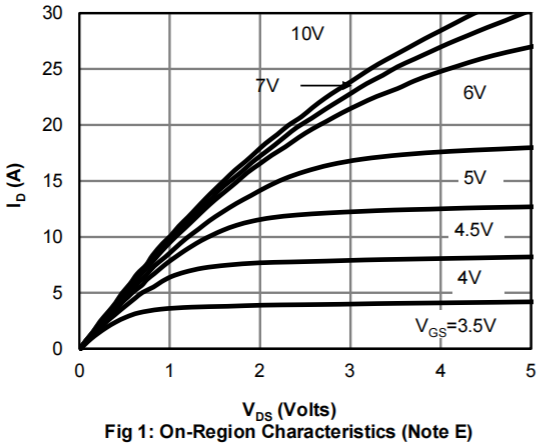


Fig 1: On-Region Characteristics (Note E)

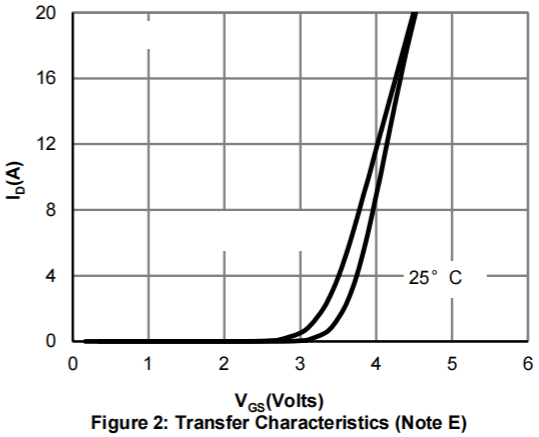


Figure 2: Transfer Characteristics (Note E)

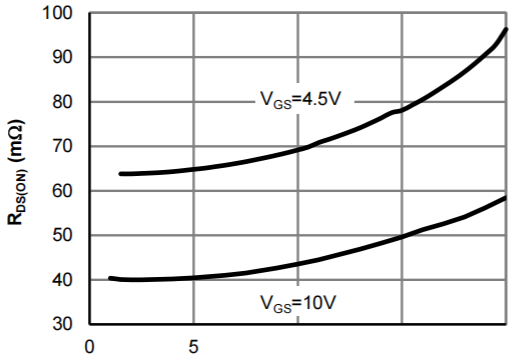


Figure 3: On

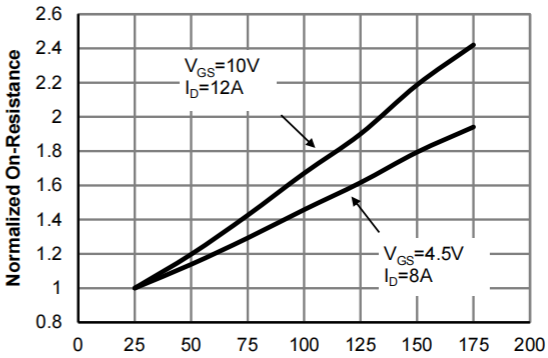


Figure 4: On-Resistance vs. Junction Temperature (Note E)

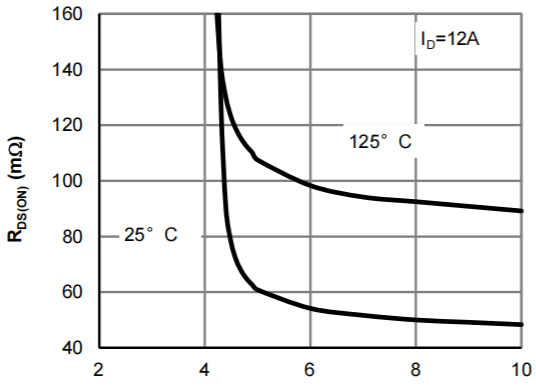


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

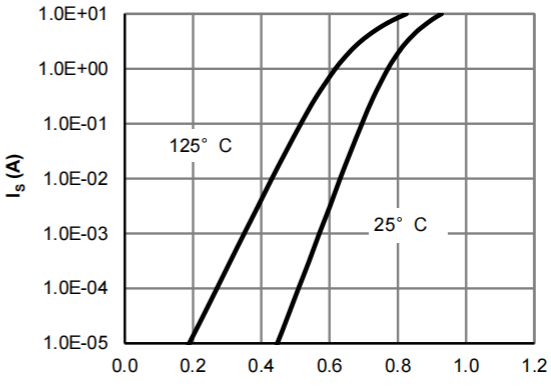


Figure 6: Body-Diode Characteristics (Note E)

N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

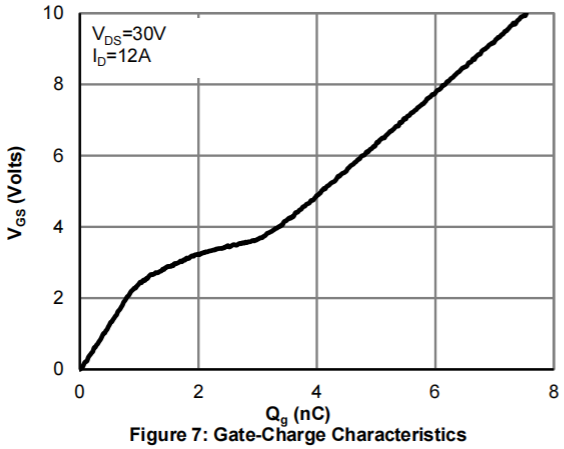


Figure 7: Gate-Charge Characteristics

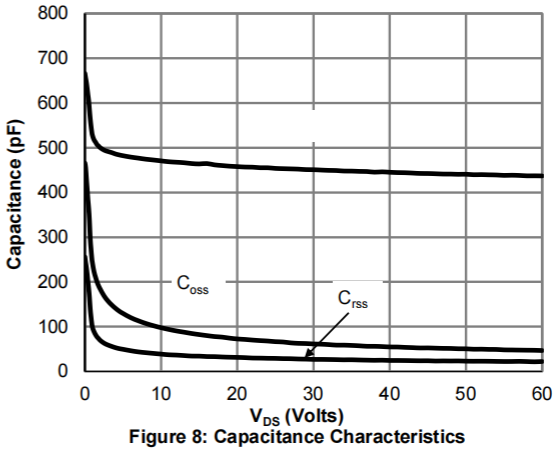


Figure 8: Capacitance Characteristics

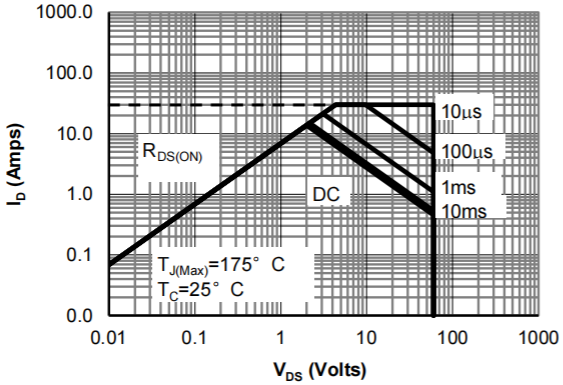


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

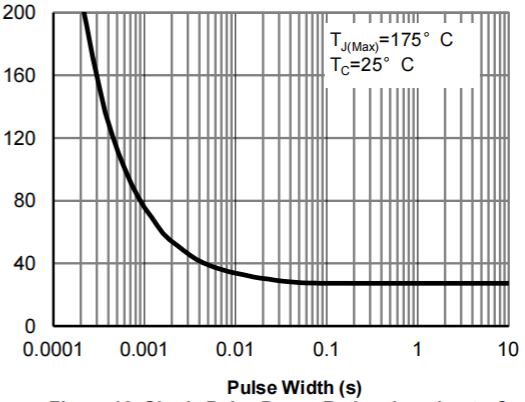


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

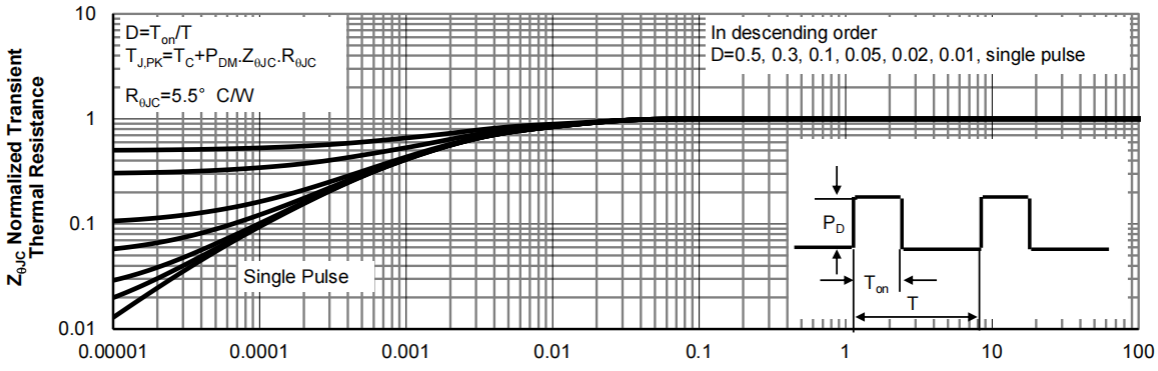


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

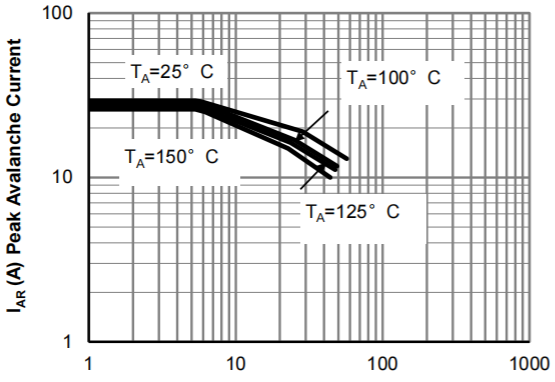


Figure 12: Single Pulse Avalanche capability (Note C)

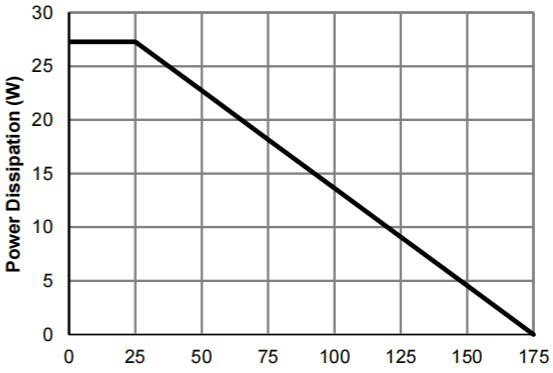


Figure 13: Power De-rating (Note F)

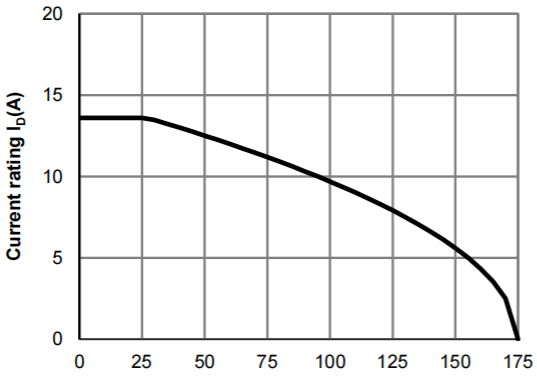


Figure 14: Current De-rating (Note F)

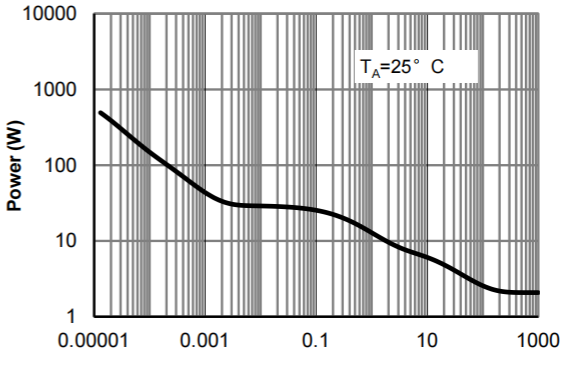


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

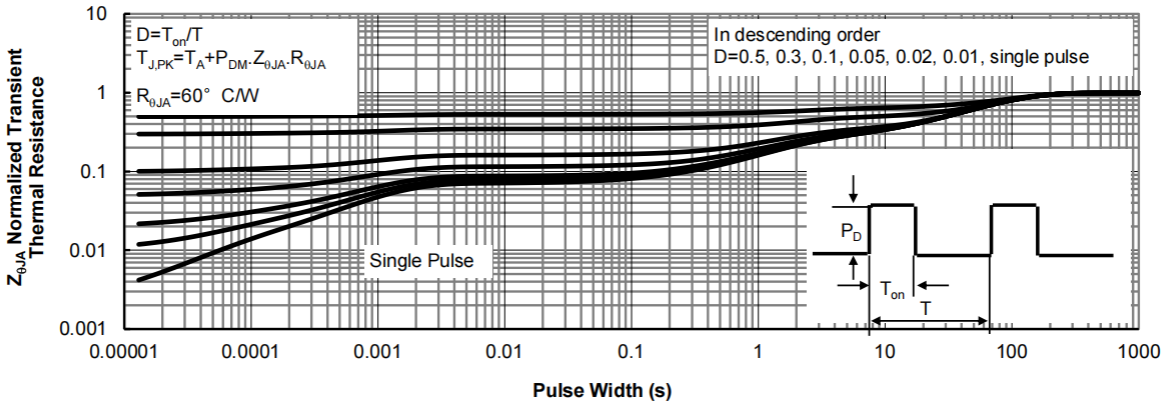
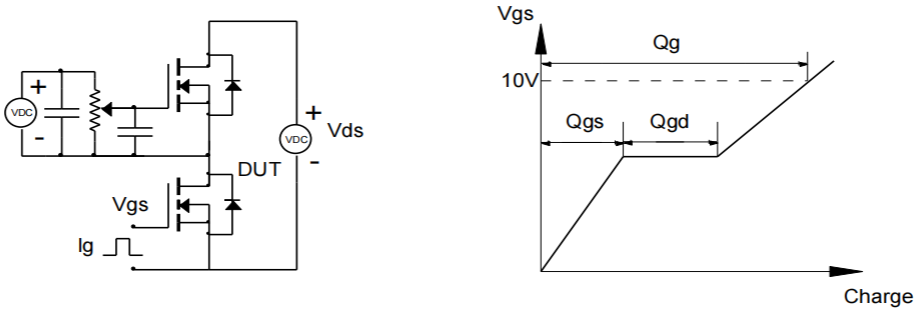
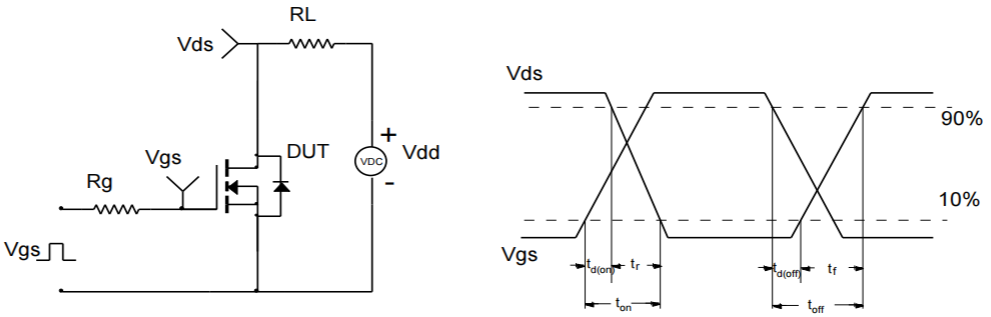


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

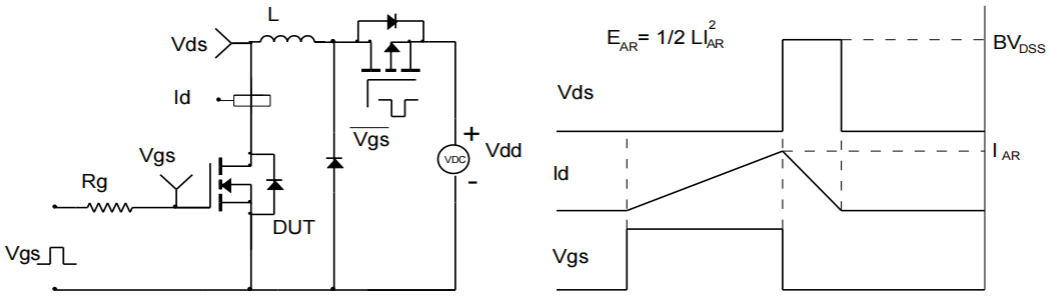
Gate Charge Test Circuit & Waveform



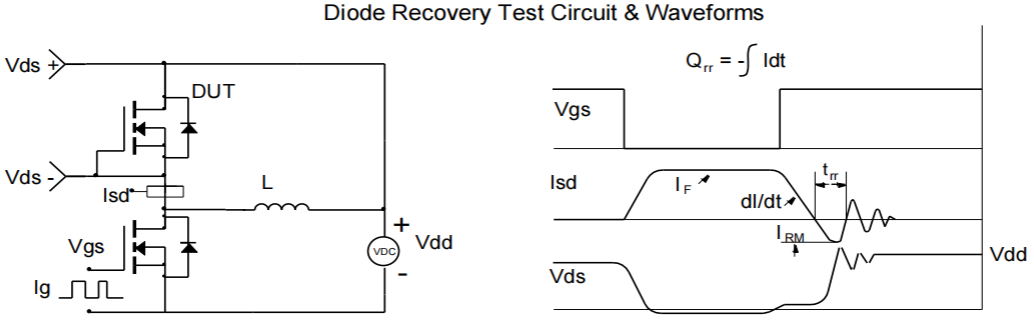
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-60V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-1.5	-2.1	-3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-12A		91	115	mΩ
		T_J=125°C		150	180	
		V_{GS}=-4.5V, I_D=-8A		114	150	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-12A		12		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.76	-1	V
I_S	Maximum Body-Diode Continuous Current [G]				-12	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-30V, f=1MHz		960		pF
C_{oss}	Output Capacitance			86		pF
C_{rss}	Reverse Transfer Capacitance			38		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		9.5	15	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-30V, I_D=-12A		15.8	22	nC
Q_g(4.5V)	Total Gate Charge			7.4	12	nC
Q_{gs}	Gate Source Charge			3		nC
Q_{gd}	Gate Drain Charge			3.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-30V, R_L=2.5Ω, R_{GEN}=3Ω		9		ns
t_r	Turn-On Rise Time			10		ns
$t_{D(off)}$	Turn-Off DelayTime			25		ns
t_f	Turn-Off Fall Time			11		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-12A, dI/dt=100A/µs		27.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-12A, dI/dt=100A/µs		30		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

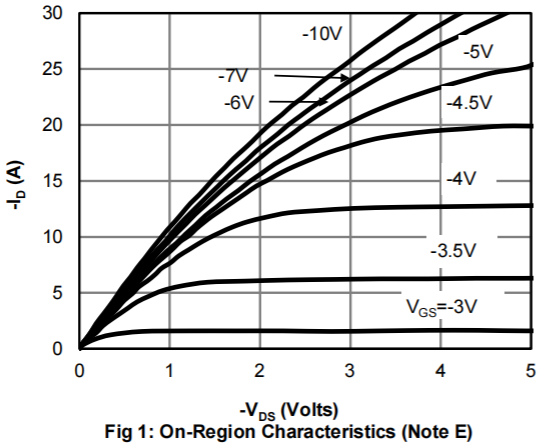


Fig 1: On-Region Characteristics (Note E)

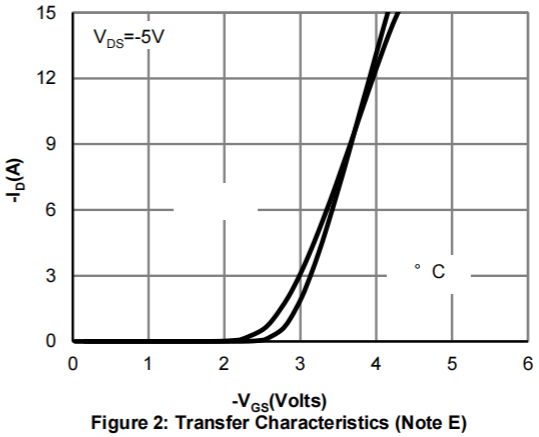


Figure 2: Transfer Characteristics (Note E)

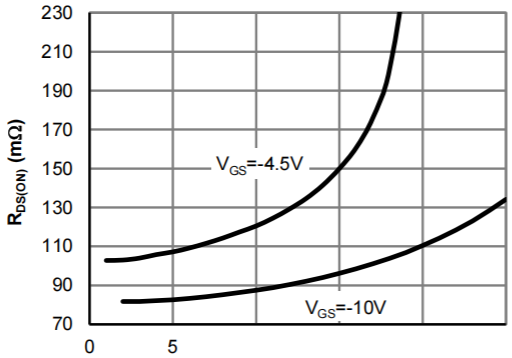


Figure 3: On-

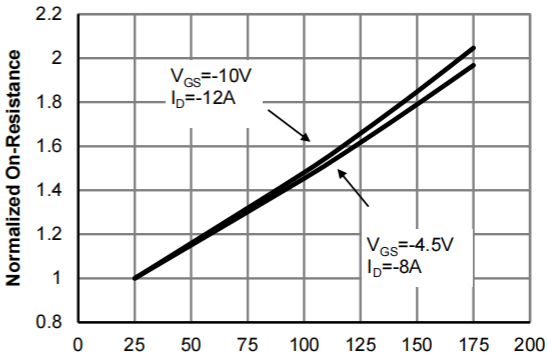


Figure 4: On-Resistance vs. Junction Temperature (Note E)

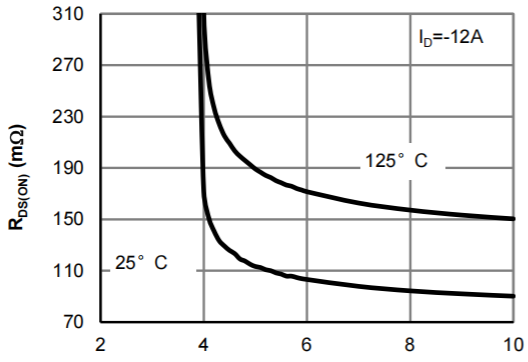


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

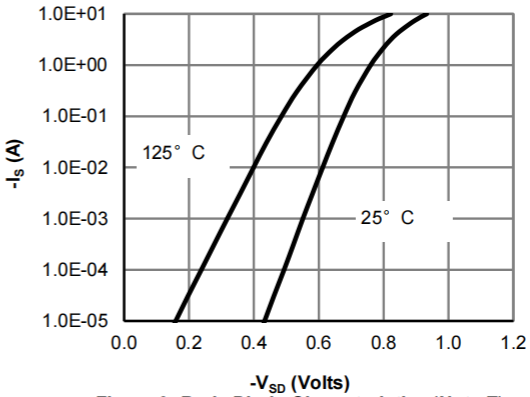


Figure 6: Body-Diode Characteristics (Note E)

P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

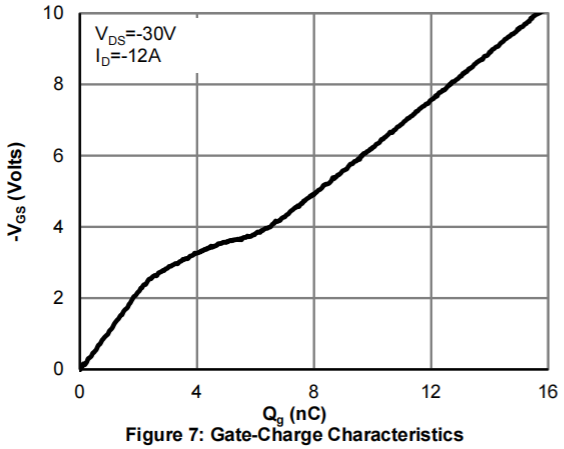


Figure 7: Gate-Charge Characteristics

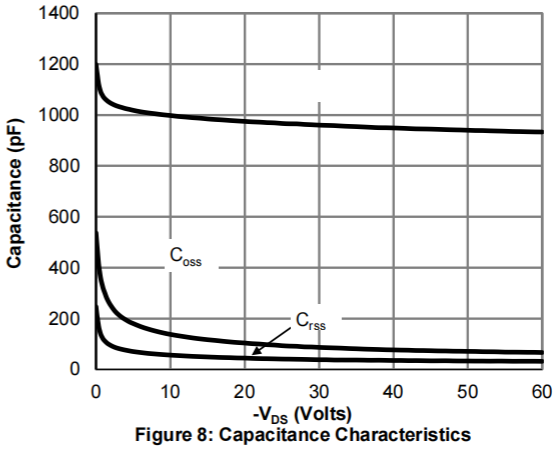


Figure 8: Capacitance Characteristics

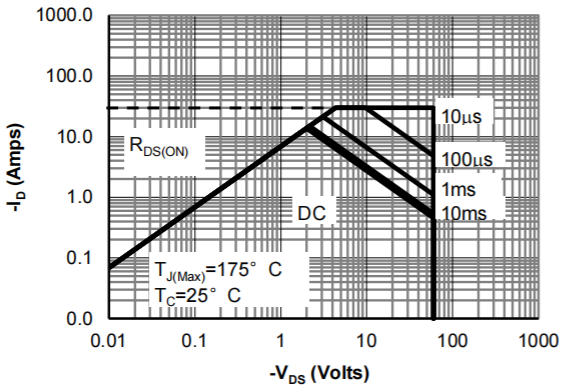


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

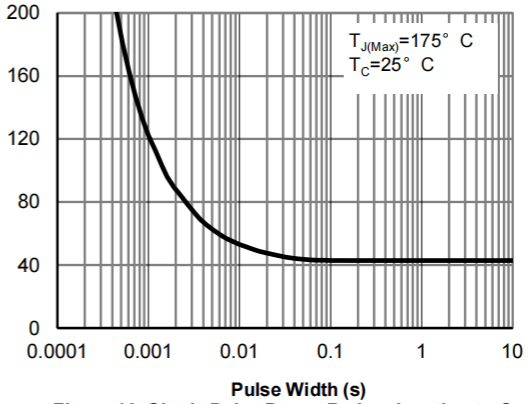


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

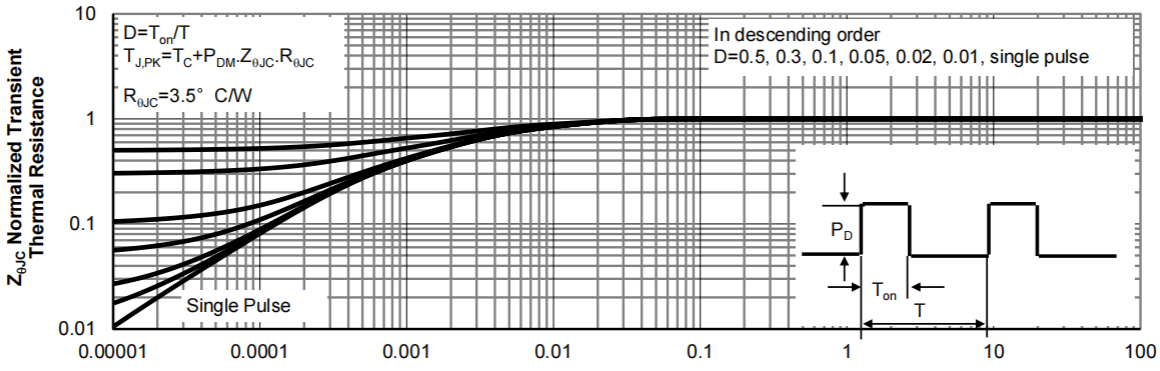


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

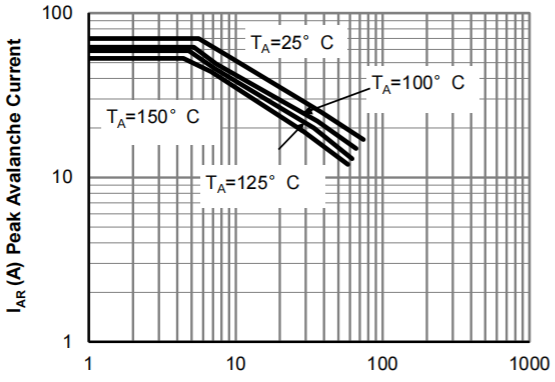


Figure 12: Single Pulse Avalanche capability (Note C)

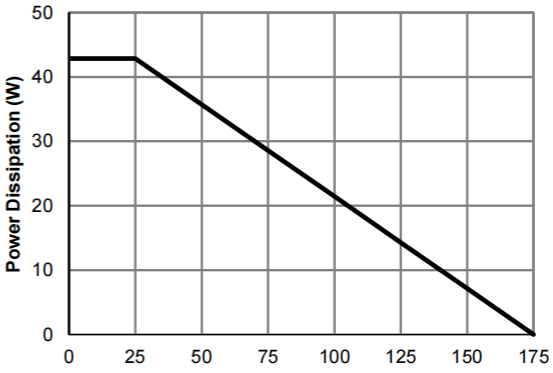


Figure 13: Power De-rating (Note F)

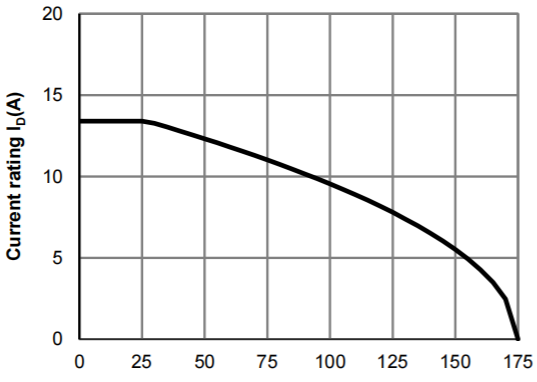


Figure 14: Current De-rating (Note F)

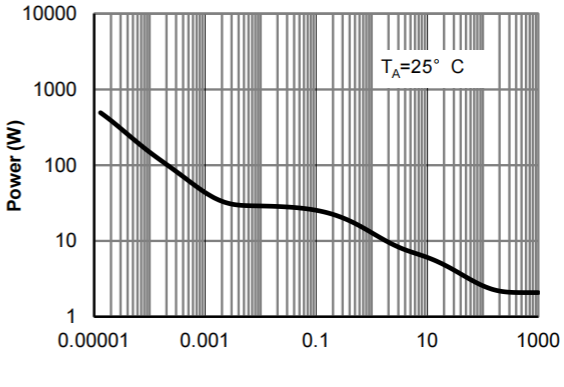


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

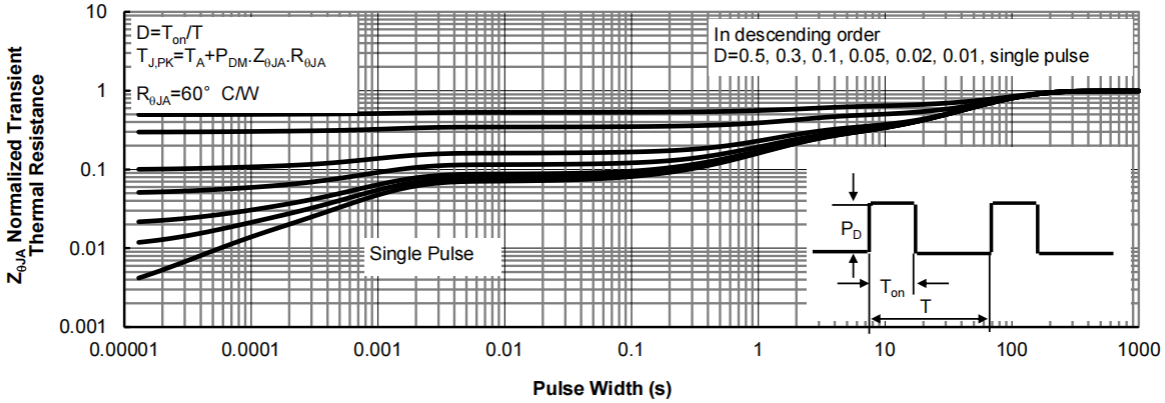
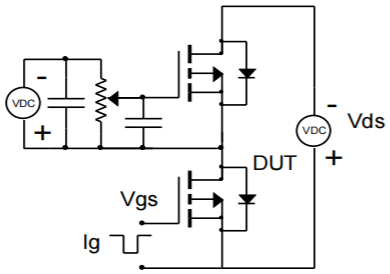
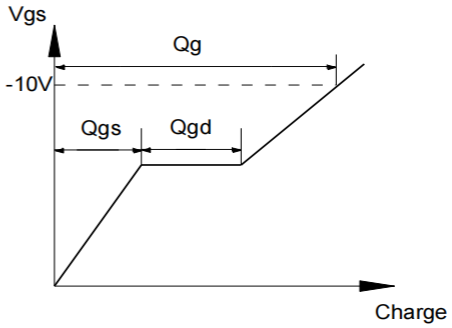


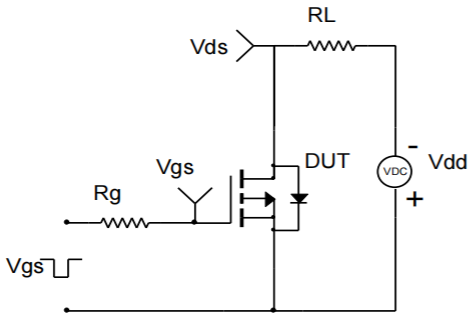
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

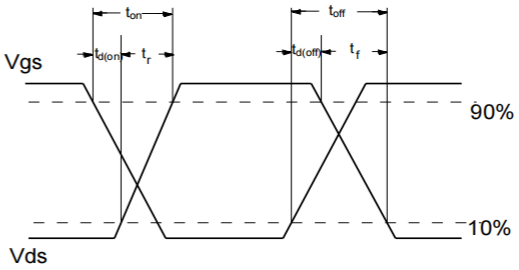
Gate Charge Test Circuit & Waveform



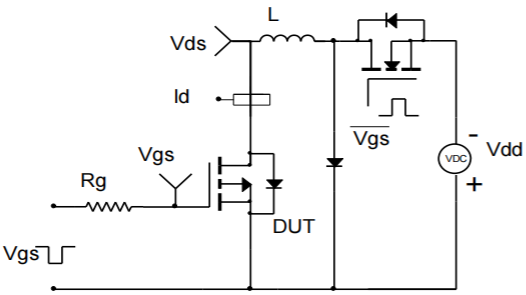


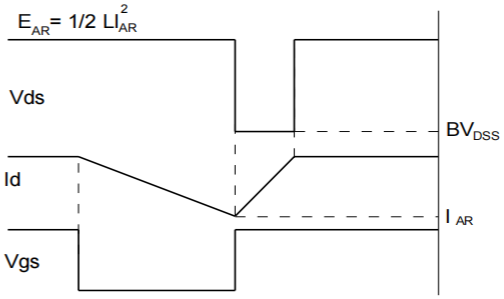
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms