UMW®
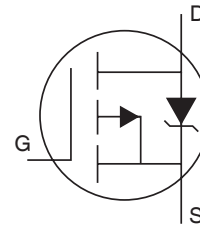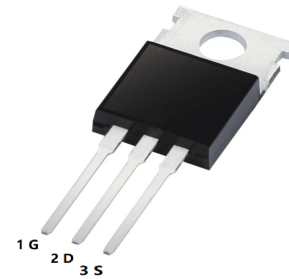
Description

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Features

- V_{DS} (V) = -60V

- I_D = -31A (V_{GS} = -10V)

- $R_{DS(ON)}$ < 60mΩ (V_{GS} = -10V)
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
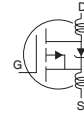- Fully Avalanche Rated Lead-Free

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-31	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V	-22	A
I_{DM}	Pulsed Drain Current ①	-110	
P_D @T_C = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	280	mJ
I_{AR}	Avalanche Current①	-16	A
E_{AR}	Repetitive Avalanche Energy①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case		1.4	
$R_{θCS}$	Case-to-Sink, Flat, Greased Surface	0.50		°C/W
$R_{θJA}$	Junction-to-Ambient		62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-60			V	V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		-0.034		V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance			60	mΩ	V_{GS} = -10V, I_D = -16A ④
$V_{GS(th)}$	Gate Threshold Voltage	-1.1	-2	-3.0	V	V_{DS} = V_{GS}, I_D = -250μA
g_{fs}	Forward Transconductance	8.0			S	V_{DS} = -25V, I_D = -16A
I_{DSS}	Drain-to-Source Leakage Current			-25	μA	V_{DS} = -55V, V_{GS} = 0V
				-250		V_{DS} = -44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage			100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage			-100		V_{GS} = -20V
Q_g	Total Gate Charge			63		I_D = -16A
Q_{gs}	Gate-to-Source Charge			13	nC	V_{DS} = -44V
Q_{gd}	Gate-to-Drain ("Miller") Charge			29		V_{GS} = -10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time		14			V_{DD} = -28V
t_r	Rise Time		66			I_D = -16A
$t_{d(off)}$	Turn-Off Delay Time		39		ns	R_G = 6.8Ω
t_f	Fall Time		63			R_D = 1.6Ω, See Fig. 10 ④
L_D	Internal Drain Inductance		4.5			Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance		7.5		nH	from package and center of die contact
C_{iss}	Input Capacitance		1200			V_{GS} = 0V
C_{oss}	Output Capacitance		520		pF	V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance		250			ƒ = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)			-31	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①			-110		
V_{SD}	Diode Forward Voltage			-1.3	V	T_J = 25°C, I_S = -16A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time		71	110	ns	T_J = 25°C, I_F = -16A
Q_{rr}	Reverse RecoveryCharge		170	250	nC	di/dt = -100A/μs ④

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = -25V, starting T_J = 25°C, L = 2.1mH
   R_G = 25Ω, I_{AS} = -16A. (See Figure 12)

③ $I_{SD} \leq$ -16A, di/dt $\leq$ -280A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

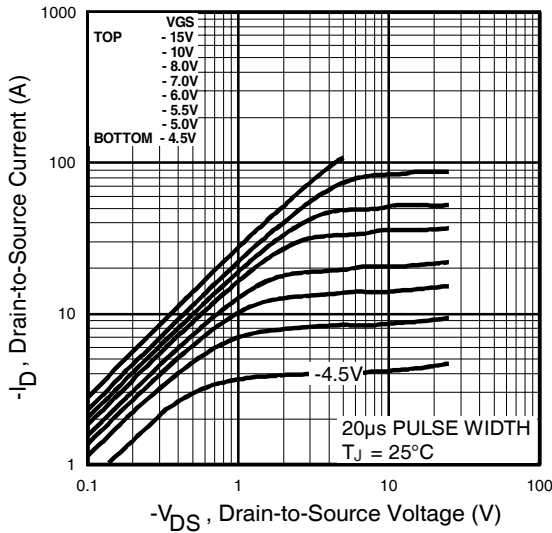④ Pulse width $\leq$ 300μs; duty cycle $\leq$ 2%.
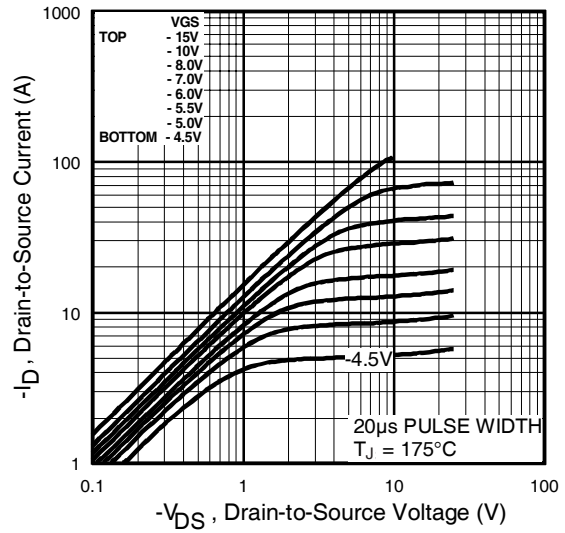
Fig 1. Typical Output Characteristics

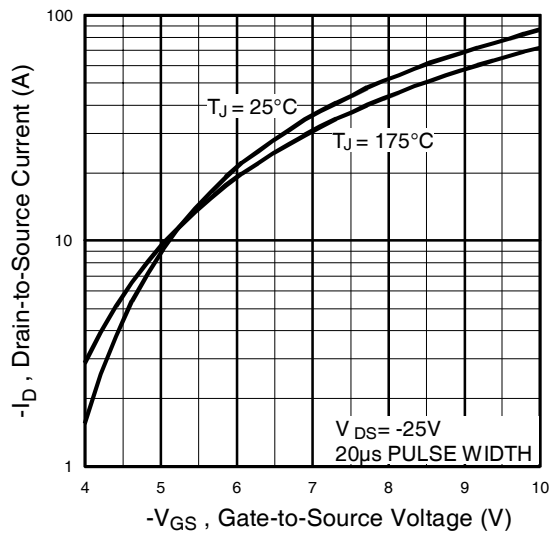Fig 2. Typical Output Characteristics

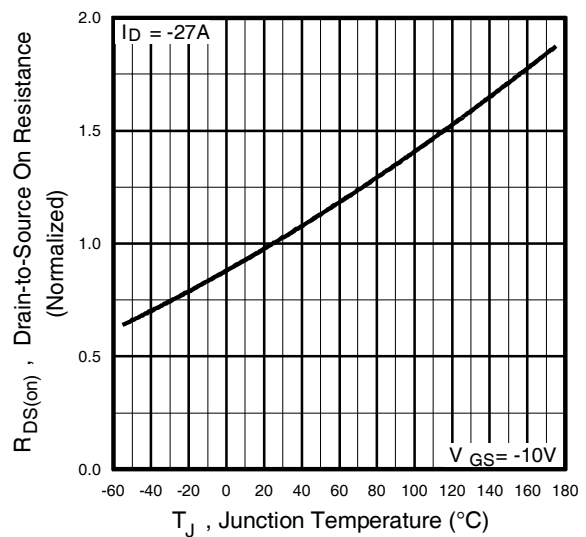Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance
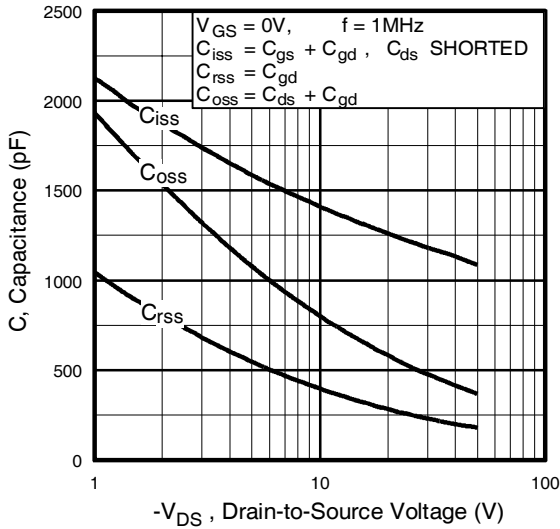Vs. Temperature

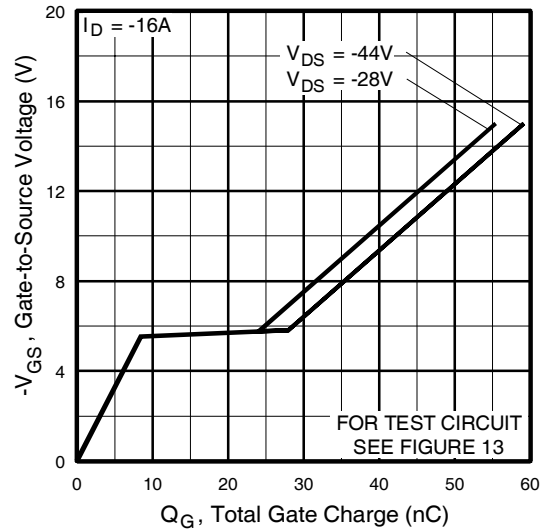**Fig 5.** Typical Capacitance Vs.
Drain-to-Source Voltage

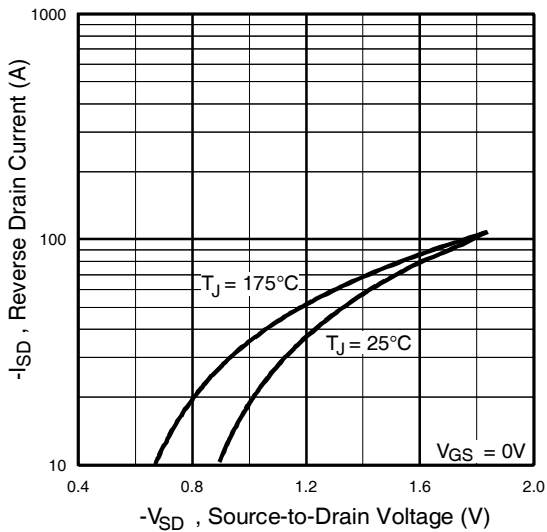**Fig 6.** Typical Gate Charge Vs.
Gate-to-Source Voltage

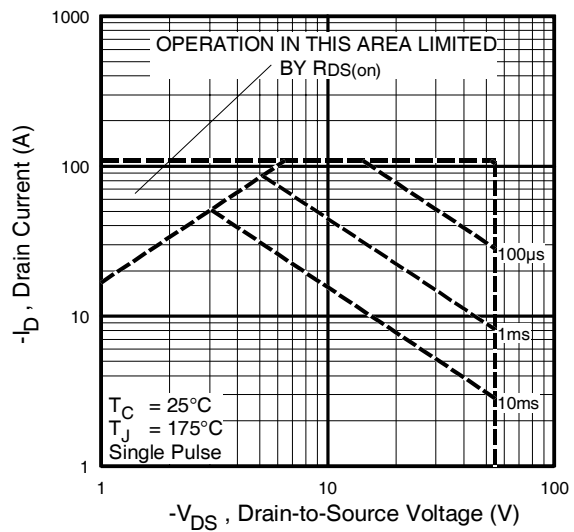
Fig 7. Typical Source-Drain Diode
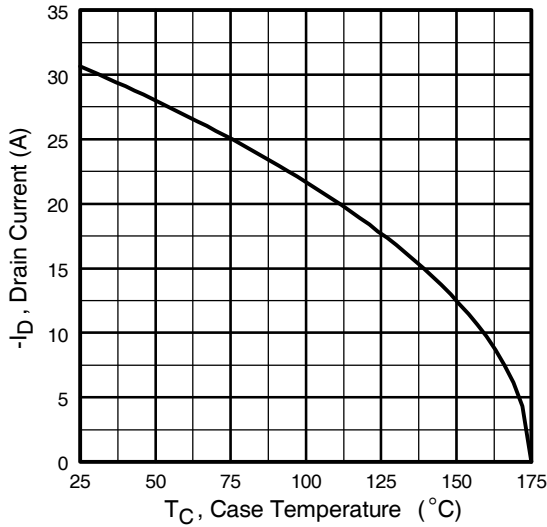Forward Voltage

Fig 8. Maximum Safe Operating Area
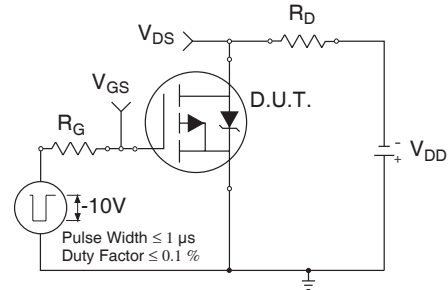
Fig 9. Maximum Drain Current Vs. Case Temperature

Fig 10a. Switching Time Test Circuit

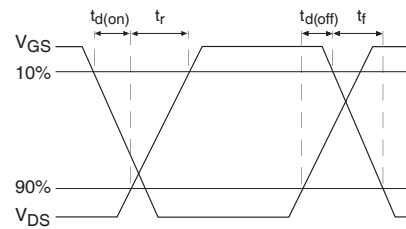**Fig 10b.** Switching Time Waveforms

Notes:
1. Duty factor $D = t_1 / t_2$
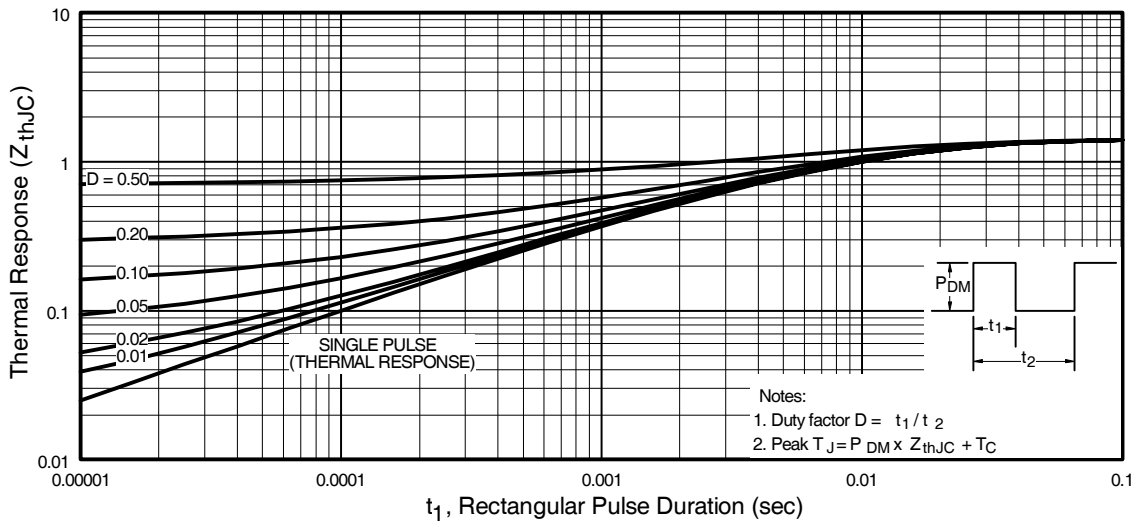2. Peak $T_J = P_{DM} \times Z_{thJC} + T_C$

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 12a. Unclamped Inductive Test Circuit

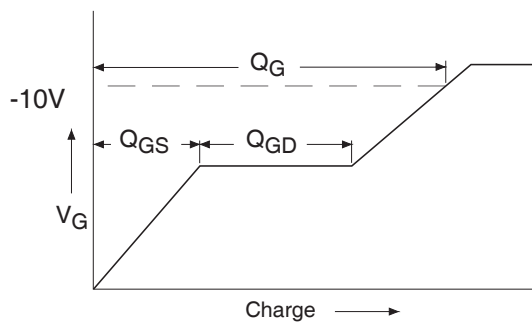**Fig 12b.** Unclamped Inductive Waveforms

Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

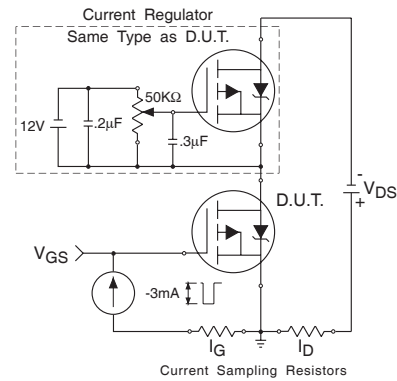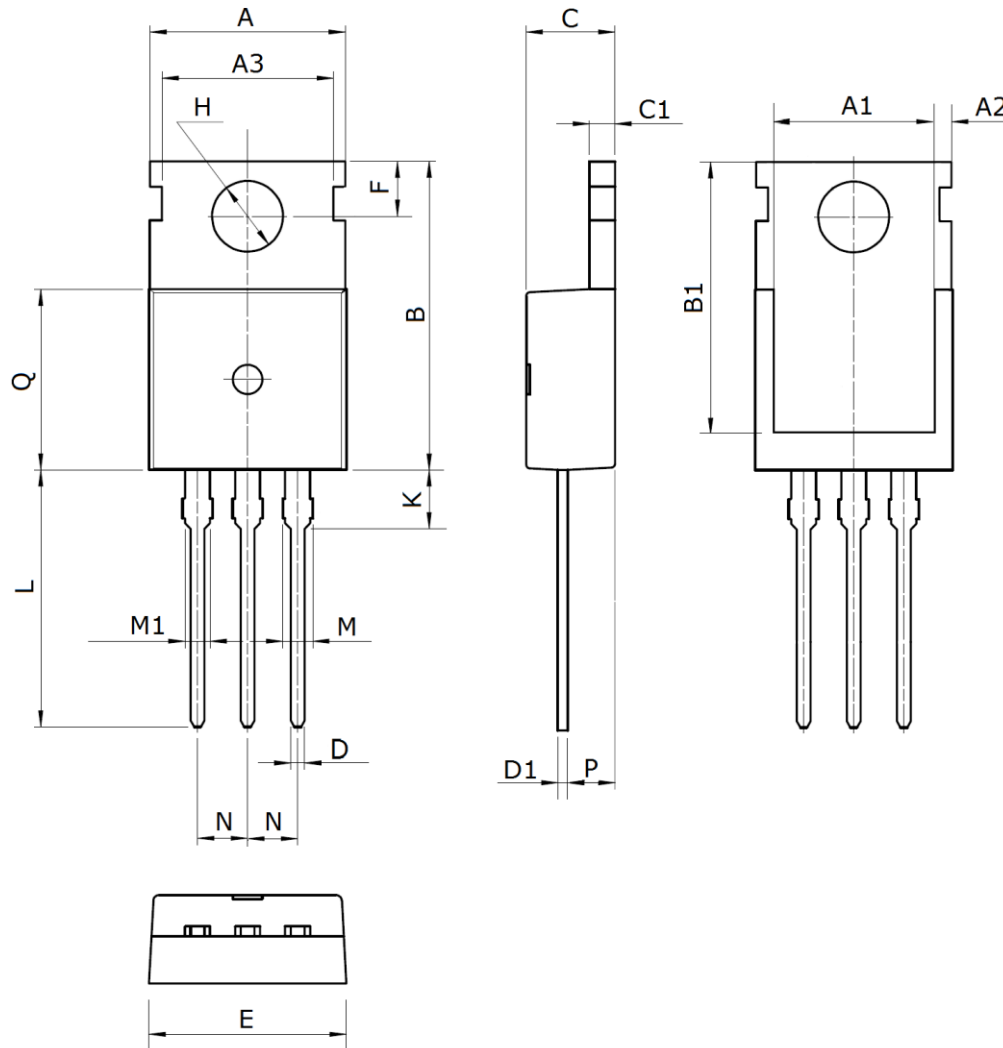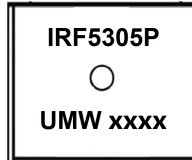**Fig 13a.** Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

Package Mechanical Data TO-220

Symbol	Dimensions（mm）	Symbol	Dimensions (mm)	Symbol	Dimensions (mm)
A	10.0±0.3	C1	1.3±0.2	L	13.2±0.4
A1	8.0±0.2	D	0.8±0.2	M	1.38±0.1
A2	0.94±0.1	D1	0.5±0.1	M1	1.28±0.1
A3	8.7±0.1	E	10.0±0.3	N	2.54(typ)
B	15.6±0.4	F	2.8 ±0.1	P	2.4±0.3
B1	13.2 ±0.2	H	3.6±0.1	Q	9.15±0. 25
C	4.5±0. 2	K	3.1±0.2		

Marking

IRF5305P

○

UMW xxxx

Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IRF5305PBF	TO-220	1000	Tape and reel