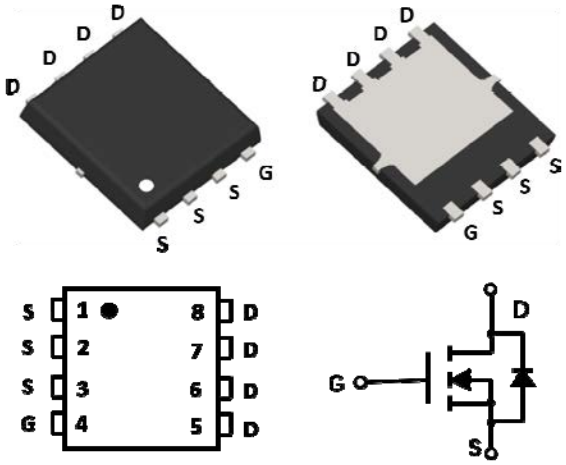
SKG85G06A

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 60V
- I_D 130A
- I_D (Package limited) 85A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜3.0 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜4.5 mohm
- 100% UIS Tested
- 100% ▽V_{DS} Tested

PDFN5060-8L



General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current		I_D	130	A
Drain Current [A]	T_C=25℃	I_D	85	A
	T_C=100℃		54	
Pulsed Drain Current [B]		I_{DM}	390	A
Avalanche energy [C]		EAS	270	mJ
Total Power Dissipation [D]		P_D	105	W
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	1.2	℃/ W
Thermal Resistance Junction-to-Ambient [E]		$R_{\theta JA}$	55	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SKG85G06A	F1	SKG85G06A	5000	10000	50000	13“ reel

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=20A		2.5	3.0	mΩ
		V_{GS}= 4.5V, I_D=10A		3.5	4.5	
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				85	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=30V,V_{GS}=0V,f=1MHz		3350		pF
Output Capacitance	C_{oss}			1666		
Reverse Transfer Capacitance	C_{rss}			77.7		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=30V,I_D=25A		66.1		nC
Gate-Source Charge	Q_{gs}			10.7		
Gate-Drain Charge	Q_{gd}			10.9		
Reverse Recovery Chrage	Q_{rr}	I_F=25A, di/dt=100A/us		73		
Reverse Recovery Time	t_{rr}			68		ns
Turn-on Delay Time	$t_{d(on)}$	V_{GS}=10V,V_{DD}=30V,I_D=25A R_{GEN}=2Ω		22.5		
Turn-on Rise Time	t_r			6.7		
Turn-off Delay Time	$t_{d(off)}$			80.3		
Turn-off fall Time	t_f			26.9		

Note:

A. The maximum current rating is package limited.

B. Repetitive rating; pulse width limited by max. junction temperature.

C. V_{DD}=50 V, R_G=25 Ω, L=0.5 mH, starting T_j=25 ℃.

D. P_D is based on max. junction temperature, using junction-case thermal resistance.

E. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with Ta=25 ℃.

Typical Performance Characteristics

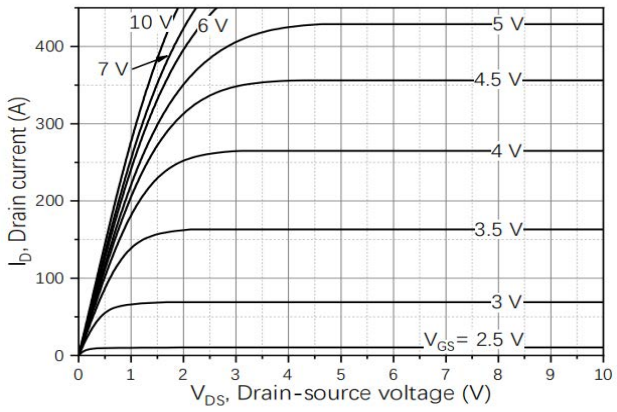


Figure1. Output Characteristics

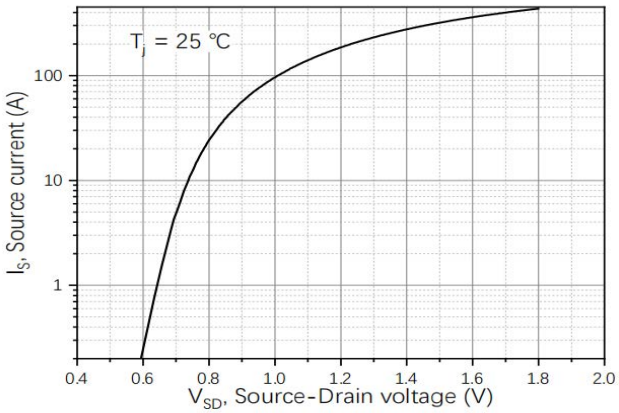


Figure2. Transfer Characteristics

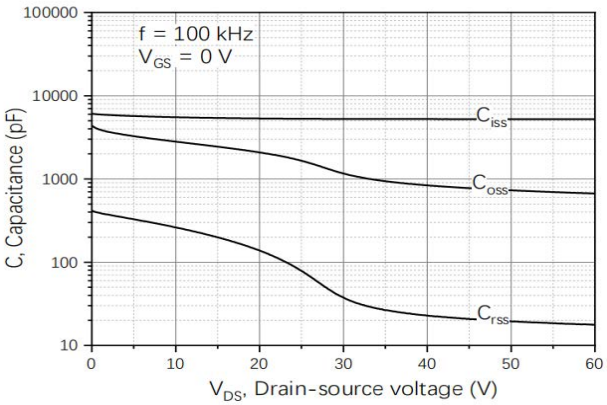


Figure3. Capacitance Characteristics

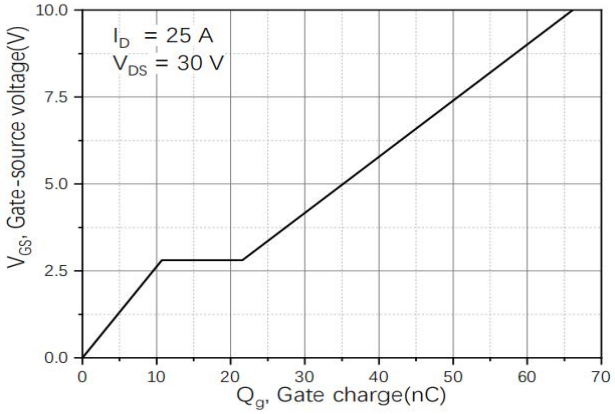


Figure4. Gate Charge

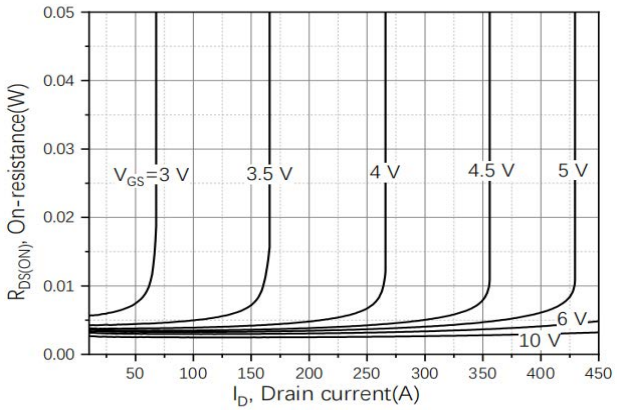


Figure5. Drain-Source on Resistance

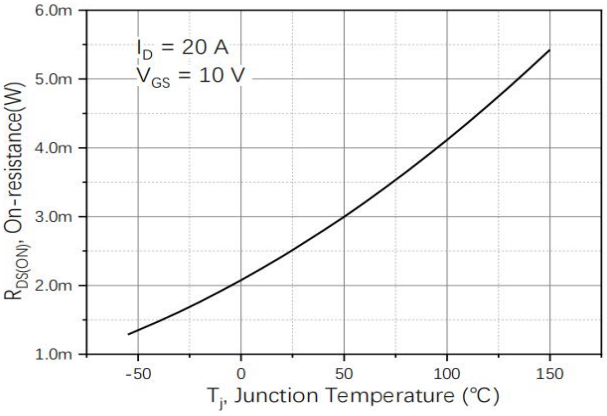


Figure6. Drain-Source on Resistance

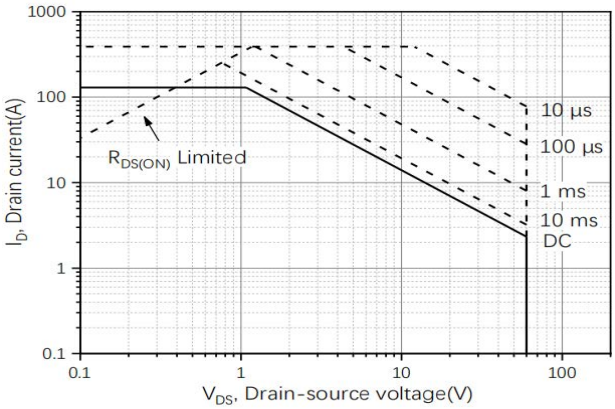


Figure7. Safe Operation Area

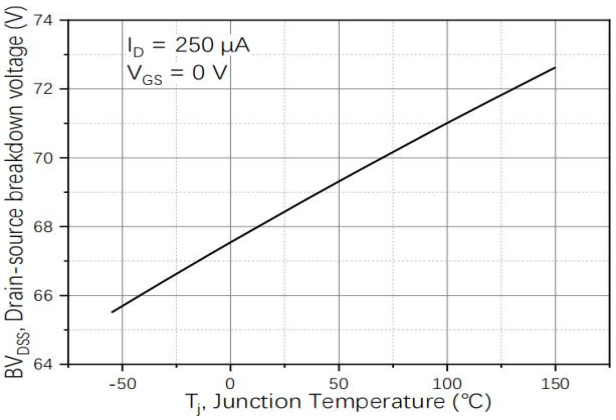


Figure8. Drain-source breakdown voltage

Test circuits and waveforms

Figure A: Gate Charge Test Circuit & Waveforms

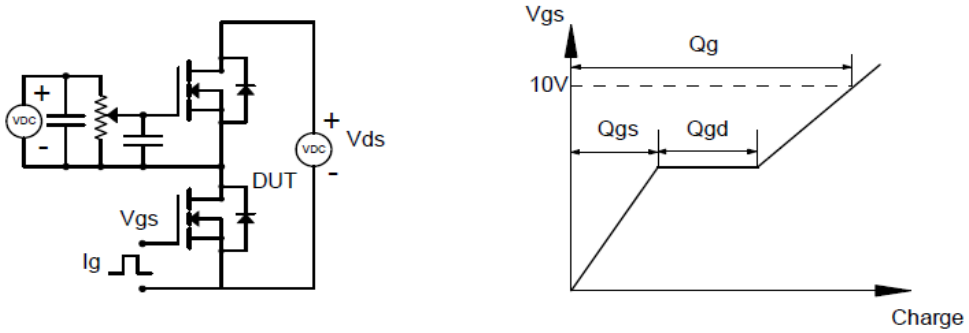


Figure B: Resistive Switching Test Circuit & Waveforms

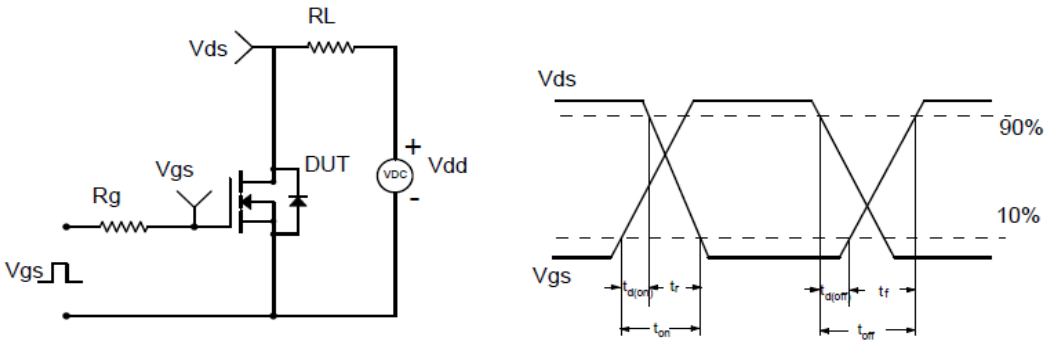


Figure C: Unclamped Inductive Switching (UIS) Test

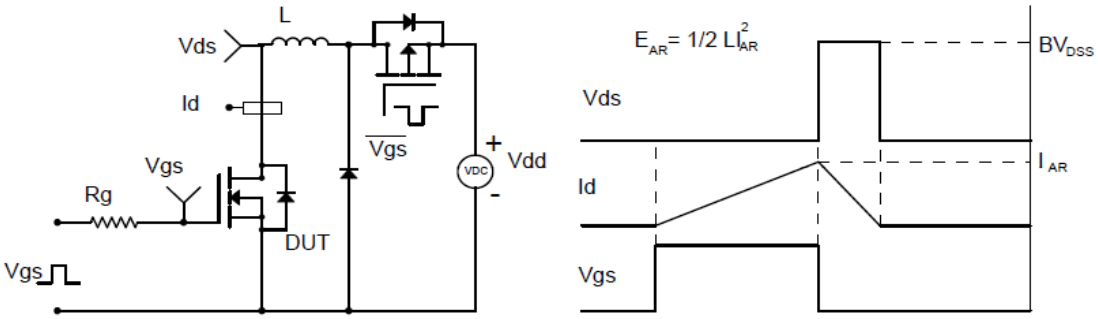
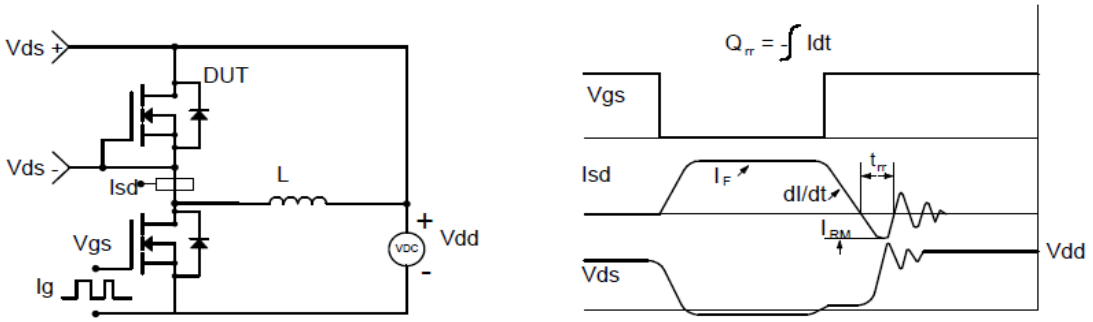


Figure D: Diode Recovery Test Circuit & Waveforms



PDFN5060-8L Package Information