

Pulse width modulation circuit

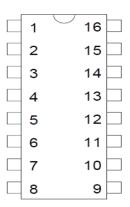
Description:

CD4017 is a 5th order Johnson decoding counter with 10 decoding outputs, CLOCK, RE, INH inputs, and a Schmidt trigger with pulse shaping function at the clock input, which has no limit on the rise and fall time of input clock pulses. INH is low level, and the counter counts on the rising edge of the clock; On the contrary, the counting function is invalid. RE is high level, and the counter is reset to zero. Its main characteristics are as follows:

Features:

- -Fully static operation
- -5V, 10V, 15V parameter standard range
- -Standard symmetrical output characteristics
- -Working within the industrial standard temperature range (-40~85) -100% static current tested at 20V
- -Packaging form: DIP16/SOP16

Pin Assignment:



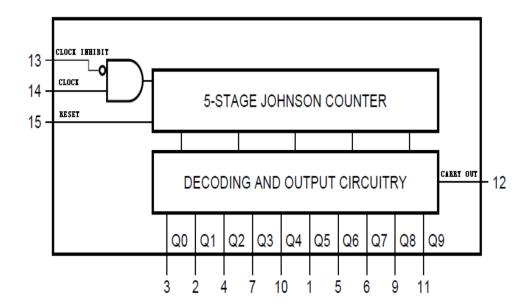
Pin No.	Symbol	Pin Definition	Pin No.	Symbol	Pin Definition
1	Q5	Decoding output terminal	16	VDD	power supply
2	Q1	Decoding output terminal	15	RESET	RESET
3	Q0	Decoding output terminal	14	CLOCK	CLOCK
4	Q2	Decoding output terminal	13	CLOCK INHIBIT	Clock suppression
5	Q6	Decoding output terminal	12	CARRY OUT	Carry output terminal
6	Q7	Decoding output terminal	11	Q9	Decoding output terminal
7	Q3	Decoding output terminal	10	Q4	Decoding output terminal
8	Vss	grounds	9	Q8	Decoding output terminal



Absolute Maximum Ratings

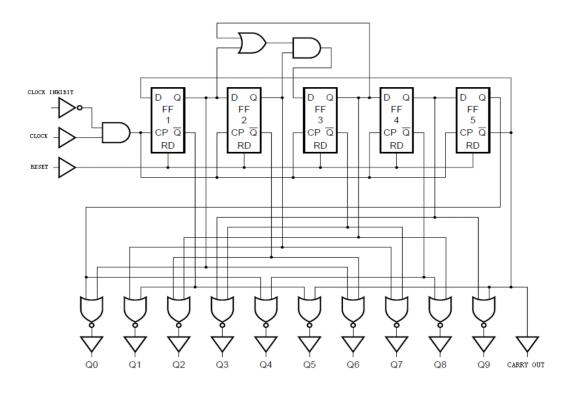
parameter	symbol	limit value	unit
supply voltage	V_{DD}	-0.5~20	V
INPUT VOLTAGE	Vı	-0.5~VDD+0.5	V
Input and output current	±Ι	±10	mA
consumption	P _D	500	mW
Output power consumption	Р	100	mW
Ambient Temperature	Tamb	-40~+85	°C
Storage temperature	Tstg	-65~+150	°C
welding temperature	TL	250	°C

Functional Block Diagram





Logic diagram



Truth table

	Onesation			
MR	CP0	CP1	Operation	
Н	X	X	Q0=Q5-9=H; Q1 to Q9=L	
L	Н	\	counter advances	
L	↑	L	counter advances	
L	L	X	no change	
L	X	Н	no change	
L	Н	↑	no change	
L	<u> </u>	L	no change	

Note:

H=HIGH voltage level; L=LOW voltage level; X=don't care;

↑=positive-going transition; ↓=negative-going transition.



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
supply voltage	$V_{ m DD}$	-	3	-	15	V
ambient temperature	T_{amb}	in free air	-40	-	+105	$^{\circ}$
-11i		$V_{DD}=5V$	ı	-	2.5	MHz
clock input frequency	${ m f_{CL}}$	$V_{DD}=10V$	ı	-	5	MHz
requeries		$V_{DD}=15V$	1	-	5.5	MHz
		$V_{DD}=5V$	200	-	-	ns
clock pulse width	$t_{\rm w}$	$V_{DD}=10V$	90	-	ı	ns
		$V_{DD}=15V$	60	-	-	ns
.11		$V_{DD}=5V$				-
clock rise and fall time	t_{rCL}, t_{fCL}	$V_{DD}=10V$	unlimited			-
ian time		$V_{DD}=15V$				-
.11. 11.11.14		$V_{DD}=5V$	230	-	1	ns
clock inhibit setup time	t _s	$V_{DD}=10V$	100	-	1	ns
setup time		$V_{DD}=15V$	70	-	1	ns
		$V_{DD}=5V$	260	-	1	ns
reset pulse width	t _{RW}	$V_{DD}=10V$		-	-	ns
		$V_{DD}=15V$	60	-	-	ns
1		$V_{DD}=5V$		-	-	ns
reset removal time	t_{rec}	$V_{DD}=10V$	280	-	-	ns
time		$V_{DD}=15V$	150	-	-	ns



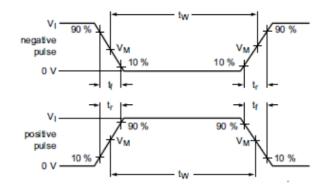
DC Characteristics

(T_{amb}=25 $^{\circ}$ C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

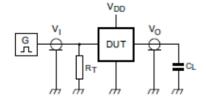
D	Symbol	Conditions (V)			T _{amb} =25°C			T T •.
Parameter		Vo	V _{IN}	V_{DD}	Min.	Тур.	Max.	Unit
		-	0, 5	5		0.04	5	uA
supply current	I_{DD}	-	0, 10	10	-:1	0.04	10	uA
	111	-	0, 15	15	-	0.04	20	uA
LOWI		0.4	0, 5	5	0.51	1	-	mA
LOW-level output current	I_{OL}	0.5	0, 10	10	1.3	2.6	-	mA
output current		1.5	0, 15	15	3.4	6.8	-	mA
		4.6	0, 5	5	-0.51	-1	-	mA
HIGH-level	T	2.5	0, 5	5	-1.6	-3.2	-	mA
output current	І _{ОН}	9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
LOWI	V _{OL}	-	0, 5	5		0	0.05	V
LOW-level output voltage		-	0, 10	10	-	0	0.05	V
output voltage		-	0, 15	15	-	0	0.05	V
IIICII II	V _{OH}	-	0, 5	5	4.95	5	_	V
HIGH-level output voltage		-	0, 10	10	9.95	10	-	V
output voltage		-	0, 15	15	14.95	15	-	V
LOWI	V _{IL}	0.5, 4.5	-	5		-	1.5	V
LOW-level input voltage		1, 9	-	10	-	1.4	3	V
input voitage		1.5, 13.5		15	==	-	4	V
IIICII 11	V _{IH}	0.5, 4.5	-	5	3.5	-	-	V
HIGH-level input voltage		1, 9	-	10	7	-	-	V
input voltage		1.5, 13.5	78	15	11	-	-	V
input leakage current	$I_{\rm I}$	-	0, 15	15	-	±10 ⁻⁵	±0.1	uA



AC Testing Circuit



a. Input waveforms



b. Test circuit

Figure 6. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

 R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

AC Testing Waveforms

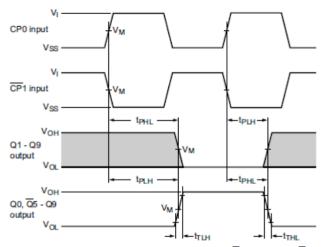
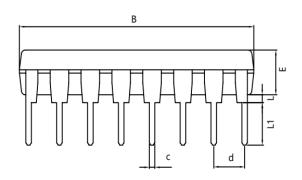


Figure 7. Waveforms showing the propagation delays for CP0, $\stackrel{\frown}{\text{CP}}1$ to Qn, $\stackrel{\frown}{\text{Q}}5$ -9 outputs and the output transition times

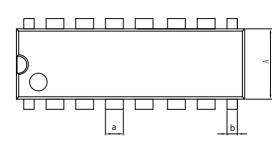


PACKAGE MECHANICAL DATA

DIP16

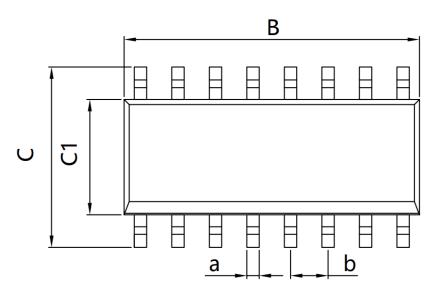


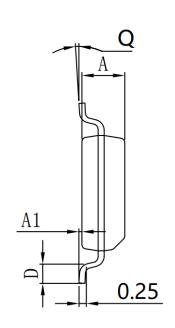




Dimensions In Millimeters								
Symbol:	Min :	Max:	Symbol:	Min :	Max:			
Α	6.100	6.680	L	0.500	0.800			
В	18.940	19.560	а	1.524 TYP				
D	8.200	9.200	b	0.889 TYP				
D1	7.42	7.820	С	0.457 TYP				
E	3.100	3.550	d	2.540 TYP				
L	0.500	0.800						

SOP16





Dimensions In Millimeters								
Symbol: Min: Max: Symbol: Min: Max:								
Α	1.225	1.570	D	0.400	0.950			
A1	0.100	0.250	Q	0°	8°			
В	9.800	10.00	а	0.420 TYP				
С	5.800	6.250	b	1.270 TYP				
C1	3.800	4.000						