

1. DESCRIPTION

The XL4021B is a 8-stage parallel- or serial-input/serial output chip having common CLOCK and PARALLEL/SERIALCONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. In the XL4021B serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the XL4021B, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

The XL4021B is supplied in packages SOP16.

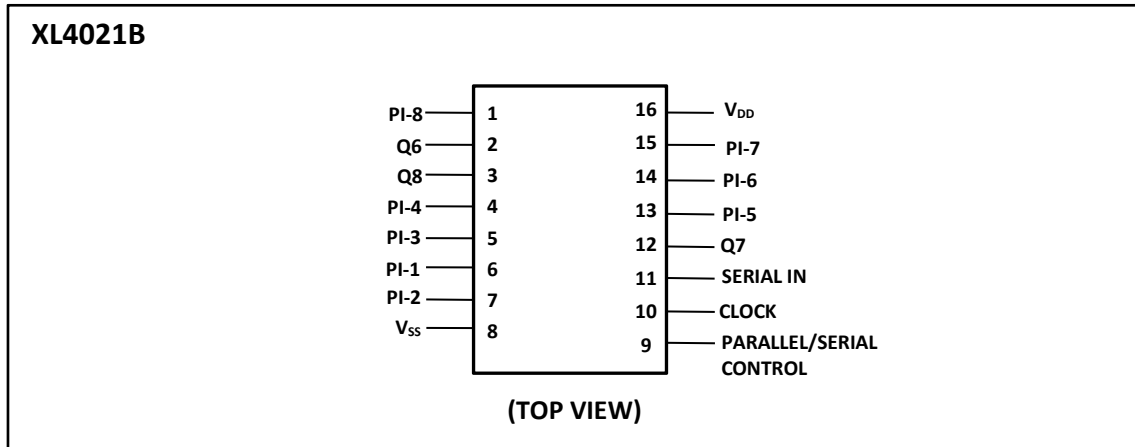
2. FEATURES

- Medium-speed operation ... 12 MHz (typ.) clock rate at $V_{DQ}-V_{SS} = 10\text{ V}$
- Fully static operation
- 8 master-slave flip-flops plus output buffering and control gating
- 100% tested for quiescent current at 20 V
- Maximum input current of $1\mu\text{A}$ at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = $1\mu\text{A}$ at $V_{DD} \ll 5\text{ V}$
 - 2 V at $V_{DD} = 10\text{ V}$
 - 2.5 V at $V_{DD} = 15\text{ V}$
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

3. Applications

- Parallel input/serial output data queueing
- Parallel to serial data conversion
- General-purpose register

4. PIN FUNCTIONS



Pin number	Symbol	Name and function
6, 7, 5, 4, 13, 14, 15, 1	PI-1 to PI-8	Parallel input
11	SERIAL IN	Serial input
9	PARALLEL/SERIAL CONTROL	Parallel/serial input control
10	CLOCK	Clock input
2, 3, 12	Q6, Q7, Q8	Buffered outputs
8	V _{SS}	Negative supply voltage
16	V _{DD}	Positive supply voltage

5. LOGIC DIAGRAM

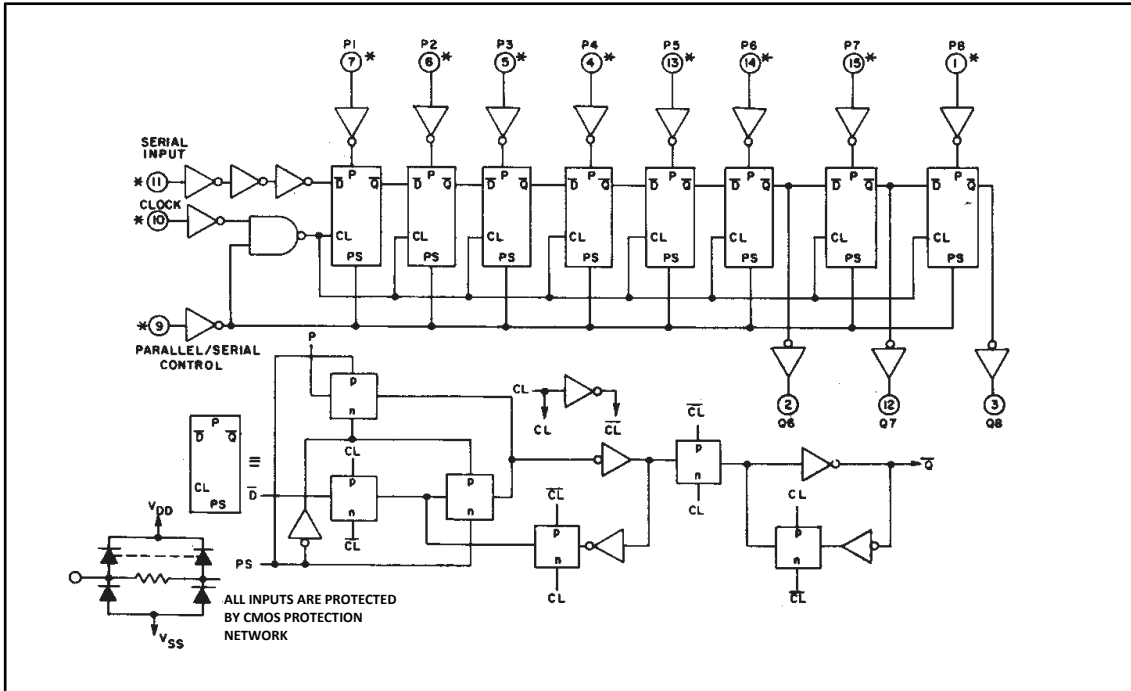


Fig. 1 Logic diagram for XL4021B.

CL	Serial Input	Paralle/ Serial Control	PI-1	PI-n	Qi (Internal)	On
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
$\sqrt{\quad}$	0	0	X	X	0	Qn 1
$\sqrt{\quad}$	1	0	X	X	1	Qn 1
\swarrow	X	0	X	X	Qi	On

[1] X - DON'T CARE CASE

6. SPECIFICATIONS

6.1. Absolute Maximum Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{DD}	DC SUPPLY-VOLTAGE RANGE	Voltages referenced to V _{gg} Terminal	-	+20	V
V _{IN}	INPUT VOLTAGE RANGE, ALL INPUTS	ALL INPUTS	-	V _{DD} +0.5	V
V _O	DC INPUT CURRENT, ANY ONE INPUT		-10	+10	mA
P _D	POWER DISSIPATION PER PACKAGE	For T _A = -55°C to +100°C	-	500	mW
		For T _A = +100°C to +125°C	Derate linearity at 12mW/°C to 200mW		
P _{DDO}	DEVICE DISSIPATION PER OUTPUT TRANSISTOR	F _{ORTA} = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	-	+100	mW
T _A	OPERATING TEMPERATURE RANGE (T _A)		-40	+85	°C
T _{stg}	STORAGE TEMPERATURE RANGE		-50	+125	°C
T _L	LEAD TEMPERATURE (DURING SOLDERING)	At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	-	+265	°C

6.2. Recommended Operating Conditions at T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V _{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (T _A = Full Package-Temperature Range)	-	3	18	V
Clock Pulse Width, t _w	5	180	-	ns
	10	80	-	
	15	50	-	
Clock Frequency, f _{CL}	5	-	3	MHz
	10	-	6	
	15	-	8.5	
Clock Rise and Fall Time, t _{rCL} , t _{fCL}	5	-	15	MS
	10	-	15	
	15	-	15	
Set-up Time, t _S : Serial Input (ref. to CL)	5	120	-	ns
	10	80	-	
	15	60	-	
Parallel Inputs XL4021B (ref. to P/S)	5	50	-	ns
	10	30	-	
	15	20	-	
Parallel/Serial Pulse Width, t _w (XL4021B)	5	160	-	ns
	10	80	-	
	15	50	-	
Parallel/Serial Removal Time, t _{REM} (XL4021B)	5	280	-	ns
	10	140	-	
	15	100	-	

6.3. Static Electrical Characteristics

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V ₀ (V)	V _{IN} <V>	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{QD} Max.	-	0,5	5	5	5	150	150	-	0.04	5	mA
	-	0,10	10	10	10	300	300	-	0.04	10	
	-	0,15	15	20	20	600	600	-	0.04	20	
	-	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I _{QL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I _{QH} ^{MIN.}	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage: High-Level, V _{QH} Min.	-	0,5	5	4.95				4.95	5	-	V
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage V _{IL} Max.	0.5,4.5	-	5	1.5				-	-	1.5	V
	1,9	-	10	3				-	-	3	
	1.5,13.5	-	15	4				-	-	4	
Input High Voltage, V _{IH} Min.	0.5,4.5	-	5	3.5				3.5	-	-	V
	1,9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current I _{IN} Max.	-	0,18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	MA

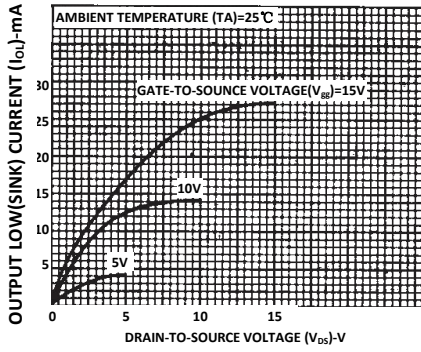


Fig. 2 Typical output low (sink) current characteristics.

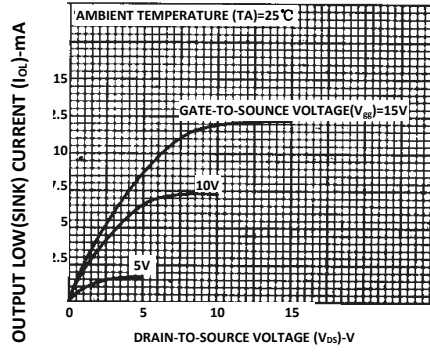


Fig. 3 Minimum output low (sink) current characteristics.

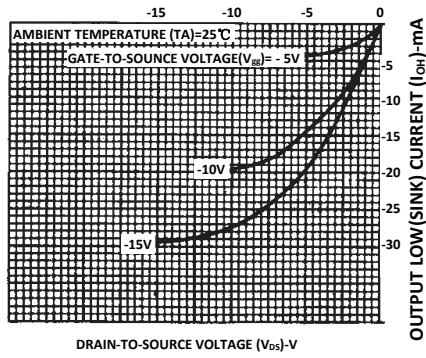


Fig. 4 Typical output low (source) current characteristics.

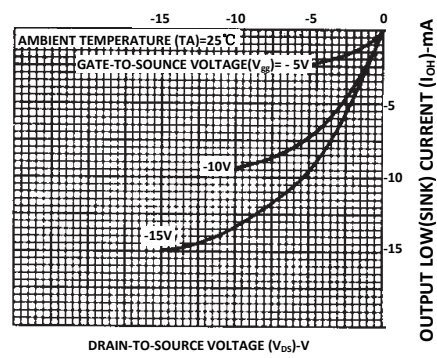


Fig. 5 Minimum output low (source) current characteristics.

6.4. DYNAMIC ELECTRICAL CHARACTERISTICS at TA=25°C, Input $t_r, t_f=20$ ns, $C_L=50$ pF, $R_L=200$ K Ω

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		V _{DD} (V)	Min.	Typ.		Max.
Propagation Delay Time, t_{PLH}, t_{PHL}		5	-	160	320	ns
		10		80	160	
		15		60	120	
Transition Time, $t_{THL} - t_{TLH}$		5	-	100	200	ns
		10		50	100	
		15		40	80	
Maximum Clock Input Frequency, f_{CL}		5	3	6	-	MHz
		10	6	12		
		15	8.5	17		
Minimum Clock Pulse Width, t_w		5	-	90	180	ns
		10		40	80	
		15		25	50	
Clock Rise and Fall Time, t_{rCL}, t_{fCL} ^[1]		5	-	-	15	μ s
		10			15	
		15			15	
Minimum Set-up Time, t_s : Serial Input (ref. to CL)		5	-	60	120	ns
		10	-	40	80	
		15	-	30	60	
Parallel Inputs XL4021B (ref. to P/S)		5	-	25	50	ns
		10	-	15	30	
		15	-	10	20	
Minimum Hold Time, t_H : Serial In, Parallel In, Parallel/Serial Control		5	-	-	0	ns
		10	-	-	0	
		15	-	-	0	
Minimum P/S Pulse Width, t_{WH} (XL4021B)		5	-	80	160	ns
		10	-	40	80	
		15	-	25	50	
Minimum P/S Removal Time, t_{REM} XL4021B (ref. to CL)		5	-	140	280	ns
		10	-	70	140	
		15	-	50	100	
Average Input Capacitance, C_I	Any Input		-	5	7.5	pF

[2] If more than one unit is cascaded t_{rCL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

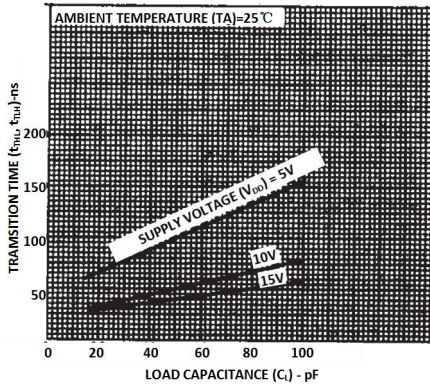


Fig.6 Typical transition time as a function of load capacitance.

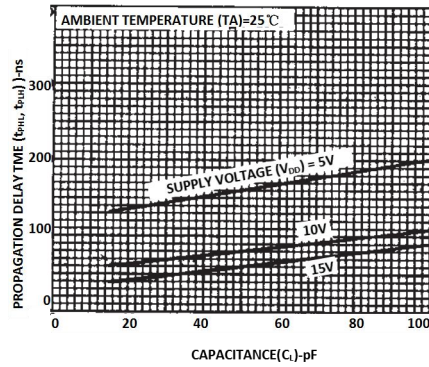


Fig. 7 Typical propagation delay time as a function of load capacitance.

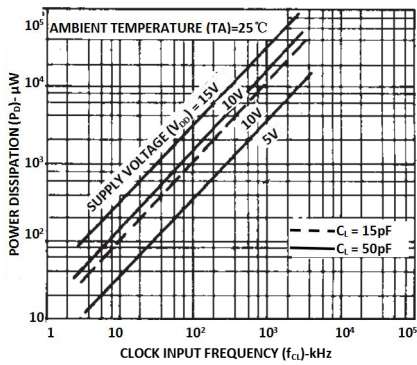


Fig.8 Typical dynamic power dissipation as a function of dock input frequency.

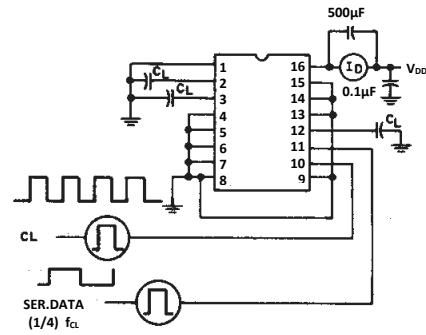


Fig.9 Dynamic power dissipation test circuit.

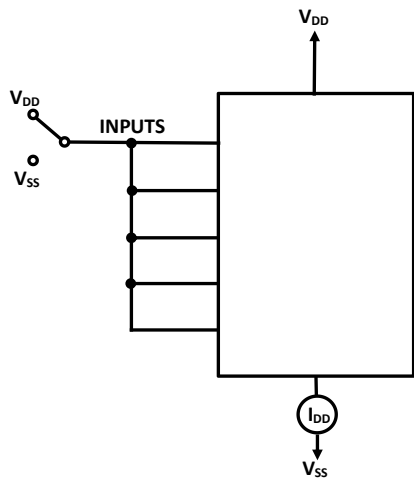


Fig. 10 Quiescent device current test circuit.

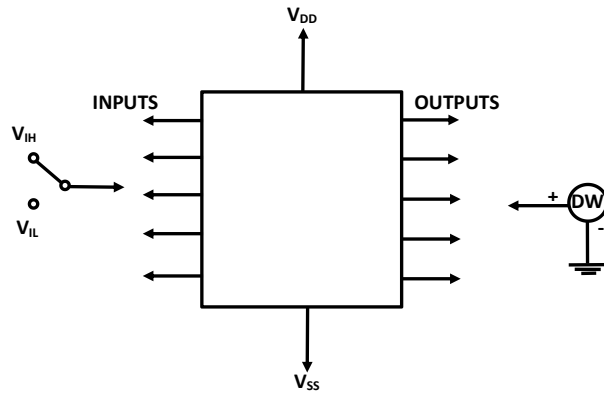
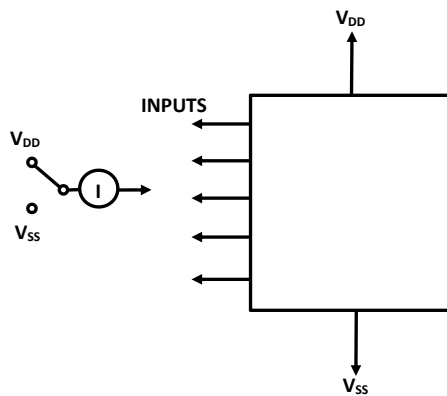


Fig. 11 Input voltage test circuit.



NOTE:
MEASURE INPUTS SEQUENTIALLY,
TO BOTH V_{DD} AND V_{SS} CONNECT
ALL UNUSED INPUTS TO EITHER
 V_{DD} OR V_{SS}

Fig. 12 Input current test circuit.

7. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL4021B	XL4021B	SOP16	10.00 * 3.95	-40 to +85	MSL3	T & R	2500

8. DIMENSIONAL DRAWINGS

SOP16

Mark	Size	Min (mm)	Max (mm)	Mark	Size	Min (mm)	Max (mm)
A		9.80	10.00	C4		0.203	0.233
A1		0.356	0.456	D		1.05TYP	
A2		1.27TYP		D1		0.40	0.70
A3		0.302TYP		D2		0.15	0.25
B		3.85	3.95	R1		0.20TYP	
B1		5.84	6.24	R2		0.20TYP	
B2		5.00TYP		θ 1		8° ~ 12° TYP4	
C		1.40	1.60	θ 2		8° ~ 12° TYP4	
C1		0.61	0.71	θ 3		0° ~ 8°	
C2		0.54	0.64	θ 4		4° ~ 12°	
C3		0.05	0.25				

