Six ininverter **CD4069**

An Overview of the

CD4069 is composed of six CMOS inverter circuits which are mainly used as a general purpose inverter, i. e. for unnecessary medium power TTL

In a circuit for drive and logical level conversion.

CD4069 provides 14 lead multilayer ceramic double line (D), Lead-out end arrangement (top view)

Molded ceramic J, plastic P, and ceramic sheet carrier

(C) 4 forms of packaging.

Recommended working conditions:

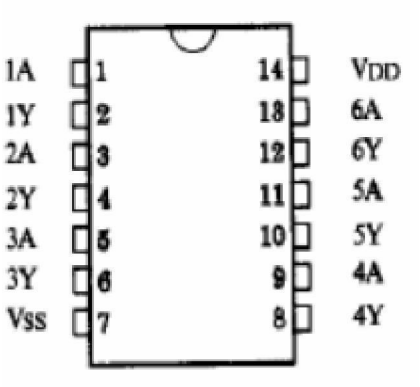
Power supply voltage range ... V~15V

Input voltage range ...0V~VDD

Operating temperature range

Class M ...····· - 55℃ ~ 125℃

Class E ...····· - 40℃ ~ 85℃



Limit value:

Power supply voltage ... -0.5V~18V

Input voltage ... -

0.5V~VDD+0.5V Input

current ...·····± 10mA

Storage temperature ... - 65℃ ~ 150℃

Lead-end symbol:

1A~6A	Data input terminal
VDD	Power supply
Vss	Ground
1Y~6Y	Data input terminal

Logical expression: $\overline{Y}$ A

Static properties:

Parameters	Test conditions			Specification value			Unit:
	Vo/V	Vi/V	VDD/V	-40℃	25℃	85℃	
Low V oL output Level voltage (Max.)	-	5/0 10/0 15/0	5.0 10.0 15.0	0.05			V
The Vo H output is high Level voltage (Min.)	-	5/0 10/0 15/0	5.0 10.0 15.0	4.95 9.95 14.95			V
V IL input of low-level voltage (Max.)	4.5 9.0 13.5	-	5.0 10.0 15.0	1.0 2.0 2.5			V
V IH Input a high-level voltage (Min.)	0.1 1.0 1.5	-	5.0 10.0 15.0	4.0 8.0 12.5			V
Output, high-level current, I O H (Min.)	2.5 4.6 9.5 13.5	5/0 5/0 10/0 15/0	5.0 5.0 10.0 15.0	-1.8 -0.61 -1.5 -4.0	-1.6 -0.51 -1.3 -3.4	-1.3 -0.42 -1.1 -2.8	mA
Output low level Current: I O L (Min.)	0.4 0.5 1.5	5/0 10/0 15/0	5.0 10.0 15.0	0.64 1.6 4.2	0.61 1.5 4.0	0.42 1.1 2.8	mA
I I input current	-	15/0	15.0	±0.1		±1.0	uA
I DD Power current (Max.)	-	5/0 10/0 15/0	5.0 10.0 15.0	0.25 0.5 1.0	0.25 0.5 1.0	7.5 15.0 30.0	uA

Dynamic Features:

Parameters	Test conditions	V DD /V	Specification value		Unit:
			Minimum:	Maximum:	
t PLH output transmission from low level to high level transmission delay time	CL=50pF RL=200kΩ tr=20ns tf=20ns	5.0 10.0 15.0	--	110 60 50	ns
t PHL output from high level to low level transmission delay time		5.0 10.0 15.0	--	110 60 50	
tTLH output transmission from low level to high level conversion time		5.0 10.0 15.0	--	200 100 80	
t THL output from high level to low level conversion time		5.0 10.0 15.0	--	200 100 80	
CI input capacitor (Either input side)		--	--	15	Pf

Logic diagram: