Four-door and non-gate trigger

summary

CD4093 is composed of four Schmidt trigger circuits, each having a 2-input and non-gate with a Schmidt trigger function at both inputs, each opening, closing at different points of the signal rise, down line, and up voltage (V_P)And drop voltage(V_N)The difference is defined as a lag voltage (Δ V T)

All outputs have symmetrical irrigation current capability to B series output drive standards

Main features:

☆ power supply range wide: 3V~15V

☆ has a Schmidt trigger for each input oscillator

☆ has a strong anti-interference capability

☆ symmetric irrigation current capacity

☆ rise down down time unlimited

☆ B-Series Output Drive Standard

Application scope:

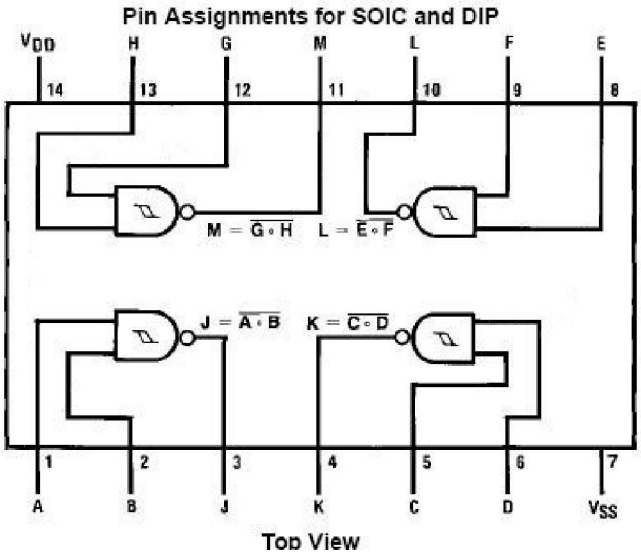
Waveform and pulse shaping

Single-stable multi-frequency

High environmental noise system

Unsteady multiharmonic oscillator

Pipe et arrangement diagram:



CD4093 pin function:

A	Data input terminal	E	Data input terminal	J	Data Output End
B	Data input terminal	F	Data input terminal	K	Data Output End
C	Data input terminal	G	Data input terminal	L	Data Output End
D	Data input terminal	H	Data input terminal	M	Data Output End
VDD	Positive power supply	VSS	Ground	-	-

Limit parameters

DC Supply Voltage DC power supply voltage (VDD)	-0.5 to + 18 VDC
Input Voltage Input voltage (VIN)	-0.5 to VDD + 0.5 VDC
Storage Temperature Range storage temperature range (TS)	-65 ℃ to + 150 ℃
Power Dissipation Power Consumption (PD)	
Dual-In-Line Common Double-column Package	700 mW
Sm a l l O u tl i ne Small shape	500 mW

Recommended working conditions

DC Supply Voltage DC power supply voltage (VDD)	3 to 15 VDC
Input Voltage Input voltage (VIN)	0 to VDD VDC
Operating Temperature Range Operating	0 ℃ to + 70 ℃

DC electric gas characteristics

Symbol	Parameters	Conditions	+25℃			Unit:
			Minimum:	Typical:	Maximum:	
IDD	Static current	VDD = 5V			1.0	μA
		VDD = 10V			2.0	
		VDD = 15V			4.0	
VOL	Output a low-level voltage	VIN = VDD, | IO | <1 μA				
		VDD = 5V		0	0.05	V
		VDD = 10V		0	0.05	
		VDD = 15V		0	0.05	
VOH	Output a high-	VIN = VSS, | IO | <1 μA				
		VDD = 5V	4.95	5		V

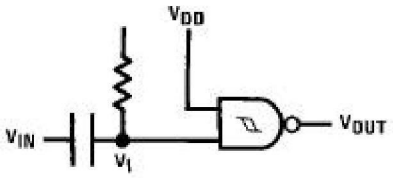
		VDD = 15V	14.95	15		
VT-	Negative threshold voltage (any input)	| IO | <1 μA				
		VDD =5V, VO =4.5V	1.5	1.7	2.25	V
		VDD=10V, VO = 9V	3.0	3.7	4.5	
		VDD =15V, VO =13.5V	4.5	5.6	6.75	
VT +	Forward threshold voltage (any input)	| IO | <1 μA				
		VDD = 5V, VO = 0.5V	2.75	3.4	3.5	V
		VDD = 10V, VO = 1V	5.5	6.5	7.0	
		VDD = 15V, VO = 1.5V	8.25	9.4	10.5	
VH	VT + -VT-) (any Input in.)	VDD = 5V	0.5	1.7	2.0	V
		VDD = 10V	1.0	2.8	4.0	
		VDD = 15V	1.5	3.8	6.0	
IOL	Output Low-level current	VIN = VDD				
		VDD =5V, VO =0.4V	0.44	0.88		mA
		VDD=10V, VO=0.5V	1.1	2.25		
		VDD=15V, VO =1.5V	3.0	8.8		
IOH	Output a high-level current	VIN = VSS				
		VDD =5V, VO =4.6V	0.44	-0.88		mA
		VDD =10V, VO=9.5V	-1.1	-2.25		
		VDD =15V, VO =13.5V	-3.0	-8.8		
IIN	Input-in current	VDD=15V, VIN = 0V		-10^{-5}	-0.3	μA

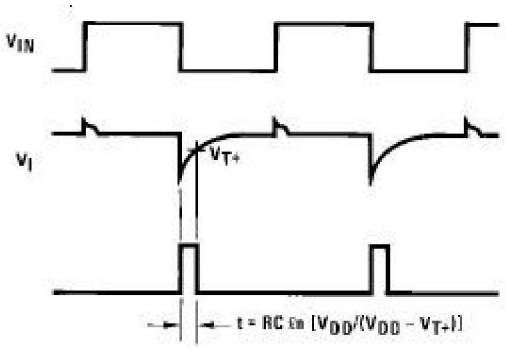
AC electrical characteristics

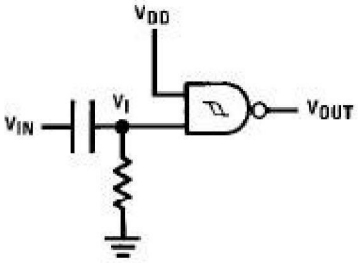
Symbol	Parameters	Conditions condition	Minimum:	Typical:	Maximum:	Unit:
tPHL tPLH	Propagation Delay Time Delivery Delay Time	VDD = 5V		300	450	ns
		VDD = 10V		120	210	
		VDD = 15V		80	160	
tTHL tTLH	Transition Time transition time	VDD = 5V		90	145	ns
		VDD = 10V		50	75	
		VDD = 15V		40	60	
CIN	Input Capacitance input capacitor	(Any Input)		5.0	7.5	pF

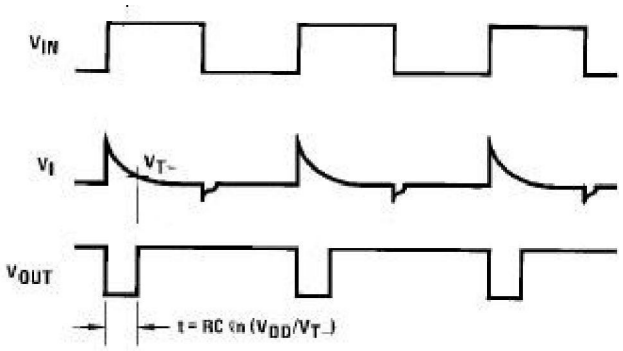
CPD	Power Dissipation Capacitance dissipative capacitor	(Per Gate)		24		pF

Typical application circuits:

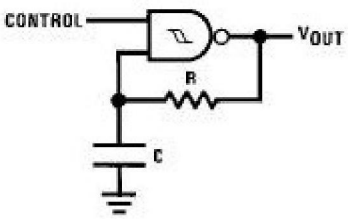








Gated Oscillator



Assume $t_1 + t_2 >> t_{PHL} + t_{PLH}$ then:

$t_0 = RC\ \ell n\ [V_{DD}/V_{T-}]$

$t_1 = RC\ \ell n\ [(V_{DD} - V_{T-})/(V_{DD} - V_{T+})]$

$t_2 = RC\ \ell n\ [V_{T^+}/V_{T^-}]$

$$f = \frac{1}{t_1 + t_2} = \frac{1}{RC\ \ell n \frac{(V_T^+)(V_{DD} - V_T^-)}{(V_T^-)(V_{DD} - V_T^+)}}$$