programmable timer

1. An Overview

CD 4541B The programmable timer is composed of a 16-bit binary counter, a built-in oscillator (with an external capacitor and two resistors), an output control logic, and a special power-up reset circuit.

The particularity of the power reset circuit lies in: 1. There is no additional static current consumption; 2. This power reset function is valid in the entire voltage range (3~15V), whether allowed or prohibited.

If the power reset function is allowed, the internal timer and counter initialize when the power is on. The external reset pulse can also be initialized with the timer and counter when the power is already on. When the reset action is complete, the frequency of the built-in oscillator is determined by the external RC constant. The 16-bit counter divides the frequency of the oscillator with the value of any 4-digit binary number.

2. Features

Order Available by frequency: 2^8, 2^{10}, 2^{13}Or 2^{16}。

Make the counter add one on the positive edge of the clock transition.

Keep the built-in low-power RC oscillator (± 2% over the entire temperature range in a frequency range of less than 10kHz

Precision, maintaining ± 10% accuracy and ± 3% process deviation accuracy in the entire operating power supply voltage range).

Order oscillator frequency range: DC ~ 100 kHz.

Make the internal oscillator bypass when the external clock is used.

After the power supply increases, automatically reset and initialize all the counters.

Make the external master reset completely independent of the automatic reset operation.

Order can be used as a 2^nFrequency divider or a single timer.

To flexibly change the output logic level by selecting Q / Q.

Order reset (automatic or master reset) places the oscillator in a forbidden state during the reset period, reducing the dynamic power consumption during this period.

Althe clock adjustment circuit to operate with extremely slow clock rise and down time.

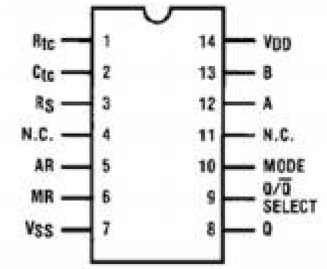
Wide power supply voltage range: 3.0~15V.

Order 5V10V15V three gear parameter.

Make high noise tolerance-0.45 VDD (tape p).

The maximum input leakage current is 1 μA over the entire temperature range of 15V.

3. Pipe pin diagram



4. Truth value table

Pipe foot number	state	
	0	1
5	Automatic reset operation	Prohibit the automatic reset
6	Timer operation	master reset
9	After the reset, the output initial value is a low level	After the reset, the output initial value is a high level
10	Single cycle mode	Circulating mode

5. Frequency division meter

A	B	The N th counter level of the data	2N value
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

6. Working characteristics

When the automatic reset pin is set to ″0″, the counter circuit is initiated. Or when the power supply is switched on

When the main reset pin is set to ″1″ in time. Both reset all counters simultaneously, regardless of the original state of the counter.

Make the RC oscillator frequency determined by the external RC constant:

F = 1 / (2.3RtcCtc) (frequency within 1kHz f 100 kHz)

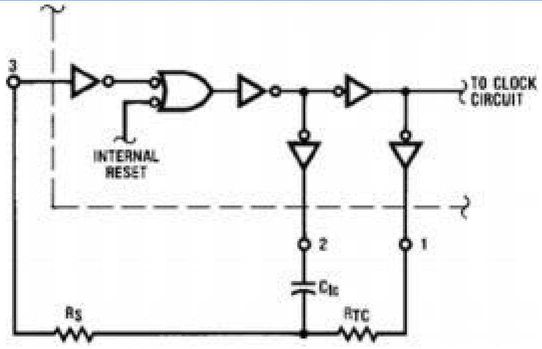
The selected value of Rs is Rs = 2 Rtc (Rs 10k Ω)

Order the timing selection input (A and B) to provide A two-bit address to select the output of four count levels (2^8、2^{10}、2^{13}Or 2^{16}) Any one of them. And 2 in the frequency division table^{n}Counts represent the Q output of the N level of the counter. When A is ″1″ and B is ″1″, 2 will be selected^{16}. When A is ″1″ and B is ″0″, the normal count is interrupted and the level 9 of the counter jumps the previous level 8 counter to receive the clock directly from the oscillator (effective count is 2^8output).

Make the Q / Q pins used to select the output level. When the counter is in the reset state, Q / Q selects the pin to ″0″, then Q output is ″0″; Q / Q selects the pin to ″1″, then Q output is ″1″.

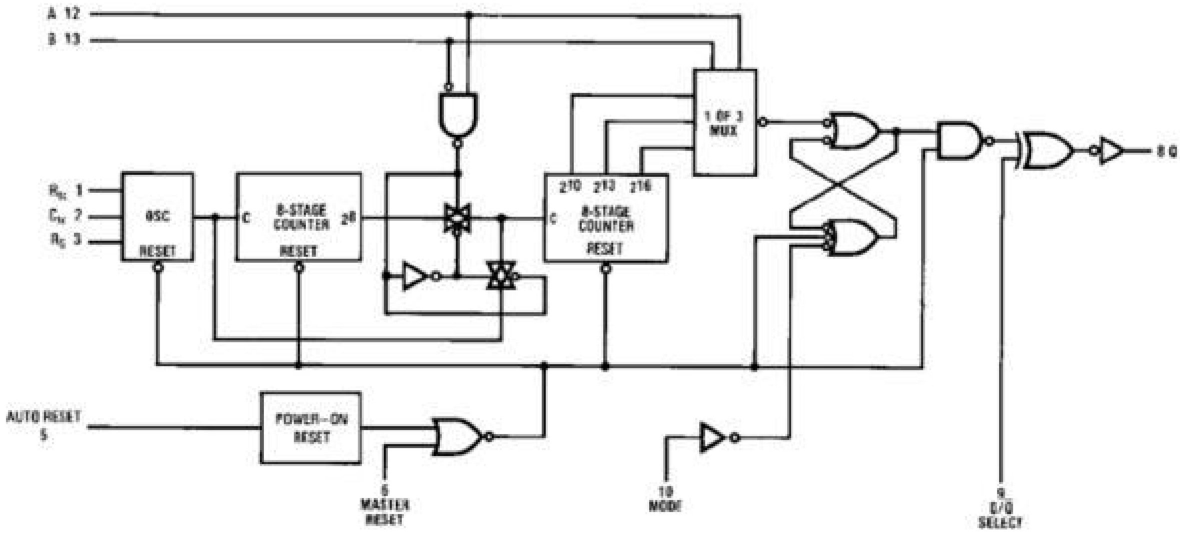
When the mode control pin (Pin 10) is set to ″1″, the selected count value is continuously transmitted to the output. When the mode control

The pipe pin is set to ″0″, and after the reset state, the RS trigger reset (see logical block diagram), the start row count, count to 2^{n1}Later, the RS trigger is positioned and causes a change in the output state. Therefore, each count over 2^{n1}After the number, you change the state of the output once. Therefore, a master reset pulse must be applied or the level of the mode control pin changed to reset the single-cycle operation.



Oscillator circuit uses a RC configuration diagram

7. Logical block diagram



8. Limit parameters

symbol	parameter	condition	numeric value	unit
V DD	Power voltage range		-0.5~+18	V
V IN	input voltage range		-0.5~VDD +0.5	V
T stg	Package work, temperature range		-65~150	℃
P D	Maximum power dissipation	DI P	700	m W
		C OB	500	
T L	Point welding temperature		260	℃

9. Recommended working conditions

symbol	parameter	condition	numeric value	unit
VD D	Power voltage range		3~15	V
VI N	input voltage range		0~VDD	V
	operating temperature range		-40~85	℃

remarks:

The working condition of the limit parameter exceeds the range to ensure the normal operation of the device. Devices can not be guaranteed under the limiting parameters

job security. Users are advised to use the device according to the working conditions recommended in the electrical parameter table.

Order Unless otherwise specified, VSS = 0 V.

10., and the electrical parameters

(Reference Voltage: Vss)

parameter	symbol	condition	V DD	-40℃		25℃			+85℃		unit
				minimum	maximum	minimum	typical case	maximum	minimum	maximum	
quiescent current	IDD	VIN = either VDD or VSS	5.0		20		0.005	20		150	μA
		VIN = either VDD or VSS	10		40		0.010	40		300	
		VIN = either VDD or VSS	15		80		0.015	80		600	
Output low power flat	V OL		5.0		0.05		0	0.05		0.05	V
		IO <1uA	10		0.05		0	0.05		0.05	
			15		0.05		0	0.05		0.05	
Output high electricity flat	V OH		5.0	4.95		4.95	5		4.95		V
		IO <1uA	10	9.95		9.95	10		9.95		
			15	14.95		14.95	15		14.95		
Input low power flat	V OL	.5VO = 4 or 0.5V	5.0		1.5		2	1.5		1.5	V
		.0VO = 9 or 1.0V	10		3.0		4	3.0		3.0	
		VO = 13.5 or 1.5V	15		4.0		6	4.0		4.0	
Enter high power flat	V OH	.5VO = 4 or 0.5V	5.0	3.5		3.5	3		3.5		V
		.0VO = 9 or 1.0V	10	7.0		7.0	6		7.0		
		VO = 13.5 or 1.5V	15	11		11	9		11		
Low level loss The current	IOL	VOL =0.4	5.0	1.70		1.30	2.0		1.10		mA
		VOL =0.5V	10	2.40		2.20	5.0		2.00		
		VOL =1.5V	15	9.70		8.50	15.0		6.50		
High level loss The current	IOH	VOH =2.5V	5.0	5.1		3.20	6.80		2.90		mA
		VOH =9.5V	10	3.80		3.50	5.80		2.85		
		VOH =13.5V	15	8.5		7.0	16.0		6.22		
		VIN =0V	15		-0.3		-10^{-5}	-0.3		-1.0	

input currenton	IIN	VIN =15V	15		3.0		10^{-5}	0.3		1.0	μA

*: IOH and IOL are results by testing one output.

11. Dynamic electrical parameters

(TA =25℃)

symbol	project	condition	V DD	least value	representative value	crest value	unit
tTLH	Output rise time		5V		50	200	n s
			10V		30	100	
			15V		25	80	
tTHL	Output drop time		5V		50	200	n s
			10V		30	100	
			15V		25	80	
t PLH t PHL	propagation delay time	Power off, on transmission delay from clock to Q	5V		1.8	4.0	n s
			10V		0.6	1.5	
			15V		0.4	1.0	
t PHL t PLH	propagation delay time	Transmission delay of power on and off, from clock to Q	5V		3.2	8.0	n s
			10V		1.5	3.0	
			15V		1.0	2.0	
t WH	clock-pulse width		5V	400	200		n s
			10V	200	100		
			15V	150	70		
tcl	clock frequency		5V		2.5	1.0	M Hz
			10V		6.0	3.0	
			15V		8.5	4.0	
t WH	MR pulse length		5V	400	170		n s
			10V	200	75		
			15V	150	50		
C I	Average input capacitor	Any input			5.0	7.5	pF
CPD	Power supply power consumption capacitance				100		pF

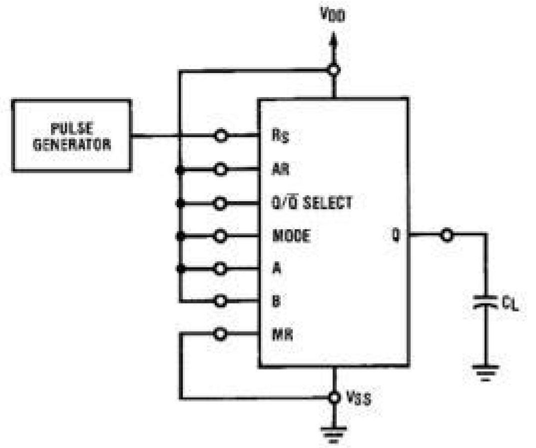
remarks:

1. The AC parameters are guaranteed by the relevant DC parameters.

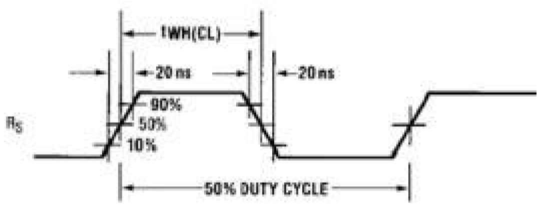
2. CPD represents the dynamic power consumption of each CMO S device with no load.

12. Test circuit and waveform graph

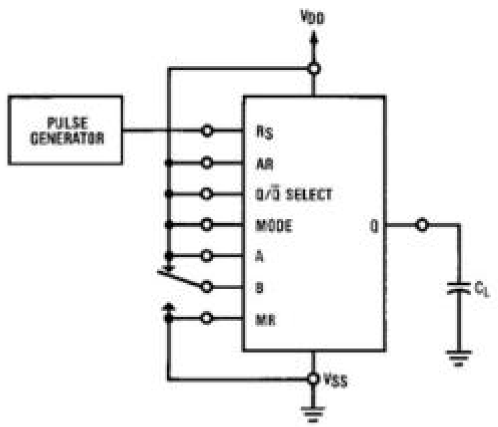
Make the power consumption test circuit and waveform diagram

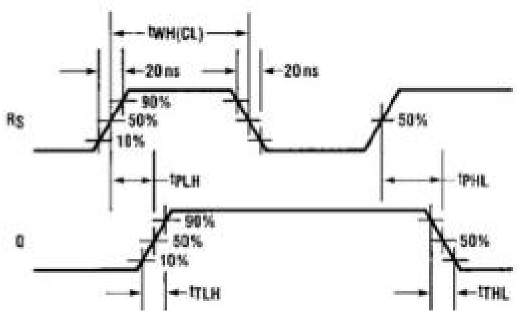


(R_{tc} and C_{tc} outputs are left open)



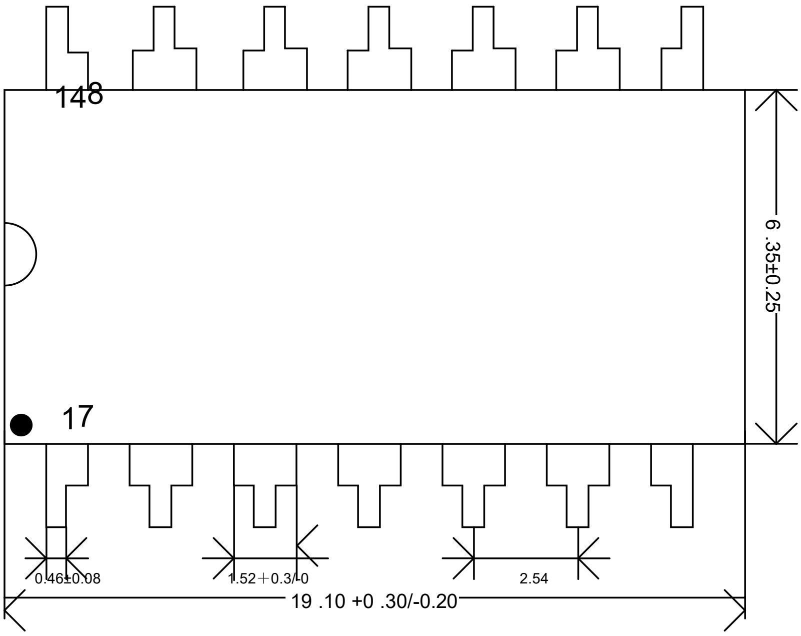
Make the switch time test circuit and the waveform diagram





13. Package size diagram

Make the DIP 14 package form



Make the SOP 14 package form