Dual Channel High Side Switch with Diagnosis and Embedded Protection

Descriptions

The CPSQ54D20 is a dual-channel 20mΩ intelligent high-side switch, integrating comprehensive protection functions and diagnostic capabilities. It is widely used in 12V automotive load systems.

The CPSQ54D20 can not only drive resistive loads, but also has the function of clamping VDS when inductive loads shut down, and the Capacitive Load Switching mode can also drive capacitive loads.

The CPSQ54D20 features multiple protection mechanisms, including overcurrent and short-circuit protection with an intelligent restart mechanism, voltage clamp during inductive load shutdown, and absolute and dynamic over-temperature protection, which effectively safeguard loads and enhance system stability during fault conditions.

The CPSQ54D20 provides diagnostic functions enabling high-precision output current detection and fault signal feedback during fault conditions.

The CPSQ54D20 is available in 4.9mm x 6.1mm SSOP-14 package. Standard product is Pb-Free and Halogen-Free.

Features

- AEC-Q100 Grade-1 Qualified for Automotive Applications
- Capacitive Load Switching Mode
- Proportional load Current Sense
- Open Load in ON and OFF state
- Short Circuit Protection with Intelligent Restart
- Absolute and Dynamic Temperature Protection with Restart Control
- Overcurrent Protection with Intelligent Restart
- Voltage Clamp during Inductive Load Shutdown
- RoHS compliant, Pb-Free and Halogen-Free

Applications

- Replaces electromechanical relays, fuses and discrete circuits
- Protection of system supply
- Main switch for ECU power supply
- Suitable for driving resistive, inductive and capacitive loads
- Suitable for driving heating elements
- Suitable for driving ADAS & AD modules, e.g. cameras, radar, ultrasonic, and LIDAR modules
- Suitable for driving sub modules, e.g. displays

Contents

Revision History

Version	Date	Description
0.1	2024-11	Initial release
0.2	2025-02	Correct some words typographical errors
0.3	2025-03	Update Electrical Characteristics
0.4	2025-04	Fix some typo
0.5	2025-08	Update Electrical Characteristics

1. Features and Applications

1.1 General Descriptions

The CPSQ54D20 is an automotive dual channel high side switch driver. It features 3V/5V CMOS compatible input control interface and two high power output channel. The CPSQ54D20 is extensively used in 12V automotive power supply systems.

The CPSQ54D20 features multiple protection mechanisms, including overcurrent and short-circuit protection with an intelligent restart mechanism, voltage clamp during inductive load shutdown, and absolute and dynamic over-temperature protection, which effectively safeguard loads and enhance system stability during fault conditions.

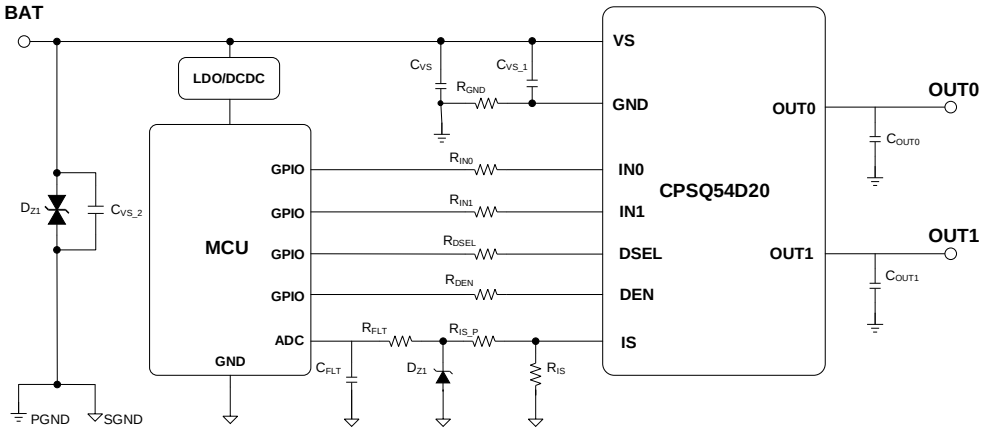


Figure 1. Typical Application

1.2 Block Diagram

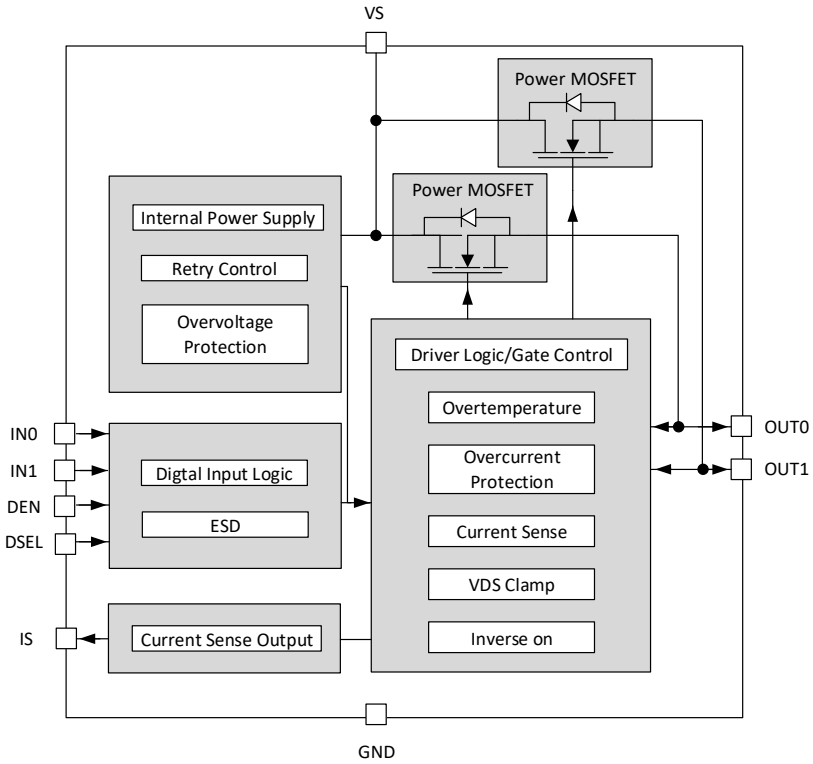
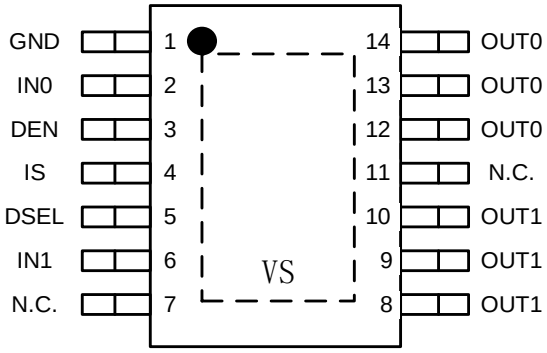


Figure 2. Block Diagram

1.3 Pin-out and Descriptions



SSOP 14pin

Bottom Exposed PAD(Top View)

Figure 3. CPSQ54D20 Pin Map

Table 1 Pin Description

Pin #	Name	Function
EP	VS(exposed pad)	Battery voltage
1	GND	Ground connection for the internal logic
2	IN0	Digital signal to switch ON channel0 ("high" active) If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
3	DEN	Digital signal to enable device diagnosis ("high" active) and to clear the protection counter If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
4	IS	Analog/digital signal for diagnosis If not used: Left open
5	DSEL	Digital signal to toggle between the channels. If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
6	IN1	Digital signal to switch ON channel1 ("high" active) If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
7,11	N.C.	Not connected, internally not bonded
8-10	OUT1	Protected high-side power output channel1 (1)
12-14	OUT0	Protected high-side power output channel0 (1)

(1). All output pins of the channel must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

2. Operation Conditions

2.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

PARAMETER		MIN	MAX	UNIT	CONDITION
Power supply voltage	V_S	-0.3	28	V	
Load dump voltage	$V_{BAT(LD)}$		35	V	Suppressed load dump acc. to ISO16750-2(2010).
Supply voltage for short circuit protection	$V_{BAT(SC)}$	0	24	V	Acc. to AEC- Q100-012
Current through GND pin	I_{GND}	-50	50	mA	
Current through DI pin	I_{DI}	-1	2	mA	
Voltage at IS pin(2)	V_{IS}	-1.5	V_S	V	I_{IS} = 10 µA
Current through IS Pin	I_{IS}	-25	$I_{IS(SAT,MAX)}$	mA	
Junction temperature	T_J	-40	150	°C	
Storage temperature	T_{STG}	–55	155	°C	
Maximum energy dissipation - single pulse	E_{AS}		37	mJ	$I_L = 2 \cdot I_{L(NOM)}$
Load current	I_L		$I_{L(OVL),MAX}$	A	

These are the stress ratings only. Stresses that exceeds the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at these or any other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

2.2 ESD Ratings

Table 3 ESD Information

PARAMETER		VALUE	UNIT
ESD Susceptibility all pins (HBM)	Human Body Model, per AEC Q100-002(1)	±2000	V
ESD Susceptibility OUT vs GND and VS connected (HBM)		±4000	
ESD Susceptibility all pins (CDM)	Charged Device Model, per AEC Q100-011	±500	
ESD Susceptibility corner pins (CDM) - (pins 1, 7, 8, 14)		±750	

2.3 Recommended Operating Conditions

Table 4 Recommended operation range

PARAMETER		MIN	TYP	MAX	UNIT
Supply voltage range for normal operation	$V_{S(NOR)}$	6	13.5	18	V
Lower extended supply voltage range for operation (normal)	$V_{S(EXT,LOW)}$	3.1		6	V
Upper extended supply voltage range for operation	$V_{S(EXT,UP)}$	18		28	V
Junction temperature	T_J	-40		150	℃

2.4 Thermal Information

PARAMETER		MIN	TYP	MAX	UNIT
Thermal characterization parameter junction-top	Ψ_{JTOP}		1.7	2.9	°C/W
Thermal resistance junction-to-ambient	R_{thJA}		30.9		°C/W

3. Electrical Characteristics

V_S = 6V to 18V, T_j= -40°C to 150°C; Typical values stated at T_j= 25°C and V_S = 13.5V, Digital input (DI) pins = IN, DEN, DSEL; R_L = 4.7Ω.unless otherwise specified.

Description	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DI pins						
Digital input voltage threshold	$V_{DI(TH)}$		1		2.1	V
Digital input clamping voltage	$V_{DI(CLAMP1)}$	I_{DI} = 100uA		**7**		V
Digital input clamping voltage	$V_{DI(CLAMP2)}$	I_{DI} = 400uA	7.5	8	8.7	V
Digital input hysteresis	$V_{DI(HYS)}$			0.25		V
Digital input current ("high")	$I_{DI(H)}$	V_{DI} = 2V	2	10	25	µA
Digital input current ("low")	$I_{DI(L)}$	V_{DI} = 0.8V	2	2.5	6	µA
VS pins						
Power supply undervoltage shutdown	$V_{S(UV)}$	V_S decreasing INx = “high” From 0 ≤V_{DS} ≤ 0.5V to V_{DS} ~V_S	2.3	2.75	3.1	V
Power supply minimum operating voltage	$V_{S(OP)}$	V_S increasing INx = “high” From V_{DS} ~V_S to 0 ≤V_{DS} ≤ 0.5V	3.0	3.5	4.1	V
Power supply undervoltage shutdown hysteresis	$V_{S(HYS)}$	$V_{S(OP)}$ - $V_{S(UV)}$		0.9		V
Breakdown voltage between GND and VS pins in reverse battery	-$V_{S(REV)}$	$I_{GND(REV)}$ = 7mA T_J = 150°C	16		30	V
Power supply current consumption in sleep mode with loads at TJ ≤ 85°C	$I_{VS(SLEEP)\_85}$	V_S = 20V V_{OUT} = 0V INx = DEN = DSEL = “low” T_J ≤ 85°C		0.03	0.5	µA
Power supply current consumption in sleep mode with loads at TJ = 150°C	$I_{VS(SLEEP)\_150}$			3.5	14	µA
Operating current in active with diagnosis mode	$I_{GND(ACTIVE)}$			3.7	6	mA
Operating current in inactive with diagnosis mode	$I_{GND(INACTIVE)}$			2.5	4.4	mA

Electrical Characteristic (continued)

V_S = 6V to 18V, T_j= -40°C to 150°C; Typical values stated at T_j= 25°C and V_S = 13.5V, Digital input (DI) pins = IN, DEN, DSEL; R_L = 4.7Ω.unless otherwise specified.

Description	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage						
Drain to source clamping voltage at T_J = -40°C	$V_{DS(CLAMP)\_-40}$	I_L = 5mA T_J = -40°C	33	36.5	42	V
Drain to source clamping voltage at $T_J \geq$ 25°C	$V_{DS(CLAMP)\_25}$	I_L = 5mA $T_J \geq$ 25°C	35	38	44	V
Switch-ON delay	$t_{ON(DELAY)}$	V_S = 13.5V V_{OUT} = 10%V_S	10	70	130	µs
Switch-OFF delay	$t_{OFF(DELAY)}$	V_S = 13.5V V_{OUT} = 90%V_S	10	50	160	µs
Switch-ON time	t_{ON}	V_S = 13.5V V_{OUT} = 90%V_S	90	110	120	µs
Switch-OFF time	t_{OFF}	V_S = 13.5V V_{OUT} = 10%V_S	70	85	100	µs
CLS activation delay	$t_{ON\_CLS(DELAY)}$	V_S = 13.5V	10	70	200	µs
CLS de-activation delay	$t_{OFF\_CLS(DELAY)}$	V_S = 13.5V	20	60	120	µs
Switch-ON/OFF Matching t_{ON} -t_{OFF}	Δt_{SW}	V_S = 13.5V	-60	25	90	µs
Switch-ON slew rate	$(dV/dt)_{ON}$	V_S = 13.5V V_{OUT} = 30% to 70% *VS*	0.3	0.6	0.9	V/µs
Switch-OFF slew rate	$-(dV/dt)_{OFF}$	V_S = 13.5V V_{OUT} = 30% to 70% *VS*	0.3	0.6	0.9	V/µs
Slew rate matching (d*V*/d*t*)ON + (d*V*/d*t*)OFF	$\Delta(dV/dt)_{SW}$	V_S = 13.5V	-0.15	0	0.15	V/µs
Input frequency for capacitive load switching mode activation	$f_{VIN(CLS)}$	$DC_{VIN(CLS)}$ = 50%	22	30	38	kHz
Duty cycle for capacitive load switching mode activation	$DC_{VIN(CLS)}$	$f_{VIN(CLS)}$ = 30kHz	30%	50%	70%	
Maximum time in CLS mode	t_{CLS1}				12	s
ON-state resistance at T_J = 25°C	$R_{DS(ON)\_25}$	T_J = 25°C		19		mΩ
ON-state resistance at T_J = 150°C	$R_{DS(ON)\_150}$	T_J = 150°C I_L = 2A			36	mΩ
ON-state resistance in cranking at T_J = 150°C	$R_{DS(ON)\_CRANK\_150}$	T_J = 150°C V_S = 3.1V I_L = 1A			45	mΩ

Electrical Characteristic (continued)

V_S = 6V to 18V, T_j= -40°C to 150°C; Typical values stated at T_j= 25°C and V_S = 13.5V, Digital input (DI) pins = IN, DEN, DSEL; R_L = 4.7Ω.unless otherwise specified.

Description	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON-state resistance in inverse current at T_J = 25°C	$R_{DS(INV)\_25}$	T_J = 25 °C V_S = 13.5V I_L = -4A DEN = “low”		21		mΩ
ON-state resistance in inverse current at T_J = 150°C	$R_{DS(INV)\_150}$	T_J = 25 °C V_S = -13.5V I_L = -4 A R_{SENSE} = 1.2kΩ			45	mΩ
Nominal load current per channel (all channels active) at T_A = 85°C	$I_{L(NOM)\_85}$	T_A = 85°C T_J ≤ 150°C		5		A
Output leakage current at T_J ≤ 85°C	$I_{L(OFF)\_85}$	V_{OUT} = 0V INx = "low" T_A ≤ 85°C			4.5	µA
Inverse current capability	$I_{L(INV)}$	V_S < V_{OUT} INx = "high"		5		A
Drain source diode voltage	$V_{DS(DIODE)}$	I_L = -190mA T_J = 150°C		550	700	mV
Switch-ON energy	E_{ON}	V_S = 18V		0.4		mJ
Switch-OFF energy	E_{OFF}	V_S = 18V		0.5		mJ
Protection						
Thermal shutdown temperature (absolute)	$T_{J(ABS)}$		150	175	200	°C
Thermal shutdown hysteresis (absolute)	$T_{HYS(ABS)}$			30		°C
Thermal shutdown temperature (dynamic)	$T_{J(DYN)}$			80		°C
Thermal shutdown temperature (dynamic) in capacitive load switching mode	$T_{J(DYN)\_CLS}$			40		°C
Power supply clamping voltage at T_J = -40°C	$V_{S(CLAMP)\_-40}$	I_{VS} = 5 mA T_J = -40°C	33	36.5	42	V
Power supply clamping voltage at T_J ≥ 25°C	$V_{S(CLAMP)\_25}$	I_{VS} = 5 mA T_J ≥ 25°C	35	38	44	V

Electrical Characteristic (continued)

V_S = 6V to 18V, T_j= -40°C to 150°C; Typical values stated at T_j= 25°C and V_S = 13.5V, Digital input (DI) pins = IN, DEN, DSEL; R_L = 4.7Ω.unless otherwise specified.

Description	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Protection						
Automatic Retries in Case of Fault after a Counter Reset	$n_{RETRY(CR)}$			5		
Automatic Retries in Case of Fault after the First t_{RETRY} Activation	$n_{RETRY(NT)}$			1		
Maximum "Retry" Cycles allowed before Channel Latch OFF	$n_{RETRY(CYC)}$			2		
Auto Retry Time after Fault Condition	t_{RETRY}		40	70	100	ms
Counter Reset Delay Time after Fault Condition	$t_{DELAY(CR)}$		40	70	100	ms
Minimum DEN pulse duration for counter reset	$t_{DEN(CR)}$		50	100	150	µs
Overload Detection Current at T_J = -40 °C	$I_{L(OVL0)\_-40}$	T_J = -40 °C dI/dt = 0.4 A/µs	38	45	53	A
Overload Detection Current at T_J = 25 °C	$I_{L(OVL0)\_25}$	T_J = 25 °C dI/dt = 0.4 A/µs	36	44	53	A
Overload Detection Current at T_J = 150 °C	$I_{L(OVL0)\_150}$	T_J = 150 °C dI/dt = 0.4 A/µs	28	36	44	A
Overload Detection Current at High V_{DS}	$I_{L(OVL1)}$	dI/dt = 0.4 A/µs		20		A
Overload Detection Current at Jump Start Condition and CLS mode	$I_{L(OVL\_JS)}$	$V_S > V_{S(JS)}$ dI/dt = 0.4 A/µs		20		A
Diagnosis						
SENSE saturation current	$I_{IS(SAT)}$	V_S = 6V to 20V R_{SENSE} = 1.2kΩ	4.4		15	mA
SENSE leakage current when disabled	$I_{IS(OFF)}$	DEN = "low" $I_L \geq I_{L(NOM)}$ V_{IS} = 0 V		0.01	0.5	µA
SENSE leakage current when enabled at $T_J \leq$ 85°C	$I_{IS(EN)\_85}$	$T_J \leq$ 85°C DEN = "high" I_L = 0A		0.2	2	µA
SENSE leakage current when enabled at T_J = 150°C	$I_{IS(EN)\_150}$	T_J = 150°C DEN = "high" I_L = 0A		0.2	2	µA
Saturation voltage in k_{ILIS} operation (VS-VIS)	V_{SIS_k}	V_S = 5 V INx = DEN = "high"		0.5	1	V
Saturation voltage in open load at OFF diagnosis (V_S-V_{IS})	V_{SIS_OL}	V_S = 5 V INx = "low" DEN = "high"		0.5	1	V

Electrical Characteristic (continued)

V_S = 6V to 18V, T_j= -40°C to 150°C; Typical values stated at T_j= 25°C and V_S = 13.5V, Digital input (DI) pins = IN, DEN, DSEL; R_L = 4.7Ω.unless otherwise specified.

Description	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Saturation voltage in open load at OFF diagnosis (V_S-V_{IS})	V_{SIS_OL}	V_S = 5 V INx = "low" DEN = "high"		0.5	1	V
Saturation voltage in fault diagnosis (VS-VIS)	V_{SIS_F}	V_S = 5 V INx = "low" DEN = "high" counter > 0		0.5	1	V
Power supply to IS pin clamping voltage at T_J =-40°C	$V_{SIS(CLAMP)\_-40}$	I_{IS} = 1mA T_J = -40°C	33	36.5	42	V
Power supply to IS pin clamping voltage at T_J ≥ 25°C	$V_{SIS(CLAMP)\_25}$	I_{IS} = 1 mA T_J ≥ 25°C	35	38	44	V
SENSE fault current	$I_{IS(FAULT)}$		4.4	5.5	10	mA
SENSE open load in OFF current	$I_{IS(OLOFF)}$		1.9	2.5	3.5	mA
SENSE delay time at channel switch ON after last fault condition	$t_{IS(FAULT)\_D}$			500		µs
SENSE open load in OFF delay time	$t_{IS(OLOFF)\_D}$	V_{DS} < $V_{DS(OLOFF)}$ from INx falling edge to I_{IS} = $I_{IS\ (OLOFF),MIN}$ · 0.9 DEN = "high" $n_{RETRY(CR)}$ = 0	30	70	120	µs
VDS threshold for k_{ILIS} enable	$V_{DS(kILIS\_EN)}$		0.8	1.2	1.4	V
Open load VDS detection threshold in OFF state	$V_{DS(OLOFF)}$		1.3	1.8	2.3	V
SENSE settling time with nominal load current stable	$t_{sIS(ON)}$	I_L = $I_{L(NOM)}$ from DEN rising edge to I_{IS} = I_L / ($k_{ILIS,MAX}$ @ I_L) · 0.9		5	20	µs
SENSE disable time	$t_{sIS(OFF)}$	I_L = $I_{L(NOM)}$ From DEN falling edge to I_{IS} = $I_{IS(OFF)}$		5	20	µs
SENSE settling time after load change	$t_{sIS(LC)}$	from I_L = $I_{L(NOM)/2}$ to I_L = $I_{L(NOM)}$		5	20	µs
Open load output current at I_{IS} = 4 µA	$I_{L(OL)\_4u}$	I_{IS} = $I_{IS(OL)}$ = 4µA	8	21	35	mA

Electrical Characteristic (continued)

V_S = 6V to 18V, T_j= -40°C to 150°C; Typical values stated at T_j= 25°C and V_S = 13.5V, Digital input (DI) pins = IN, DEN, DSEL; R_L = 4.7Ω.unless otherwise specified.

Description	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current sense ratio at $I_L = I_{L02}$	k_{ILIS02}	I_{L02} = 20mA	-29.3%	1800	+29.3%	
Current sense ratio at $I_L = I_{L05}$	k_{ILIS05}	I_{L05} = 100mA	-24%	1800	+24%	
Current sense ratio at $I_L = I_{L08}$	k_{ILIS08}	I_{L08} = 250mA	-23.5%	1800	+23.5%	
Current sense ratio at $I_L = I_{L11}$	k_{ILIS11}	I_{L11} = 1A	-12%	1800	+12%	
Current sense ratio at $I_L = I_{L13}$	k_{ILIS13}	I_{L14} = 2A	-7.3%	1800	+7.3%	
Current sense ratio at $I_L = I_{L15}$	k_{ILIS15}	I_{L16} = 4A	-4.1%	1800	+4.1%	
SENSE Current Derating with Low Current Calibration	$\Delta k_{ILIS(OL)}$	$I_{L(CAL)\_OL} = I_{L05}$ $I_{L(CAL)\_OL\_H} = I_{L08}$ $I_{L(CAL)\_OL\_L} = I_{L02}$ $T_{A(CAL)}$ = 25°C	-16	0	16	%
SENSE Current Derating with Norminal Current Calibration	$\Delta k_{ILIS(NOM)}$	$I_{L(CAL)\_OL} = I_{L13}$ $I_{L(CAL)\_OL\_H} = I_{L15}$ $I_{L(CAL)\_OL\_L} = I_{L11}$ $T_{A(CAL)}$ = 25°C	-4	0	4	%

4. General Description

4.1 I/O pins

The device has 4 digital pins for direct control. Digital input (DI) pins = IN0, IN1, DEN, DSEL.

4.1.1 Input pins

The input pins IN0 and IN1 control their respective output channels, with input circuitry optimized for 3.3V/5V microcontroller interfaces (typical tolerance ±10%). The schematic equivalent of this interface configuration is detailed in Figure 4. For unused pins, connect to GND terminal through a 10kΩ resistor.

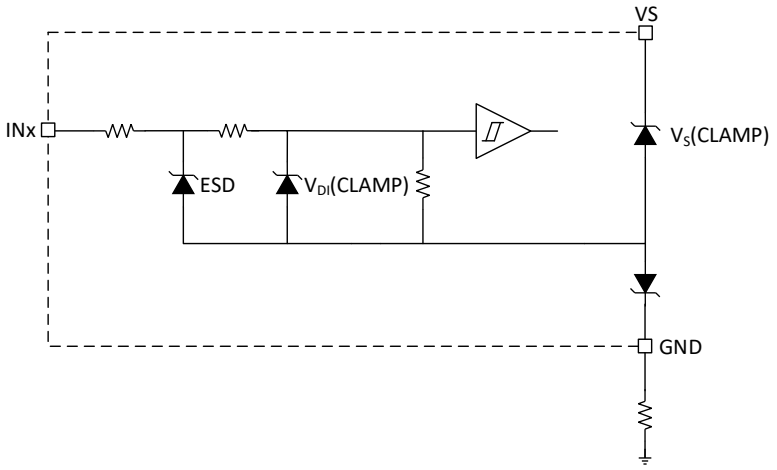


Figure 4. CPSQ54D20 Input circuitry

The voltage thresholds for LOW and HIGH logic states are determined by parameters $V_{DI(TH)}$ and $V_{DI(HYS)}$. The relationship between these two values is shown in Figure 5.

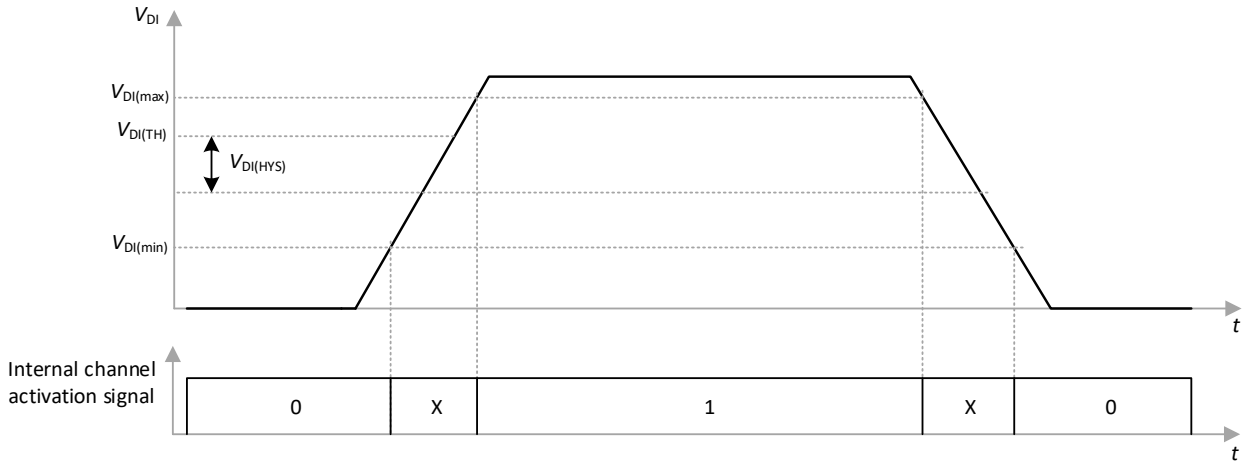


Figure 5. Input threshold voltage and hysteresis

4.1.2 Diagnosis pins

The DEN pin controls both diagnostic and protection circuits. A HIGH level enables diagnostics, while a LOW level disables diagnostics and sets the IS pin to high-impedance. The diagnosis channel is selected by Diagnosis Selection (DSEL) pin. The falling edge of the DEN pin clears the protection latch of the channel selected by the DSEL pin, depending on both the logic of IN0/1 pin and the DEN pulse length.

4.2 Operation Modes

The device operates in six distinct modes:

a. Sleep

b. Inactive with diagnosis

c. Active with diagnosis

d. Active without diagnosis

e. Capacitive load switching with diagnosis

f. Capacitive load switching without diagnosis

Mode transitions are controlled by IN0/1 pin logic levels, IN0/1 pin PWM signals, DEN and DSEL pin status.

Figure 6 illustrates the state transition diagram. Device behavior and parameters may vary independently of operational modes. The integrated under-voltage detection circuit monitoring V_S supply voltage can also trigger operational adjustments within the same mode.

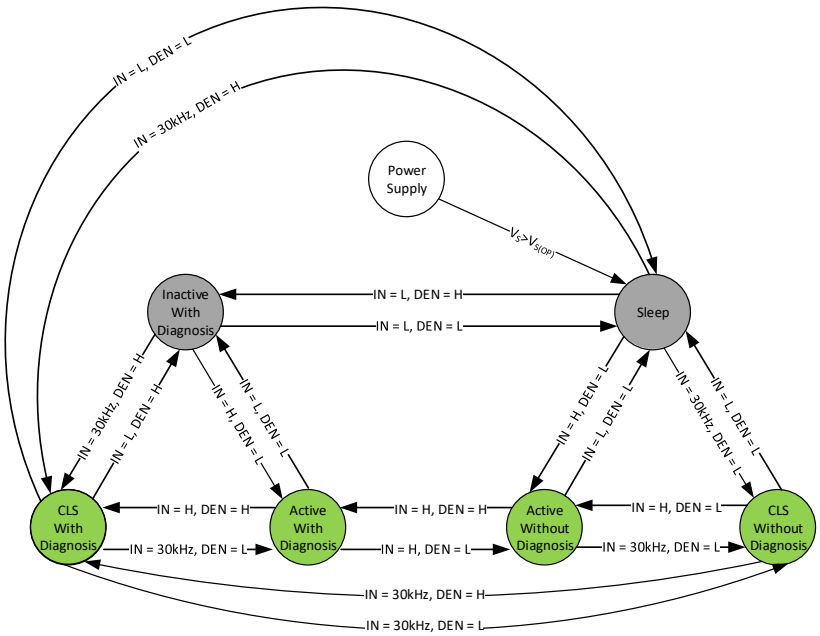


Figure 6. Operation mode state diagram

The table below shows the relationships between operational modes, VS supply voltage levels, and the status of channel status and diagnosis.

Operation mode	Function	$V_S > V_{S(OP)}$	$V_S < V_{S(OP)}$
Sleep	Channels	OFF	OFF
	Diagnosis	OFF	OFF
Inactive with diagnosis	Channels	OFF	OFF
	Diagnosis	ON	OFF
Active with diagnosis	Channels	ON	OFF
	Diagnosis	ON	OFF
Active without diagnosis	Channels	ON	OFF
	Diagnosis	OFF	OFF
Capacitive load switching mode with diagnosis	Channels	ON	OFF
	Diagnosis	ON	OFF
Capacitive load switching mode without diagnosis	Channels	ON	OFF
	Diagnosis	OFF	OFF

Sleep: The device enters sleep mode when digital input (DI) = LOW, the current consumption reduces to $I_{VS(SLEEP)}$ level while over-temperature protection, overload protection, and under-voltage detection are disabled. Sleep mode activation requires inactive protection conditions: $n_{RESTART(CR)}$ = 0, junction temperature T_J must remain below $T_{J(ABS)}$, and the temperature differential (T_J - $T_{J(REF)}$) must stay under $T_{J(DYN)}$ including hysteresis parameters.

Active with diagnosis: Active with diagnosis mode serves as the standard operational state of device. The device activates this diagnosis mode for corresponding channels when both IN and DEN = HIGH, enabling output with integrated diagnostic functionality. Operational current consumption during this mode is governed by the $I_{GND(ACTIVE)}$.

Inactive with diagnosis: The device operates in inactive with diagnosis mode when the DEN = HIGH and IN = LOW, maintaining channels in OFF state which enables open load detection in OFF condition. This mode may generate either fault current $I_{IS(FAULT)}$ or open load current $I_{IS(OLOFF)}$ at the IS pin depending on load conditions, with corresponding elevation in device current consumption during operation

Active without diagnosis: The device is in active without diagnosis mode when IN = HIGH and DEN = LOW, in this condition, the output is switched ON without diagnosis.

Capacitive load switching mode with diagnosis: The device has capacitive load switching capability to manage capacitive loads, with diagnosis activated when IN = $f_{VIN(CLS)}$ and DEN = HIGH, triggering output activation with integrated diagnostics while maintaining current consumption defined by the $I_{GND(ACTIVE)}$ parameter.

Capacitive load switching mode without diagnosis: The device is in capacitive load switching mode without diagnosis when IN = $f_{VIN(CLS)}$ and DEN = LOW, in this condition, output is switched ON without diagnosis.

5. Operation Detail Description

5.1 Power Stage

The high-side power stages utilize N-channel vertical power MOSFET integrated with charge pump.

5.1.1 Output ON-state resistance

The ON-state resistance $R_{DS(ON)}$ depends mainly on junction temperature T_J. Figure7 shows the $R_{DS(ON)}$ across the whole T_J range.

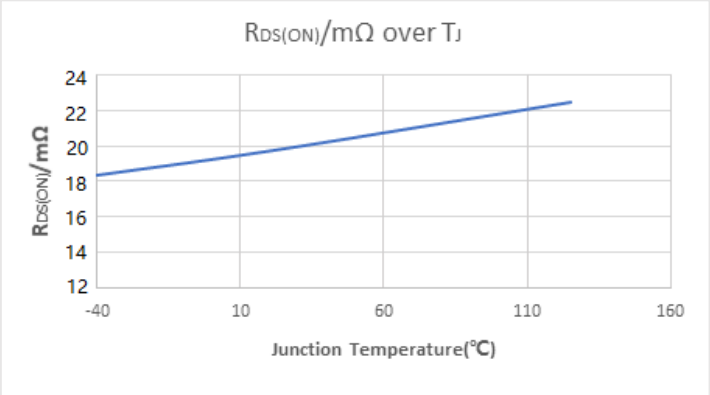


Figure 7. $R_{DS(ON)}$ over T_J

5.1.2 Switching resistive loads

For resistive load switching operations, the switching times and slew rates shown in Figure8 serve as reference values. The switching energy parameters E_{ON} and E_{OFF} exhibit direct proportionality to both load resistance and corresponding switching time intervals (t_{ON} and t_{OFF}).

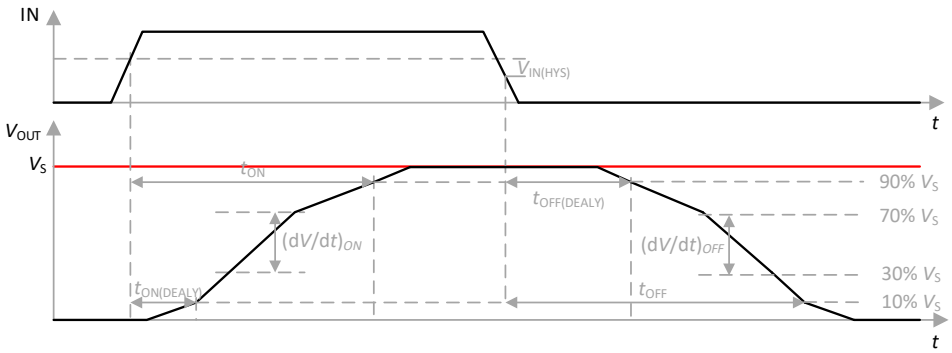


Figure 8. Switching resistive load timing diagram

5.1.3 Switching inductive loads

During high-side switch deactivation with inductive loads, the output voltage V_{OUT} experiences negative undershoot below ground potential as the inductive load strives to sustain current flow. To prevent overvoltage-induced device failure, the integrated voltage clamping architecture restricts the output voltage to ensure V_{DS} remains within the $V_{DS(CLAMP)}$ threshold. Figure 9 provides a schematic representation of this protective mechanism. The clamping functionality remains operational across all specified device operating modes.

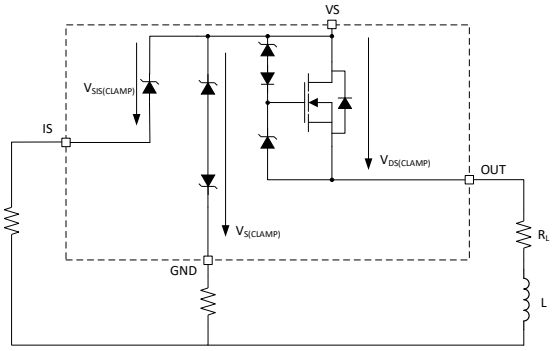


Figure 9. Output clamping circuit

During demagnetization of inductive loads, energy has to be dissipated in the device. The energy can be calculated with:

$$E = V_{\mathrm{DS(CLAMP)}} * \left[\frac{V_S - V_{\mathrm{DS(CLAMP)}}}{R_\mathrm{L}} * \ln\left(1 - \frac{R_\mathrm{L} * I_\mathrm{L}}{V_S - V_{\mathrm{DS(CLAMP)}}}\right) + I_\mathrm{L}\right] * \frac{I_\mathrm{L}}{R_\mathrm{L}}$$

The maximum energy the device can sustain is limited by the thermal design. The maximum allowed values of E_{AS} (single pulse energy) and E_{AR} (repetitive energy) is shown in EC table.

5.1.4 Switching capacitive loads

The CPSQ54D20 incorporates a dedicated Capacitive Load Switching (CLS) mode, where activation of the $f_{VIN(CLS)}$ signal initiates a transition to CLS mode following a fixed $t_{ON\_CLS(DELAY)}$ initialization period, as detailed in Figure 10. Throughout CLS mode operation, both protection and diagnosis functions are active.

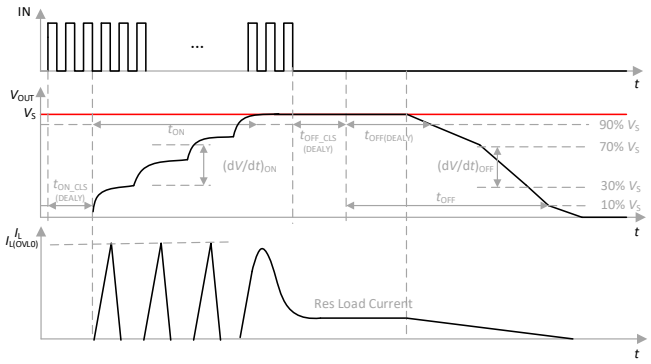


Figure 10. Capacitive load switching activations

During CLS mode operation, the dynamic over-temperature protection is reduced to $T_{J(DYN)\_CLS}$ with continuous restart. System architecture automatically executes mode transition to active state when V_{DS} parameters satisfy the $V_{DS(OLOFF)}$ comparator criteria.

Conversely, maintenance of VDS levels exceeding $V_{DS(OLOFF)}$ mandates CLS mode termination within the t_{CLS1} maximum duration threshold through input signal modulation to either LOW or HIGH states.

A transition from CLS mode to active mode shall be performed only if there is no short circuit detected, and when normal load current is detected, the mode transition is permitted. If no current (open load condition) is measured, potential output short circuit must be checked through external voltage measurement at the output terminals. Only after confirming the absence of short circuit (via valid voltage reading) can the mode transition be completed. This procedure ensures safe mode switching by distinguishing between normal operation, open circuit, and short circuit scenarios through sequential current-voltage verification.

5.1.5 Inverse current behavior

When V_{OUT} exceeds V_S, current $I_{L(INV)}$ flows into the power output transistor. This operational state is defined as "Inverse Current".

When the channel is in the OFF state, current flows through the intrinsic body diode, generating high power losses that lead to an overall temperature rise in the device. This may trigger the protection due to over-temperature, causing channel to shut down. When the channel is in the ON state, $R_{DS(INV)}$ characteristics are exhibited, with power dissipation in the output stage comparable to normal operation under $R_{DS(ON)}$ conditions. During inverse current conditions, the channel maintains its current state (ON or OFF) as long as the condition $|-I_L| < |-I_{L(INV)}|$ is satisfied. The Inverse ON feature enables active switching ON of the channel during inverse current conditions when $|-I_L| < |-I_{L(INV)}|$ is met, the operational principle is shown in Table 5.

Table 5. Inverse On Channel behavior in case of applied inverse current

IN	HIGH		LOW	
I_{Load}	NORMAL	INVERSE	NORMAL	INVERSE
Power Stage	ON	ON	OFF	OFF

5.2 Protection

The CPSQ54D20 is equipped with overload, overtemperature, and overvoltage protection. Overtemperature and overload protections remain active in all operational modes except sleep mode. Overload protection is not activated during inverse current conditions, and both overtemperature and overload protections are disabled for channel operating under inverse current conditions. Overvoltage protection remains effective across all operational modes.

5.2.1 Overcurrent protection

The CPSQ54D20 features overload and short circuit protection. As shown in Figure 12, two overload thresholds are defined and both thresholds are automatically selected based on the voltage VDS across the power DMOS:

$I_{L(OVL0)}$ when V_{DS} < 15V

$I_{L(OVL1)}$ when V_{DS} > 15V

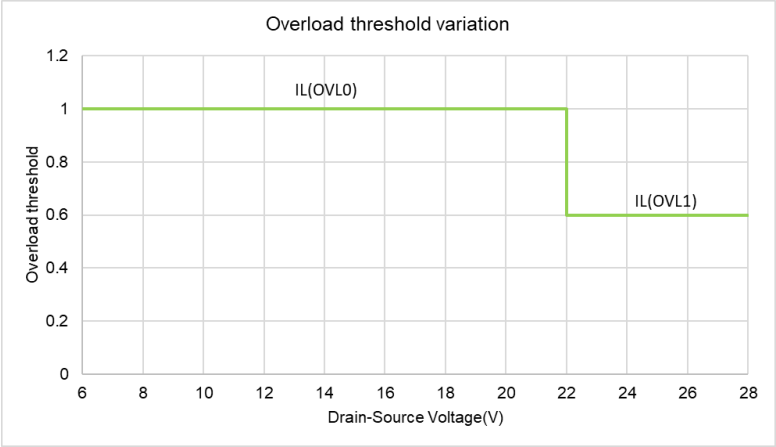


Figure 12. Overload Current Thresholds variation with VDS

To allow for higher load inrush at low temperatures, the overload threshold is maximized at low temperatures and decreases as T_J rises, as shown in Figure 13. $I_{L(OVL0)}$ typical remains approximately constant at junction temperatures as high as +75 °C.

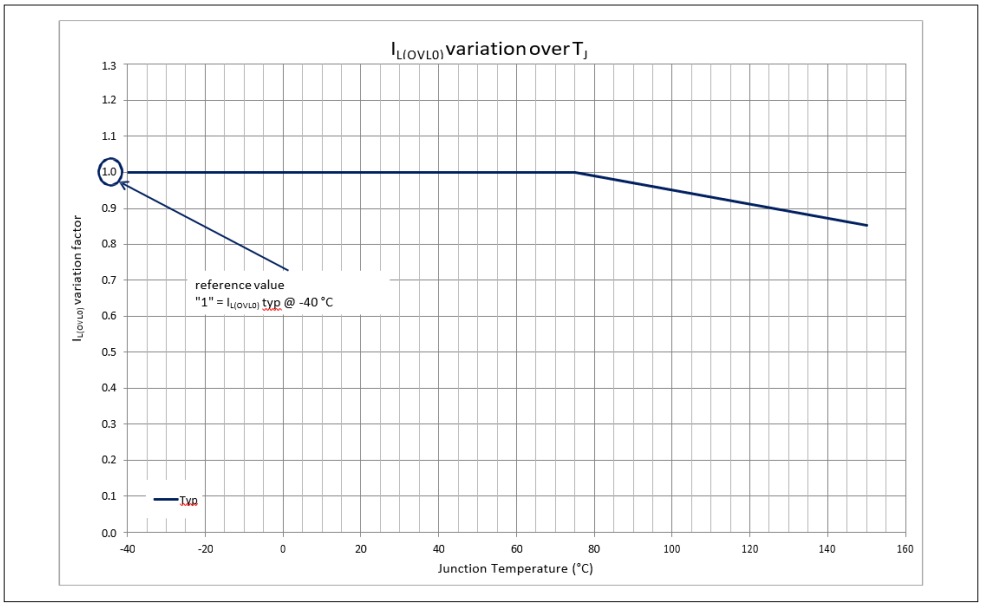


Figure 13. Overload Current Thresholds variation with T_J

The supply voltage V_S may rise above 18V for a short period of time, e.g. during a load dump or jump-start condition. As long as $V_S \geq V_{S(JS)}$, the overload detection current is set to $I_{L(OVL\_JS)}$ as shown in Figure 14.

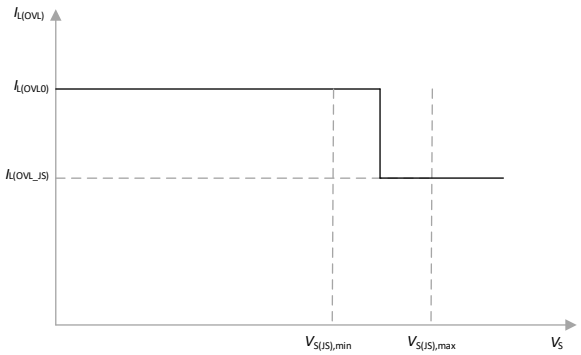


Figure 14. Overload Current Thresholds variation with Vs

When $I_L \geq I_{L(OVL)}$ ($I_{L(OVL0)}$, $I_{L(OVL1)}$ or $I_{L(OVL\_JS)}$), the channel is switched OFF. The channel will restart according to the retry strategy.

5.2.2 Overtemperature protection

The device incorporates both absolute $T_{J(ABS)}$ and dynamic $T_{J(DYN)}$ temperature protection. If the junction temperature T_J rises above one of two thresholds $T_{J(ABS)}$ or $T_{J(DYN)}$, the channel will shut down. The channel will make an automatic restart attempt. The channel remains off until the junction temperature reaches the restart conditions described in the table below. If the number of automatic restart exceeds $n_{RESTART(CR)}$, the channel will latch off to prevent damage. The behavior is shown in Figure 15 and Figure 16.$T_{J(REF)}$ is the reference temperature used for dynamic temperature protection.

Fault condition	Switch OFF event	"Restart" condition
Overtemperature	$T_J \geq T_{J(ABS)}$ or $(T_J - T_{J(REF)}) \geq$ TJ(DYN)	$T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis)
Overload	$I_L \geq I_{L(OVL)}$	I_L < 50 mA T_J within $T_{J(ABS)}$ and $T_{J(DYN)}$ ranges (including hysteresis)

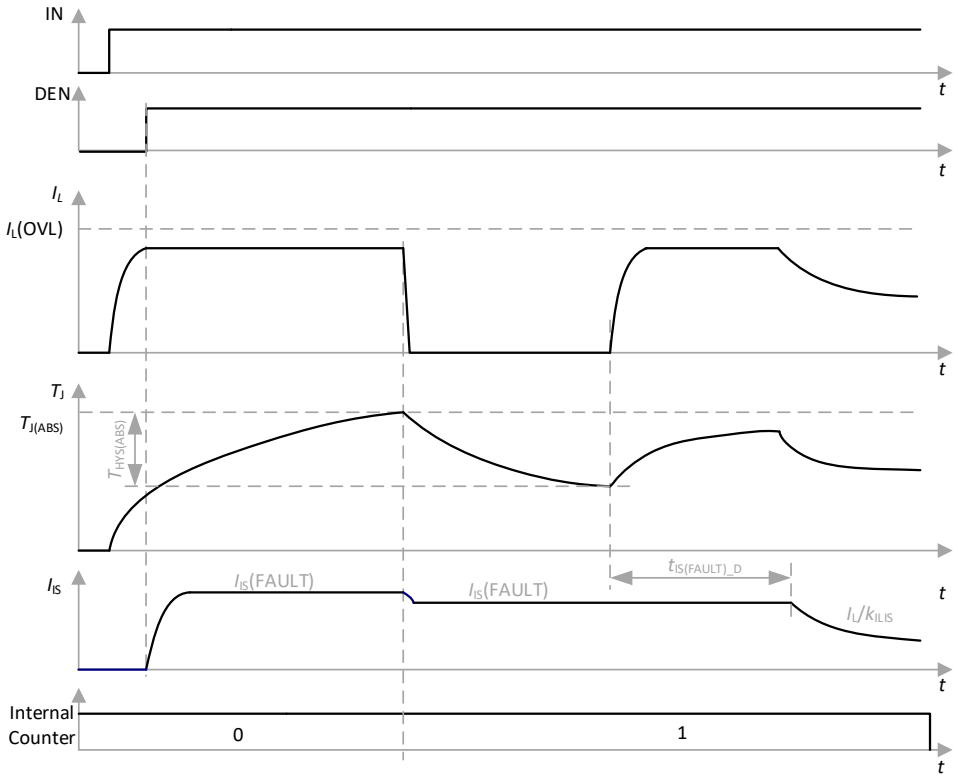


Figure 15. Overtemperature protection (absolute)

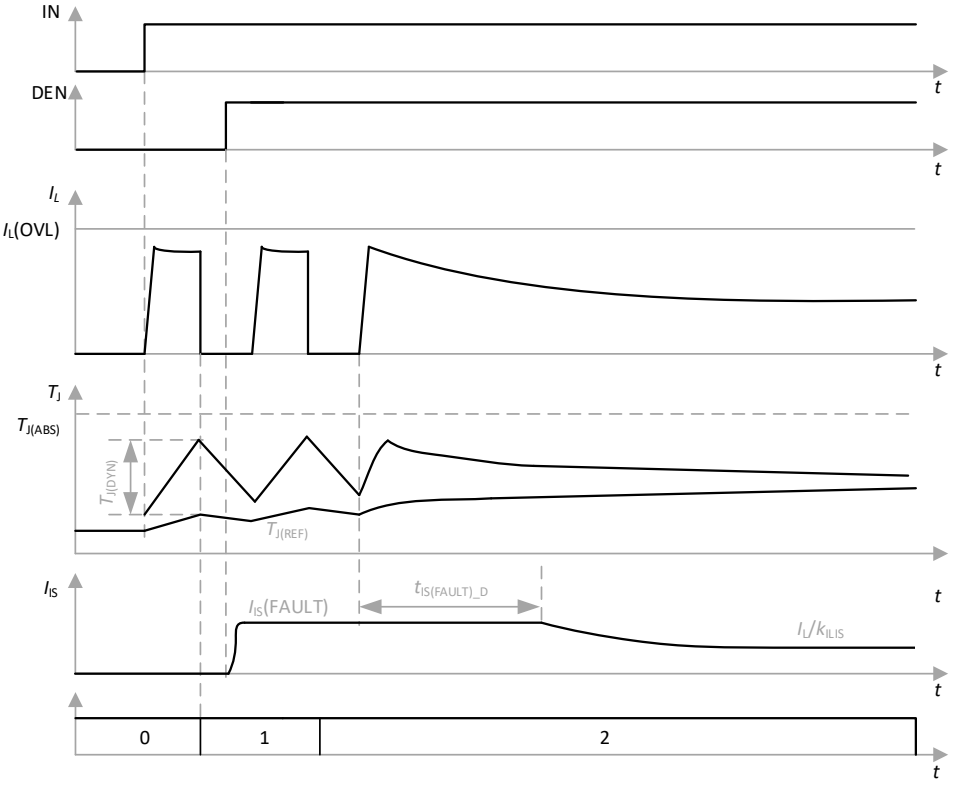


Figure 16. Overtemperature protection (dynamic)

5.2.3 Retry strategy

The channel is switched ON when IN = HIGH. If a fault occurs, the output stage is switched OFF. The channel can only be restarted when the restart conditions are satisfied.

The channel can attempt to switch ON for $n_{RETRY(CR)}$ times before switching OFF. After t_{RETRY} time, if the IN remains HIGH, the channel will switch ON again for $n_{RETRY(NT)}$ times before switching OFF again (a "retry" cycle). After $n_{RETRY(CYC)}$ consecutive retry cycles, the channel latches OFF permanently. To reset the channel, the input pin must be held LOW for longer than $t_{DELAY(CR)}$ ("counter reset delay"), which resets the internal counter to its default value.

During the counter reset delay, If the IN = HIGH, the channel remains OFF and the $t_{DELAY(CR)}$ timer resets. The timer only resumes counting when the input pin returns to LOW. If the IN stays LOW beyond $t_{DELAY(CR)}$, the internal retry counter resets, allowing $n_{RETRY(CR)}$ retries upon the next activation.

The timing diagram of retry strategy is shown in Figure 17.

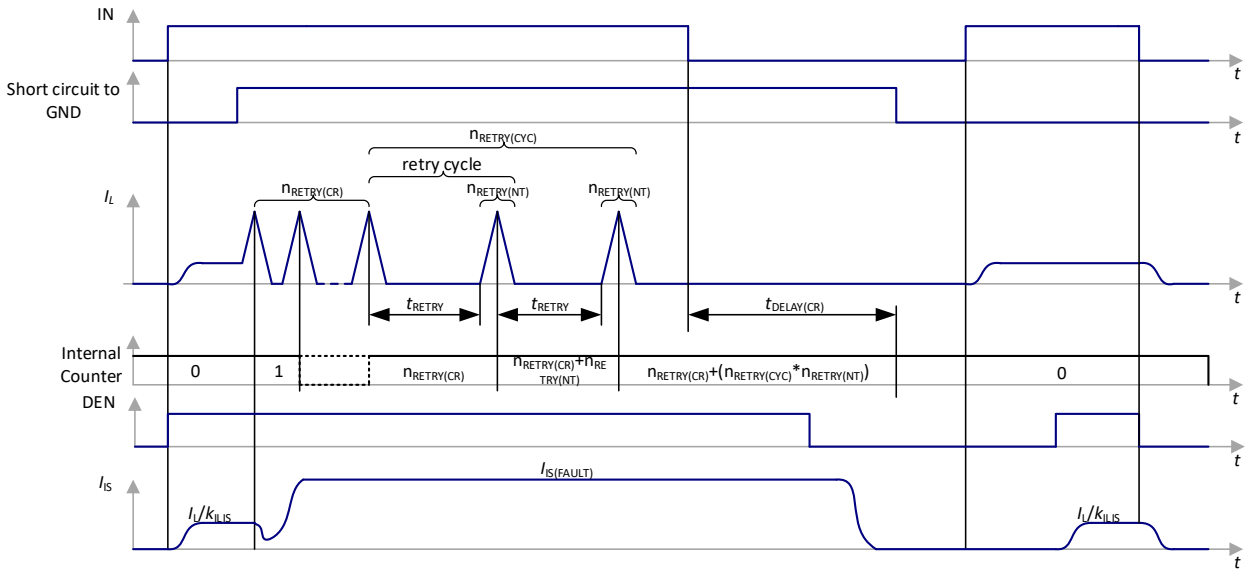


Figure 17. Retry strategy timing diagram

The internal counter can be reset without waiting for $t_{DELAY(CR)}$ by sending a pulse to the DEN pin while IN = LOW. This DEN pulse must remain HIGH for longer than $t_{DEN(CR)}$ to guarantee counter reset. The DSEL pin must select the channel requiring de-latch and maintain the same logic value during two DEN pin transitions (rising edge followed by falling edge). Force retry strategy timing diagram is shown in figure 18.

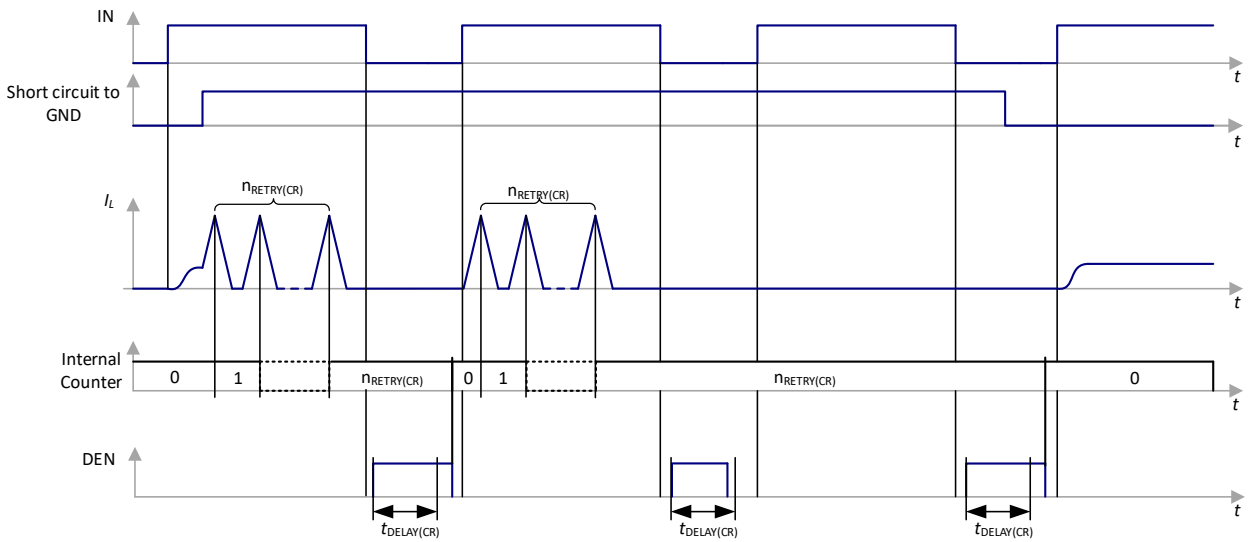


Figure 18 Retry Strategy Timing Diagram with Forced Reset

5.2.4 Additional protection

5.2.4.1 Overvoltage protection

When the supply voltage is between $V_{S(EXT,UP)}$ and $V_{BAT(LD)}$, the output transistors remain active and track the input signal.

Alongside the inductive load shutdown described in Section 4.3.3, a V_S-to-GND overvoltage clamp ($V_{S(CLAMP)}$) protects the logic and output channels by monitoring the VS pin voltage.

5.2.4.2 Loss of battery and loss of load

Device robustness remains unaffected by battery or load disconnection when handling resistive loads and wiring. However, when driving inductive loads, the stored energy in the inductance requires management.

The device supports wire harness inductances up to 10 µH under $I_{L(NOM)\_85}$ conditions.

For applications exceeding these current and/or inductance limits, an external suppressor diode (e.g., D_{Z2} in Section 1.1) is recommended to manage inductive energy and ensure a controlled load current discharge path.

5.2.4.3 Loss of ground

A resistor should be connected between each digital input pin and the microcontroller to guarantee channel deactivation during device ground loss events.

If a digital input pin is grounded (via resistor or active pull-down), a parasitic ground path may form, potentially maintaining device operation during ground loss scenarios.

5.3 Diagnosis

To enable diagnostic functionality, the device provides a proportional sense current signal (IIS) at the IS pin. When diagnostics are disabled (DEN pin set low), the IS pin enters a high-impedance state. The Diagnosis block diagram is shown in Figure 19.

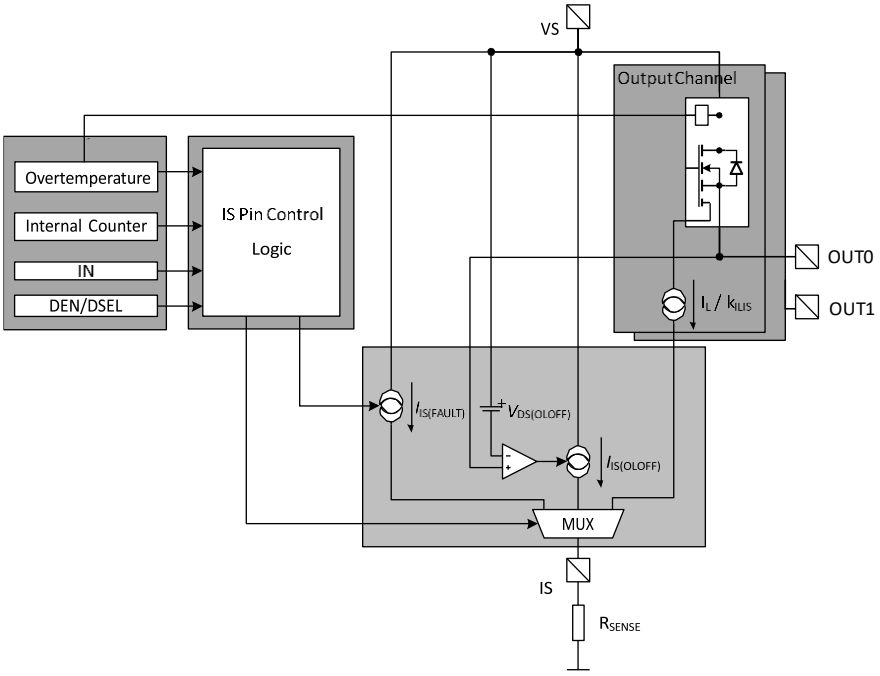


Figure 19. Diagnosis block diagram

If current sense diagnostics are implemented, a sense resistor (RSENSE) must be connected between the IS pin and module ground. This resistor shall exceed 820Ω to limit power dissipation in the sensing circuitry, with a typical value of 1kΩ.

Due to the internal connection between the IS pin and VS supply voltage, connecting the IS pin to sense current outputs of other devices is not recommended if those devices are powered by separate battery sources.

Below table gives a quick reference to the state of the IS pin during the device operation.

Operation mode	Input level	DEN level	VOUT	Diagnostic output
Normal operation	LOW/OFF	HIGH	~ GND	Z IIS(FAULT) if counter > 0
Short circuit to GND			~ GND	Z IIS(FAULT) if counter > 0
Thermal shutdown temperature (absolute)			Z	IIS(FAULT)
Thermal shutdown temperature (dynamic)			Z	IIS(FAULT)
Short circuit to VS			= VS	IIS(OLOFF)

				IIS(FAULT) if counter > 0
Open load			< VS - VDS(OLOFF) > VS - VDS(OLOFF) 1)	Z IIS(OLOFF) or IIS(FAULT) if counter > 0 for both cases
Inverse current			~ VINV = VOUT > VS	IS(OLOFF) or IIS(FAULT) if counter > 0
Normal operation	HIGH/ON or CLS		< VS - VDS(kILIS_EN)	IIS = IL / kILIS
Short circuit to GND			~ GND	IIS(FAULT)
Thermal shutdown temperature (absolute)			Z	IIS(FAULT)
Thermal shutdown temperature (dynamic)			Z	IIS(FAULT)
Short circuit to VS			= VS	IIS < IL / kILIS
Open load			~ VS	IIS = IIS(EN)
Inverse current			~ VINV = VOUT > VS	IIS = IIS(EN)
Current limitation			< VS	IIS(FAULT)
Underload			~ VS	IIS(EN) < IIS < IL(NOM) / kILIS
All conditions	N.A.	LOW	N.A.	Z

The sense channel selection is done with DSEL pin according to the table below:

DEN	DSEL	IS
LOW	/	Z
HIGH	LOW	SENSE output 0
HIGH	HIGH	SENSE output 1

5.3.1 Diagnosis in ON state

The IS pin outputs a load-proportional current signal ($I_{IS}=I_L/k_{ILIS}$) when all conditions below are met: Power output stage is in conduction state with $V_{DS} < V_{DS(kILIS\_EN)}$, channel diagnostics are enabled, and no active faults.

During sustained fault conditions, the IS pin outputs $I_{IS(FAULT)}$characteristic fault current.

5.3.1.1 Current sense (k_{ILIS})

The sensing current IIS demonstrates a linear relationship with the output current IL until saturation at $I_{IS(SAT)}$. Under open-load conditions ($I_L \approx 0A$), the IS pin delivers the maximum diagnostic current $I_{IS(EN)}$ (defined with

enabled diagnostics and no load), as depicted in Figure 20. The central trace indicates the ideal k_{ILIS} ratio, with peripheral traces representing typical product boundaries. An external RC filter between the IS pin and microcontroller ADC input must maintain a minimum 1μs time constant (R×C≥1μs) for noise suppression. The k_{ILIS} tolerance range accounts for temperature variations (-40°C to +150°C), supply voltage fluctuations (±15% nominal), and manufacturing process deviations.

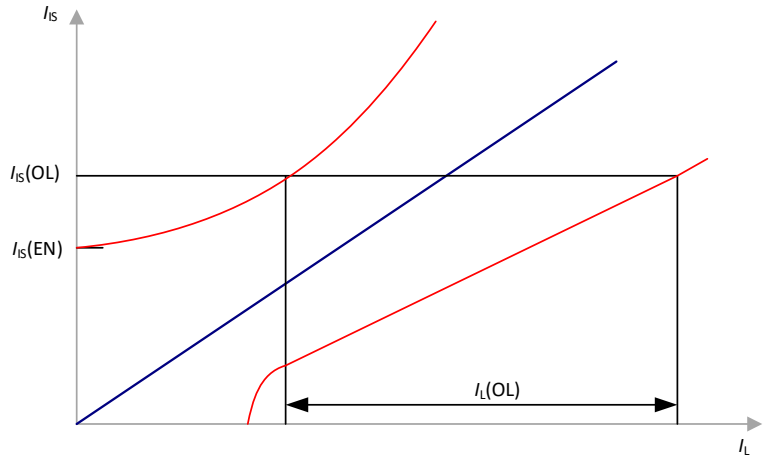


Figure 20. Current sense ratio in open load at ON condition

5.3.1.2 Fault current ($I_{IS(FAULT)}$)

Upon a protection event triggering a change in the internal retry counter, the IS pin delivers a fault current $I_{IS(FAULT)}$ when DEN is high. Scenarios include: If the channel is ON with retry counts below "$n_{RETRY(CR)}$ + $n_{RETRY(CYC)}$ × $n_{RETRY(NT)}$", $I_{IS(FAULT)}$ persists for $t_{IS(FAULT)\_D}$ post-restart before reverting to I_{IS} = I_L/k_{ILIS}(as shown in Figure 21), with $I_{IS(FAULT)}$ recurring during each diagnostic check within retry cycles (t_{RETRY} active). If retries equal "$n_{RETRY(CR)}$ + $n_{RETRY(CYC)}$ × $n_{RETRY(NT)}$", $I_{IS(FAULT)}$ continues until counter reset via IN = LOW for $t_{DELAY(CR)}$ or IN = LOW and DEN pulse for $t_{DEN(CR)}$. If the channel is OFF with a non-reset counter, $I_{IS(FAULT)}$ activates during each diagnostic check.

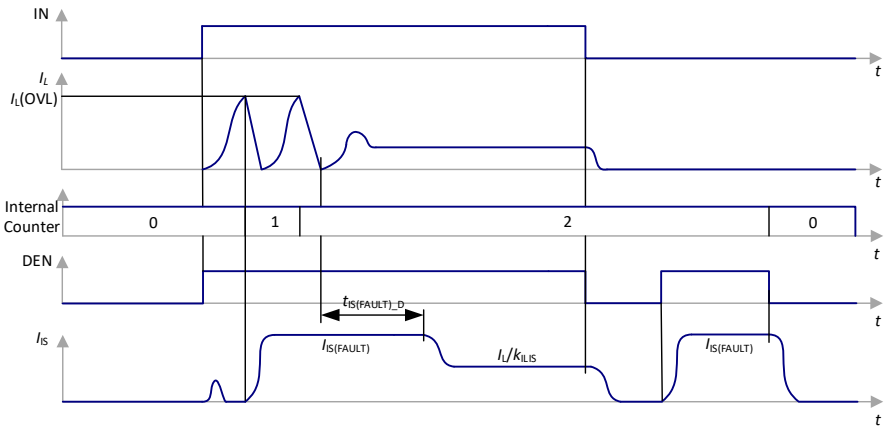


Figure 21. IIS(FAULT) at load switching

Figure 22 shows the SENSE behavior in short circuit condition and Figure 22 shows the relation between I_{IS} = I_L/k_{ILIS}, $I_{IS(SAT)}$ and $I_{IS(FAULT)}$.

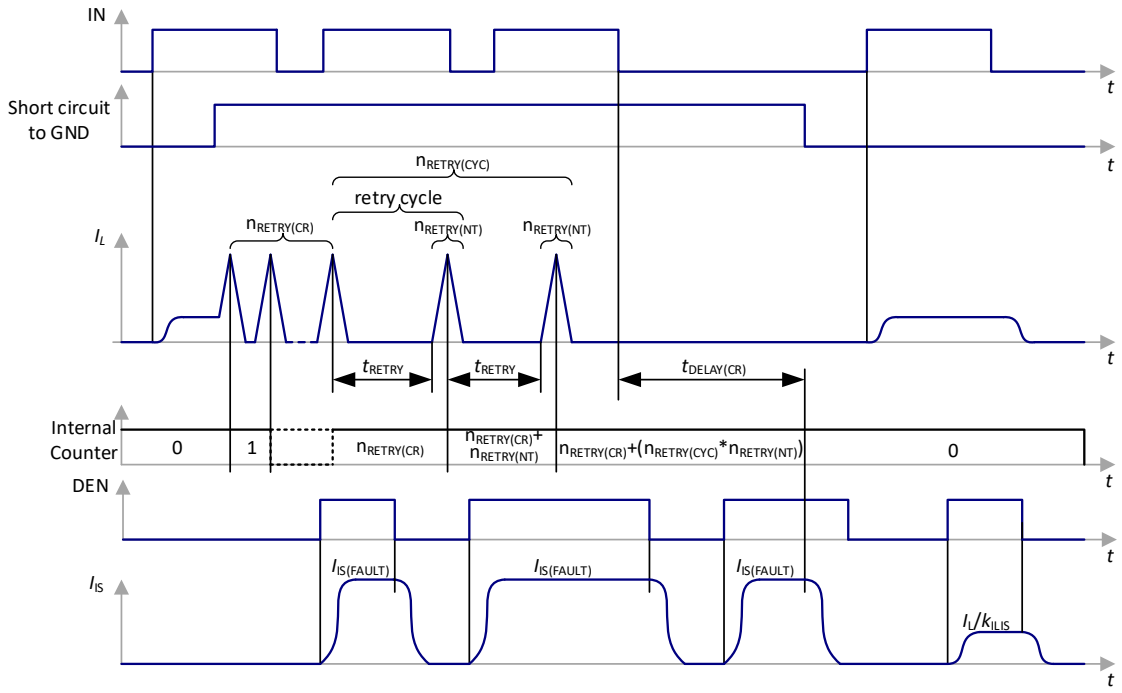


Figure 22. SENSE behavior in fault condition

5.3.2 Diagnosis in OFF State

When the power output stage is in OFF state, the device measures the output voltage and compares it with a threshold voltage. By utilizing external components (a pull-down resistor and a switchable pull-up current source), it detects load disconnection or short circuits to the battery. If a fault condition is detected (the internal counter deviates from its reset value), a current $I_{IS(FAULT)}$ is sourced from the IS pin during channel diagnosis checks, even in OFF state.

In OFF state with the DEN = HIGH, the V_{DS} voltage is compared to the threshold $V_{DS(OLOFF)}$. When diagnosis is active and $V_{DS} \leq V_{DS(OLOFF)}$, the IS pin provides $I_{IS(OLOFF)}$ current. If the load is properly connected without a battery short ($V_{DS} \approx V_S$, resulting in $V_{DS} > V_{DS(OLOFF)}$), the IS pin enters high impedance. Figure 23 demonstrates the non-overlapping relationship between $I_{IS(OLOFF)}$ and $I_{IS(FAULT)}$ as functions of V_{DS}, ensuring unambiguous differentiation between Open Load in OFF state and Fault conditions.

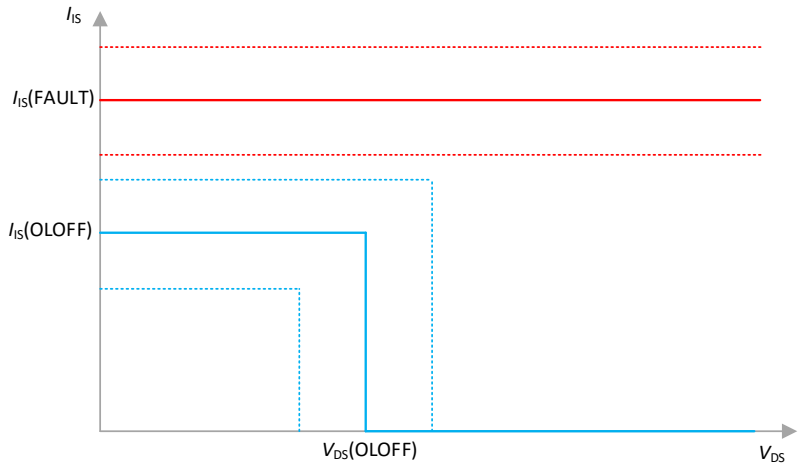


Figure 23. I_{IS} in OFF State

A time $t_{IS(OLOFF)\_D}$ must be allowed between the falling edge of the input pin and the sensing at the IS pin for Open Load in OFF diagnosis to enable the internal comparator to settle, with Figure 24 showing the Open Load detection timings where the load remains permanently disconnected.

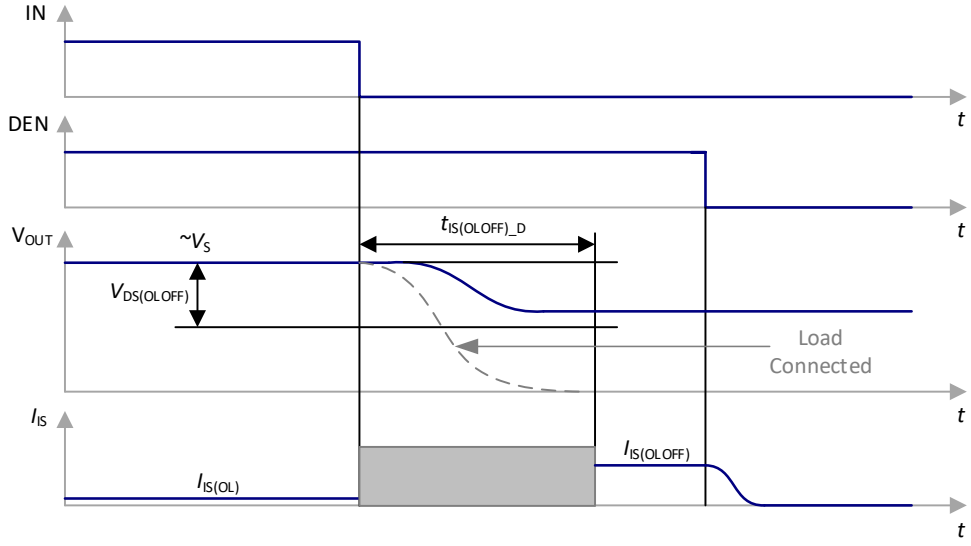


Figure 24. Open load in OFF timings - load disconnection

5.3.3 SENSE timings

Figure 25 shows the timing during the settling of $t_{sIS(ON)}$ and disabling of $t_{sIS(OFF)}$ for the SENSE function, including load change scenarios, as a proper signal cannot be established until the load current stabilizes, hence prior to t_{ON}.

$$t_{sIS(DIAG)} = t_{sIS(ON)} + t_{ON}$$

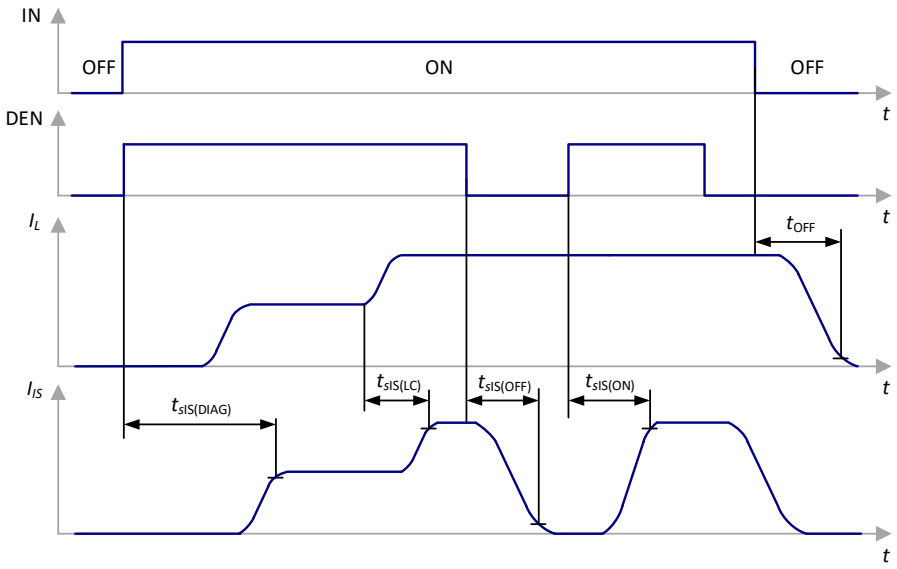
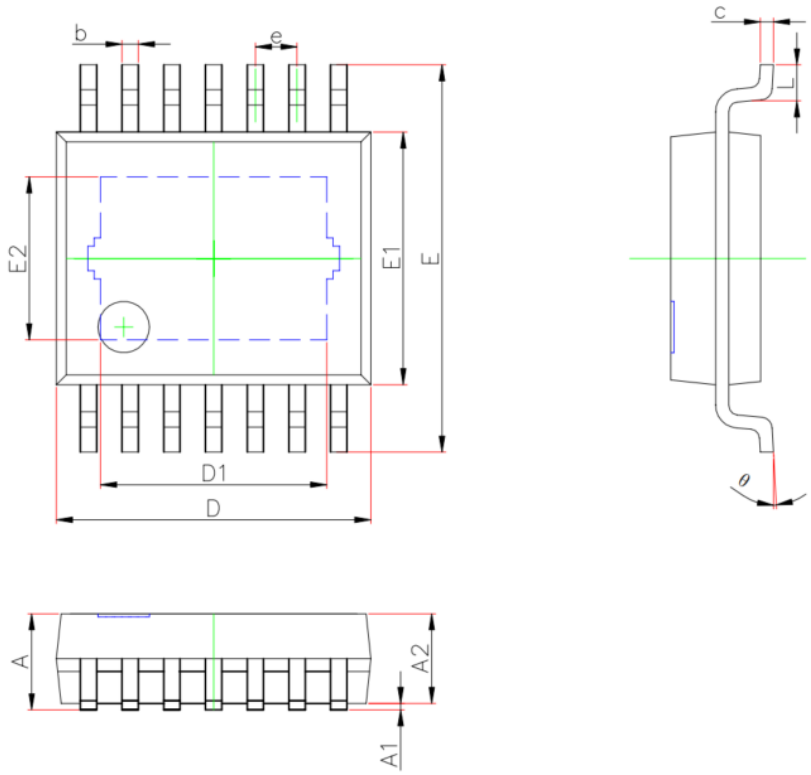


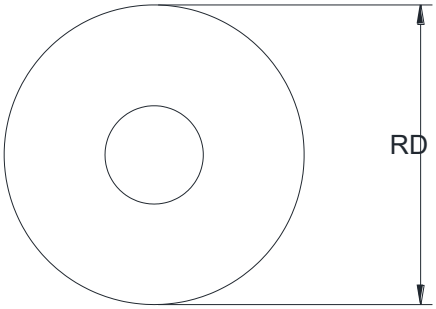
Figure 25. SENSE settling/disabling timing

6. Package Information

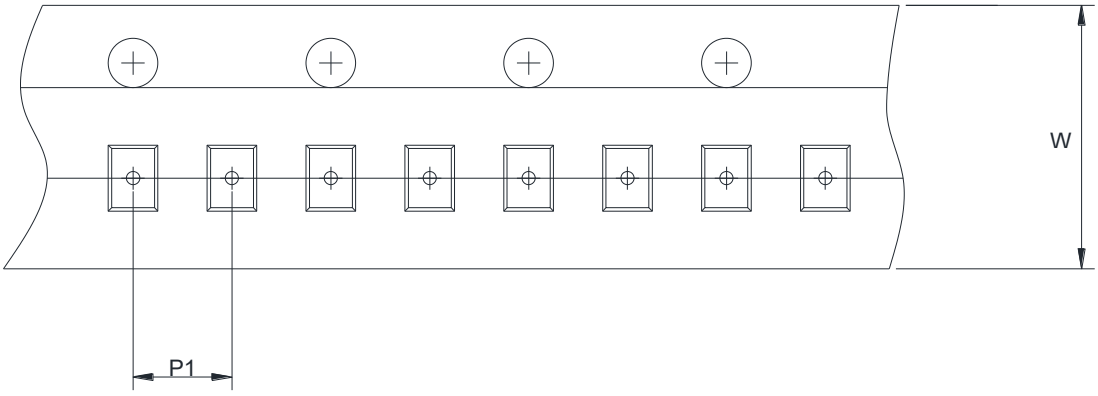


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.650	0.053	0.065
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.200	0.300	0.008	0.012
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.4216	3.6216	0.135	0.143
E	6.050	6.200	0.238	0.244
E1	3.800	4.000	0.150	0.157
E2	2.440	2.640	0.096	0.104
e	0.6500(BSC)		0.026(BSC)	
L	0.400	0.900	0.016	0.035
θ	0°	8°	0°	8°

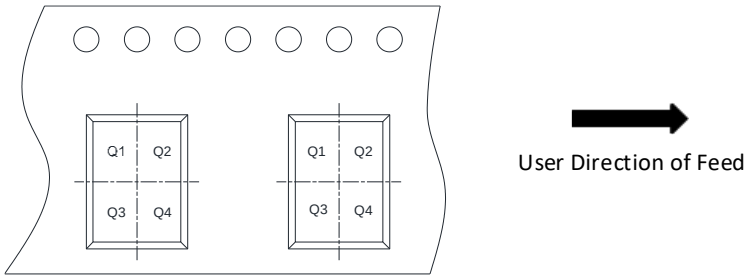
7. Tape and Reel Information



Reel Dimension



Tape Dimensions



Quadrant Assignments for PIN1 Orientation

Table 6 Tape dimensions

RD	Reel dimension	13inch
W	Overall width of the carrier tape	12mm
P1	Pitch between successive cavity centers	8mm
Pin1	Pin1 quadrant	Q1

8. Order Information

Order Number	Package	MSL Rating	Packing	Shipping	Environmental
CPSQ54D20BR	SSOP-14 4.9mm x 3.9mm	MSL3	Tape and Reel	4000ea/Reel	RoHS

9. Important Notice

ConvenientPower Semiconductor reserves the right to modify, improve and terminate its products, service, documentation, etc. without advance notice. Customers are encouraged to contact ConvenientPower Semiconductor sales representative get the latest product information.

Without proper legal authorization, ConvenientPower Semiconductor products shall not be used for medical or military applications. ConvenientPower Semiconductor does not assume any liability of personal or property damages of any kind due to such applications.