Features

- **Exceeds Requirements of EIA-485 Standard**
- **Bus-Polarity Correction within 100 ms (t_{FS})**
- **Data Rate: 300 bps to 250 kbps**
- **Works with Two Configurations:**
  - **– Failsafe Resistors Only**
  - **– Failsafe and Differential Termination Resistors**
- **Up to 256 Nodes on a Bus (1/8 unit load)**
- **Wide Supply Voltage 3V to 5.5V**
- **SOIC-8 Package for Backward Compatibility**
- **Bus-Pin Protection:**
  - **– ±18 kV HBM protection**
  - **– ±13 kV IEC61000-4-2 Contact Discharge**
  - **– +4 kV IEC61000-4-4 Fast Transient Burst**

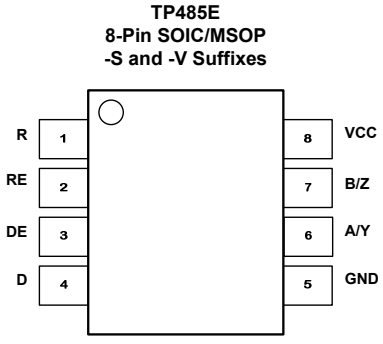
Applications

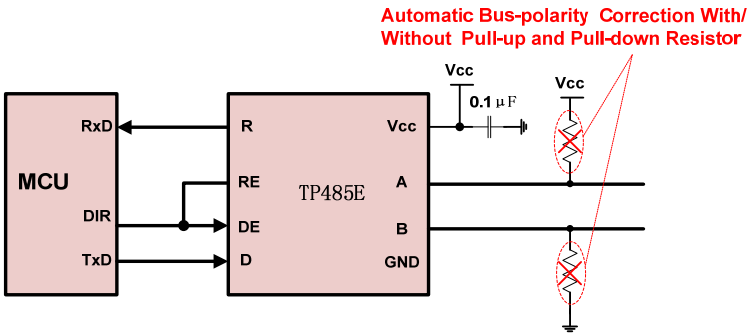
- E-Metering Networks
- Industrial Automation
- HVAC Systems
- Process Control
- DMX512-Networks
- Battery-Powered Applications

Description

The TP485E is a low-power RS-485 transceiver with automatic bus-polarity correction and transient protection. Upon hot plug-in, the device detects and corrects the bus polarity within the first 100 ms of bus idling. On-chip transient protection protects the device against IEC61000 ESD and EFT transients. This device has robust drivers and receivers for demanding industrial applications. The bus pins are robust to electrostatic discharge (ESD) events, with high levels of protection to Human-Body Model (HBM), Air-Gap Discharge, and Contact Discharge specifications. The device combines a differential driver and a differential receiver, which operate together from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex(two-wire bus) communication. The device features a wide common-mode voltage range making the device suitable for multi-point applications over long cable runs. The TP485E is available in both SOIC-8 and MSOP-8 package, and is characterized from –40°C to 125°C.

Pin Configuration (Top View)





Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP485E	TP485E-SR	8-Pin SOIC	Tape and Reel, 4,000	TP485E
TP485E	TP485E-VR	8-Pin MSOP	Tape and Reel, 3,000	TP485E

DRIVER PIN FUNCTIONS

INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
NORMAL MODE				
H	H	H	L	Actively drives bus High
L	H	L	H	Actively drives bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drives bus High
POLARITY-CORRECTING MODE(1)				
H	H	L	H	Actively drives bus Low
L	H	H	L	Actively drives bus High
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	L	H	Actively drives bus Low

(1) The polarity-correcting mode is entered when $V_{ID} < V_{IT-}$ and $t > t_{FS}$ and DE = low. This state is latched when /RE turns from Low to High.

RECEIVER PIN FUNCTIONS

DIFFERENTIAL INPUT	ENABLE	OUTPUT	DESCRIPTION
$V_{ID} = V_A - V_B$	/RE	R	
NORMAL MODE			
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle Bus	L	?	Indeterminate bus state
POLARITY-CORRECTING MODE(1)			
$V_{IT+} < V_{ID}$	L	L	Receive valid bus Low
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	H	Receive polarity corrected bus High
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle Bus	L	?	Indeterminate bus state

(1) The polarity-correcting mode is entered when $V_{ID} < V_{IT-}$ and $t > t_{FS}$ and DE = low. This state is latched when /RE turns from Low to High.

Absolute Maximum Ratings

V_{DD} to GND.....-0.3V to +7V

Input Voltages

DI, DE, RE.....-0.3V to (VCC + 0.3V)

Input/Output Voltages

A/Y, B/Z, A, B, Y, Z.....-15V to +15V

A/Y, B/Z, A, B, Y, Z (Transient Pulse Through 100Ω,

Note 1)..... ±100V

RO..... -0.3V to (VCC +0.3V)

Short Circuit Duration

Y, Z.....Continuous

ESD Rating.....See Specification Table

Recommended Operating Conditions Note 2

Supply Voltage.....3V to 5.5V

Temperature Range.....-40°C to +125°C

Bus Pin Common Mode Voltage Range .....-8V to +13V

Thermal Resistance, ΘJA (Typical)

8-Pin SOIC Package .....158°C/W

8-Pin MSOP Package .....210°C/W

Maximum Junction Temperature (Plastic Package) .....+150°C

Maximum Storage Temperature Range ..... -65°C to +150°C

Note 1: Tested according to TIA/EIA-485-A, Section 4.2.6 (±100V for 15μs at a 1% duty cycle).

Note 2: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Electrical Characteristics

Test Conditions: VCC = 5V, Over operating free-air temperature range(unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$\|V_{OD}\|$	Driver differential-output voltage magnitude	RL = 60 Ω	See Figure 1B		2.6		V
		RL = 54 Ω with V_A or V_B from –7 to +12 V, V_{CC} = 5V (RS-485)	See Figure 1A	2.4	2.6		
		RL = 54 Ω with VA or VB from -7 to +12 V, VCC = 3V (RS-485)		1.4	1.5		
		RL = 100 Ω(RS-422)			3		
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential-output voltage	RL = 54 Ω, CL=50pF	See Figure 1A	-0.01	0	0.03	V
$V_{OC(SS)}$	Steady-stage common-mode output voltage	Center of two 27-Ω load resistors	See Figure 1A	Vcc/2-0.2	V_{CC}/2	Vcc/2+0.2	V
ΔV_{OC}	Change in differential driver common-mode output voltage			-0.2	0	0.2	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage				500		
C_{OD}	Differential output capacitance				8		pF
V_{IT+}	Positive-going receiver differential-input voltage threshold				75		mV
V_{IT-}	Negative-going receiver differential-input voltage threshold				-75		mV
V_{HYS} (1)	Receiver differential-input voltage threshold hysteresis ($V_{IT+} – V_{IT–}$)				150		mV
V_{OH}	Receiver high-level output voltage	I_{OH}= -8 mA		4.64	4.65	4.66	V
V_{OL}	Receiver low-level output voltage	I_{OL}= 8 mA		0.22	0.23	0.24	V
I_I	Driver input, driver enable and receiver enable input current			0.012	0.017	0.022	μA
I_{OZ}	Receiver high-impedance output current	VO = 0 V or VCC, /RE at VCC		-0.003	0	0.01	μA
$\|I_{OS}\|$	Driver short-circuit output current	$\|I_{OS}\|$ with V_A or V_B from –7 to +12 V			80	107	mA
I_I	Bus input current(driver disabled)	V_{CC} = 4.5 to 5.5 V or V_{CC} = 0 V, DE at 0 V	VI= 12 V		55	65	μA
			VI= -7 V	-63	-50		
I_{CC}	Supply current(quiescent)	Driver and receiver enabled	DE = V_{CC}, /RE = GND, No LOAD	624	680	771	μA
		Driver enabled, receiver disabled	DE = V_{CC}, /RE = V_{CC}, No LOAD	269	278	290	
		Driver disabled, receiver enabled	DE = GND, /RE = V_{CC}, No LOAD	458	500	546	
		Driver and receiver disabled	DE = GND, /RE = V_{CC}, D= V_{cc} No LOAD	0.017	0.15	0.177	
	Supply current(dynamic)	See					

Switching CHARACTERISTICS

.3.3ms > bit time> 4μs(unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
t_r, t_f	Driver differential-output rise and fall times	RL = 54 Ω, CL=50pF	See Figure 2		620		ns
t_{PHL}, t_{PLH}	Driver propagation delay				340		
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				23		
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 3		250		ns
t_{PHZ}, t_{PLZ}	Driver enable time	Receiver enabled			562		ns
		Receiver disabled			562		
RECEIVER							
tr, tf	Receiver output rise and fall times	CL=15 pF	See Figure 5		12.4		ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				960		
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				40		
t_{PHZ}, t_{PLZ}	Receiver disable time				7		ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 6		70		ns
		Driver disabled	See Figure 6		989		
t_{FS}	Bus failsafe time	Driver disabled	See Figure 6	88	100	107	ms

Test Circuits and Waveforms

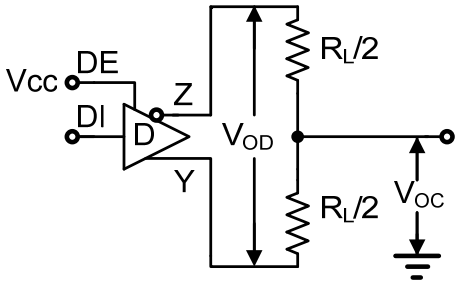


FIGURE 1A. VOD AND VOC

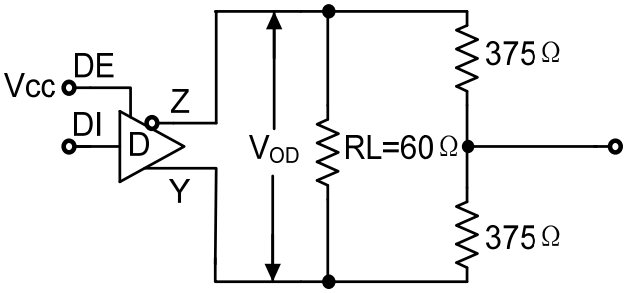


FIGURE 1B. VOD WITH COMMON MODE LOAD

FIGURE 1. DC DRIVER TEST CIRCUITS

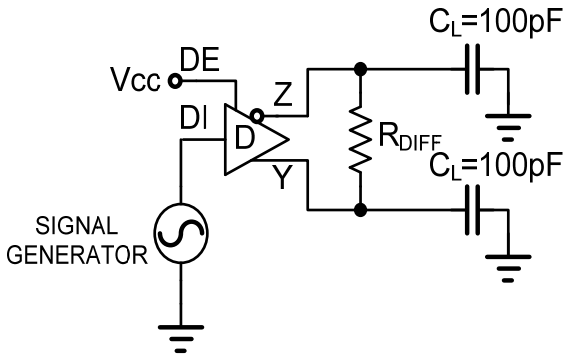


FIGURE 2A. TEST CIRCUIT

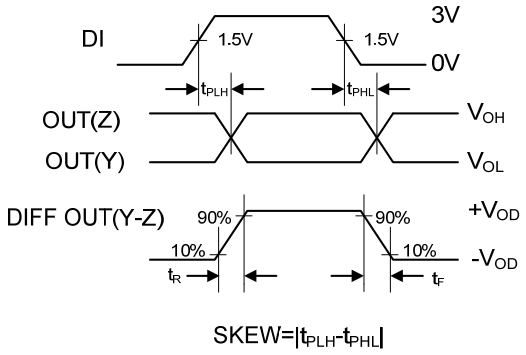
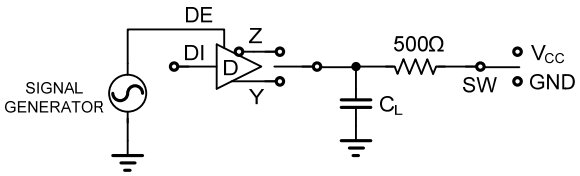


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	RE	DI	SW	CL (pF)
tHZ	Y/Z	X	1/0	GND	15
tLZ	Y/Z	X	0/1	VCC	15
tZH	Y/Z	0 (Note 9)	1/0	GND	100
tZL	Y/Z	0 (Note 9)	0/1	VCC	100
tZH(SHDN)	Y/Z	1 (Note 12)	1/0	GND	100
tZL(SHDN)	Y/Z	1 (Note 12)	0/1	VCC	100

FIGURE 3A. TEST CIRCUIT

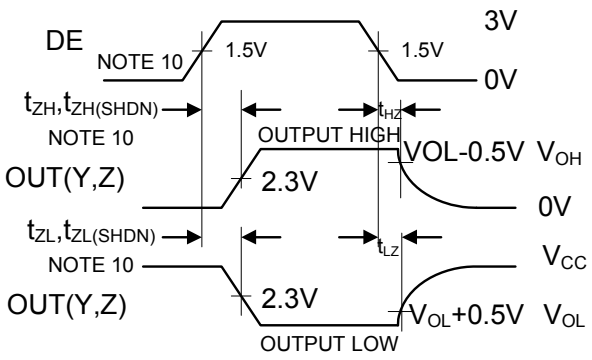


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

Test Circuits and Waveforms(continue)

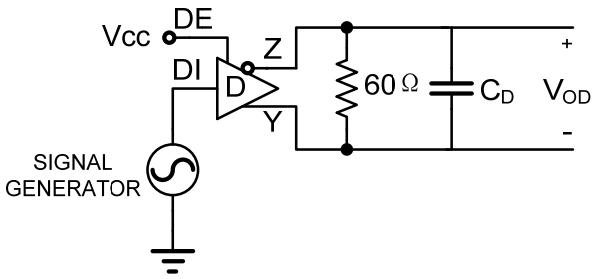


FIGURE 4A. TEST CIRCUIT

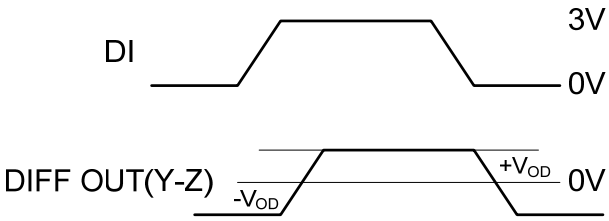


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. DRIVER DATA RATE

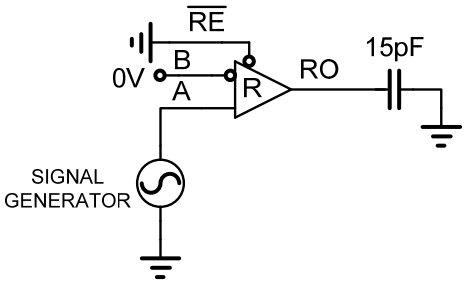


FIGURE 5A. TEST CIRCUIT

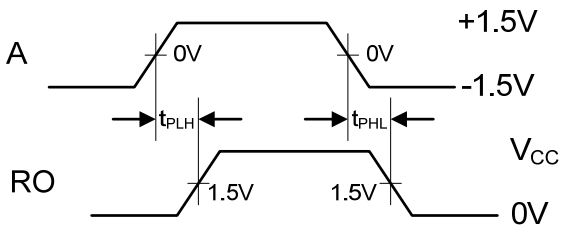
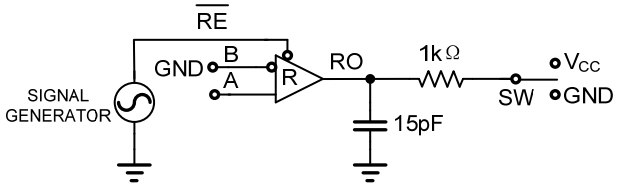


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER PROPAGATION DELAY AND DATA RATE



PARAMETER	DE	A	SW
tHZ	0	+1.5V	GND
tLZ	0	-1.5V	VCC
tZH(Note 10)	0	+1.5V	GND
tZL(Note 10)	0	-1.5V	VCC
tZH(SHDN)(Note 13)	0	+1.5V	GND
tZL(SHDN)(Note 13)	0	-1.5V	VCC

FIGURE 6A. TEST CIRCUIT

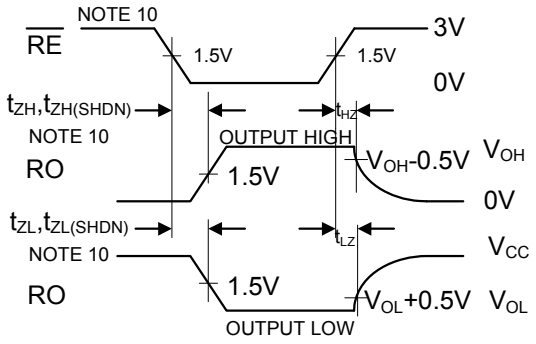


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. RECEIVER ENABLE AND DISABLE TIMES

Detailed Description

The TP485E half-duplex RS-485 transceiver features automatic polarity correction on the RS-485 bus lines. This device also includes fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when connected to a terminated transmission line with all drivers disabled. Hot-swap capability on the enable inputs allows line insertion without erroneous data transfer and controlled slew-rate drivers minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 250 kbps. The TP485E features short-circuit current limits on the driver and receiver outputs and thermal shutdown circuitry to protect against excessive power dissipation.

Automatic Polarity Detection

The TP485E is designed to detect and correct installation-based connections on RS-485 lines. With the driver disabled, internal detection circuitry samples the voltages at the A and B inputs during an idle period (100ms, typ) and configures the driver and receiver for the detected polarity. Polarity is swapped only when $|V_A - V_B| > 75mV$ for the idle period. The A/B line polarity can be defined by a pull up and pull down resistor pair on the A/B lines, for example, in the RS-485 Half duplex master terminal (see the *Typical Operating Circuit*). When the polarity is normal, A is the non inverting receiver input/driver output and B is the inverting input/output. When the polarity is inverted, A is the inverting input/output and B is the non inverting input/output.

To allow the bus to define A/B polarity, connect one pull up/pull down resistor pair to the bus to set the bus status during the idle periods. It is preferable to locate the resistor pair in the bus master, as shown in Figure 7.

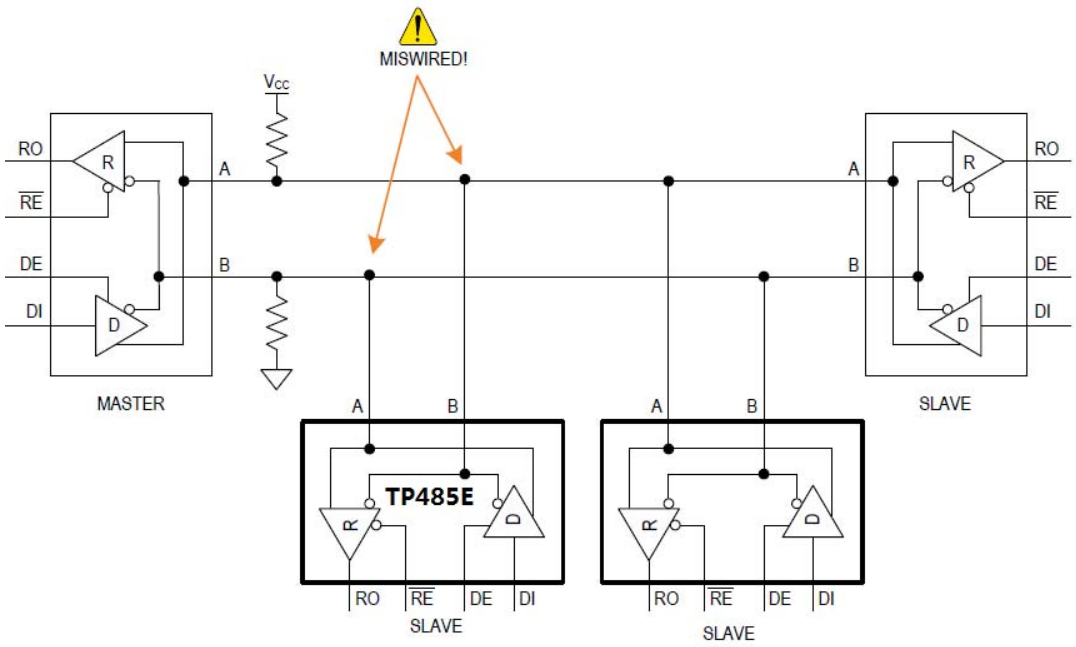


Figure 7. Polarity Definition

Hot Plug Function

When a piece of equipment powers up, there is a period of time where the processor or ASIC driving the RS-485 control lines (DE, RE) is unable to ensure that the RS-485 Tx and Rx outputs are kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up may crash the bus. To avoid this scenario, the TP485E devices incorporate a “Hot Plug” function. Circuitry monitoring V_{CC} ensures that, during power-up and power-down, the Tx and Rx outputs remain disabled, regardless of the state of DE and RE, if V_{CC} is less than ~2.5V. This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states.

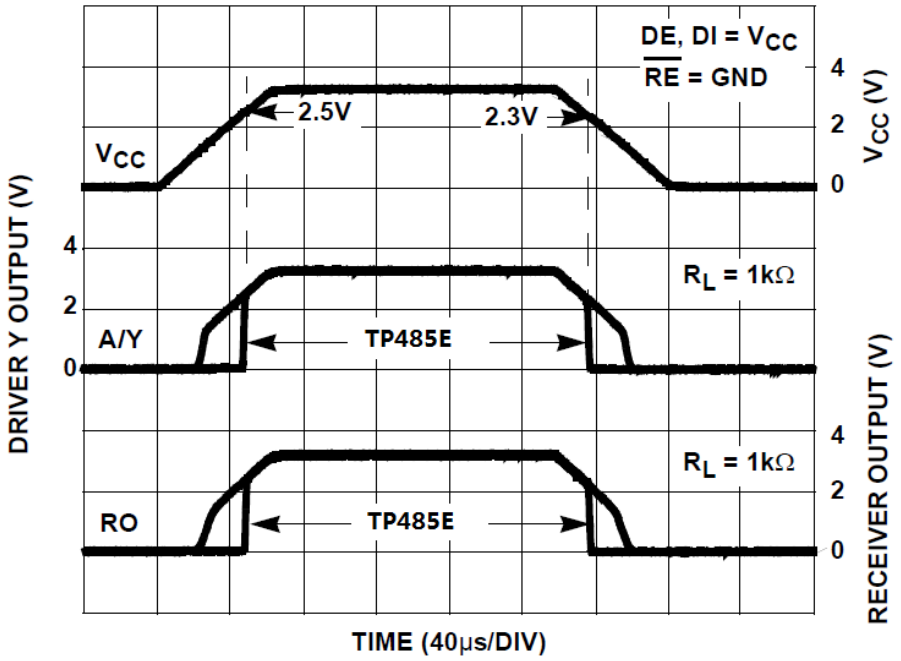


FIGURE 8. HOT PLUG PERFORMANCE (TP485E) vs Competitor WITHOUT HOT PLUG CIRCUITRY

ESD Protection

All pins on these devices include class 3 (>7 kV) Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±18 kV HBM and ±13 kV (1/2 duplex) IEC61000-4-2. The RS-485 pins are particularly vulnerable to ESD strikes because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, and without degrading the RS-485 common mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (e.g., transient suppression diodes), and the associated, undesirable capacitive load they present.

Transient Protection

The bus terminals of the TP485E transceiver family possess on-chip ESD protection against ±18 kV HBM and ±13 kV IEC61000-4-2 contact discharge. The International Electrotechnical Commision (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, CS, and 78% lower discharge resistance, RD of the IEC model produce significantly higher discharge currents than the HBM model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method. Although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.

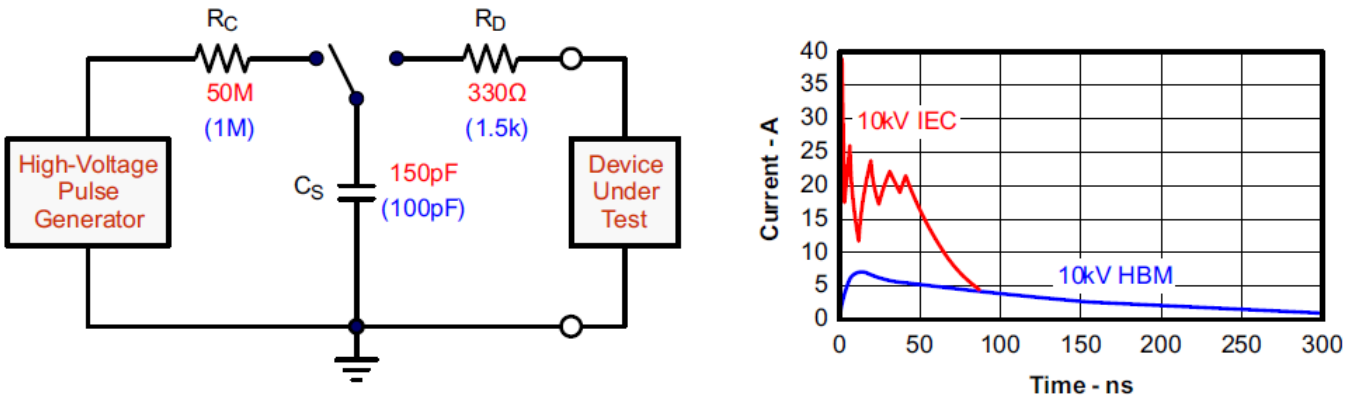


Figure 9. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients. Figure 9 suggests two circuit designs providing protection against short and long duration surge transients, in addition to ESD and Electrical Fast Transients (EFT) transients. Table 1 lists the bill of materials for the external protection devices.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuits switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems. Figure 10 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. In the diagram on the left of Figure 10, the tiny blue blip in the bottom left corner represents the power of a 10-kV ESD transient, which already dwarfs against the significantly higher EFT power spike, and certainly dwarfs against the 500-V surge transient. This type of transient power is well representative of factory environments in industrial and process automation. The diagram on the fright of Figure 10 compares the enormous power of a 6-kV surge transient, most likely occurring in e-metering applications of power generating and power grid systems, with the aforementioned 500-V surge transient.

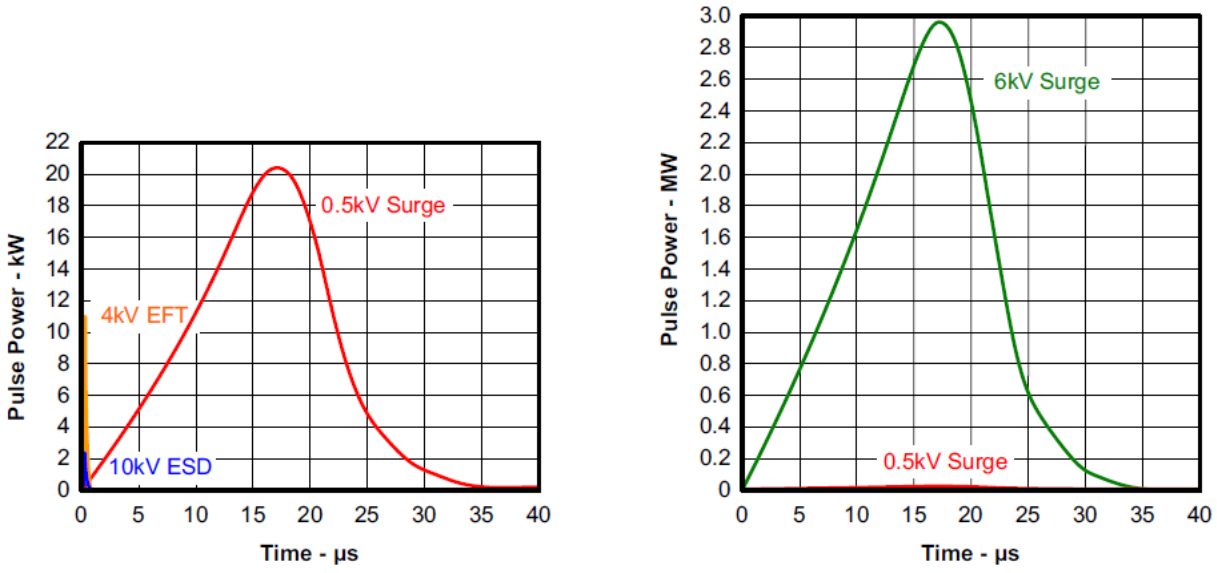


Figure 10. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, high-energy content is signified by long pulse duration and slow decaying pulse Power The electrical energy of a transient that is dumped into the internal protection cells of the transceiver is converted into thermal energy. This thermal

energy heats the protection cells and literally destroys them, thus destroying the transceiver. Figure 11 shows the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.

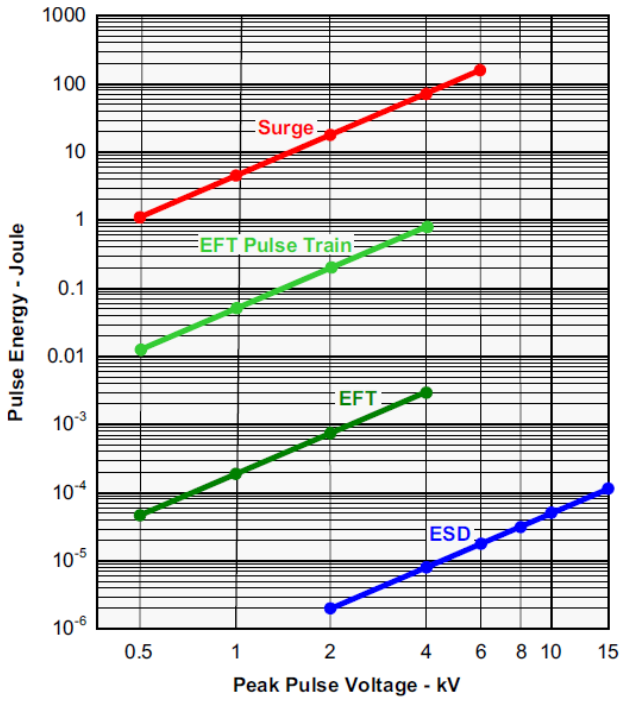


Figure 11. Comparison of Transient Energies

Table 1. Bill of Materials

Device	Function	Order Number	Manufacturer
485	5-V, 250-kbps RS-485 Transceiver	TP485E	3PEAK
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1, TBU2	Bidirectional.	TBU-CA-065-200-WH	Bourns
MOV1, MOV2	200mA Transient Blocking Unit 200-V, Metal-Oxide Varistor	MOV-10D201K	Bourns

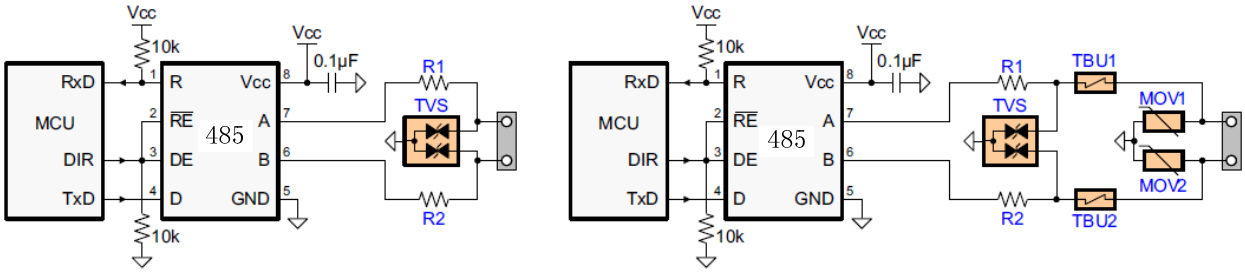


Figure 12. Transient Protections Against ESD, EFT, and Surge Transients

The left circuit shown in Figure 12 provides surge protection of ≥ 500-V transients, while the right protection circuits can withstand surge transients of 5 kV.

Typical Performance Characteristics

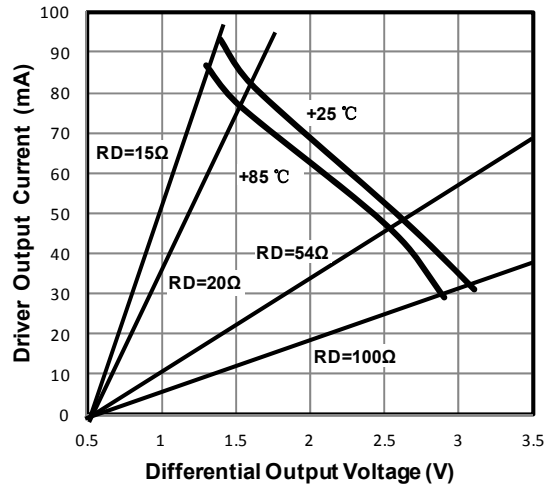


FIGURE 13. DRIVER OUTPUT CURRENT vs VOLTAGE DIFFERENTIAL OUTPUT VOLTAGE

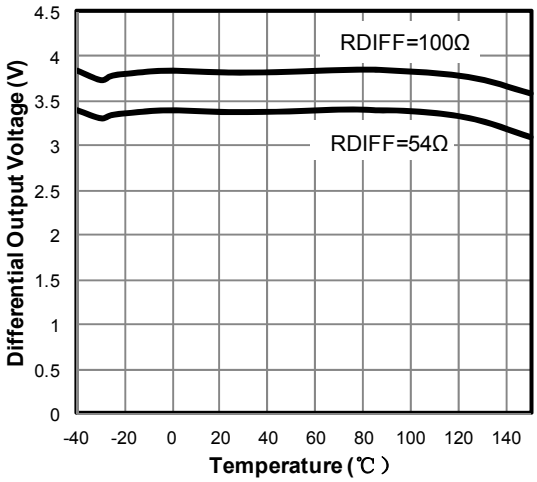


FIGURE 14. DRIVER DIFFERENTIAL OUTPUT vs TEMPERATURE

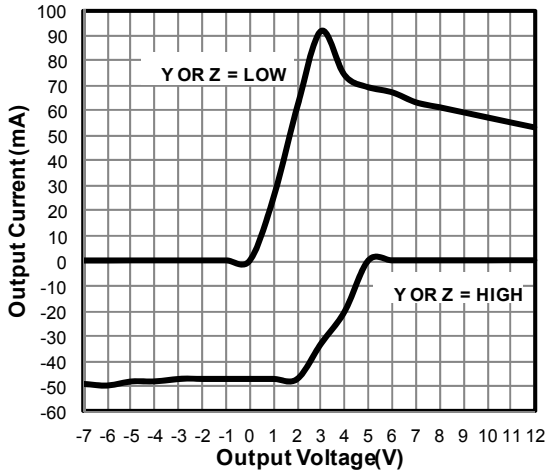


FIGURE 15. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

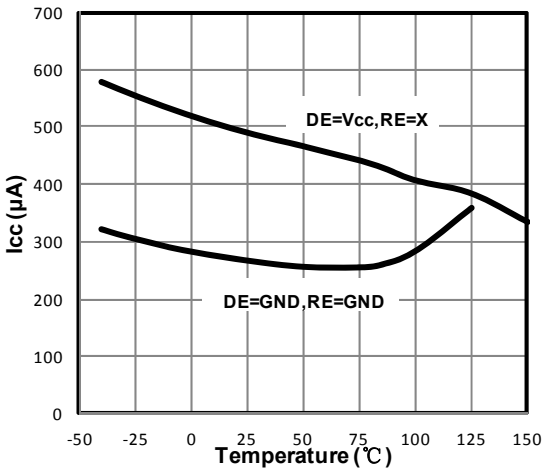


FIGURE 16. SUPPLY CURRENT vs TEMPERATURE

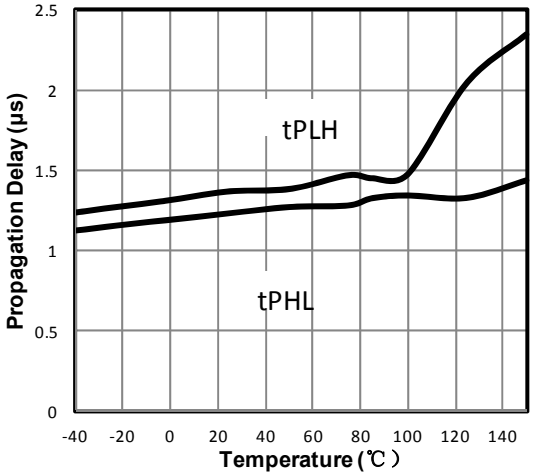


FIGURE 17. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE

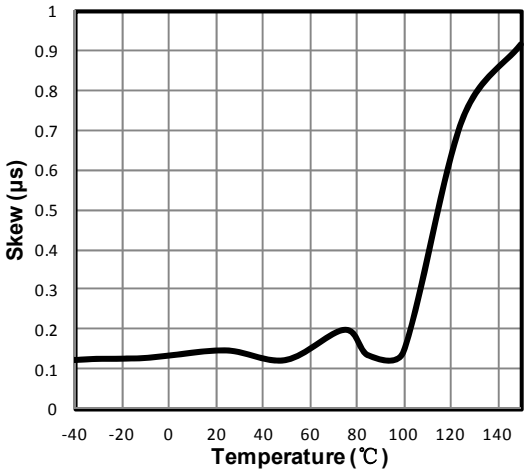


FIGURE 18. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE

Typical Performance Curves

V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified.

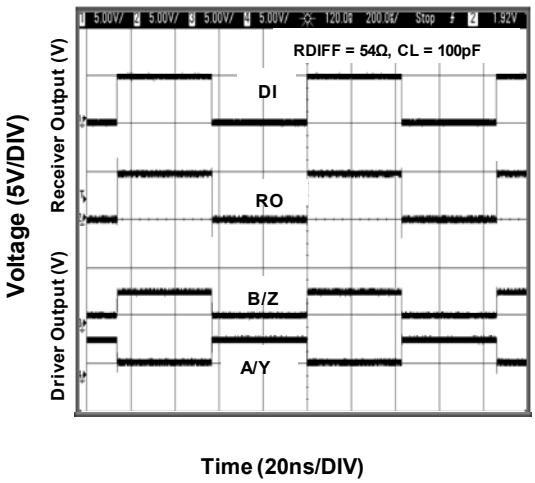
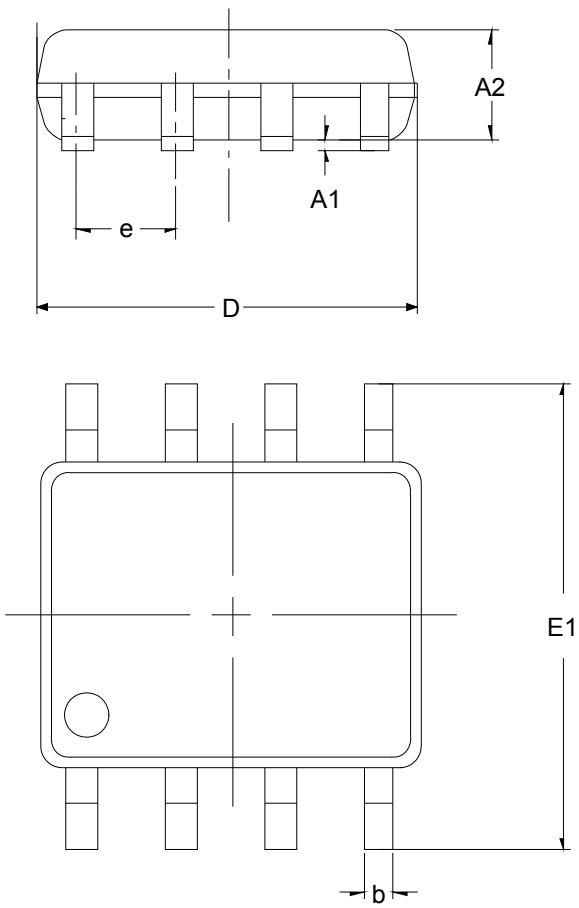


FIGURE 19. DRIVER AND RECEIVER WAVEFORMS

Package Outline Dimensions

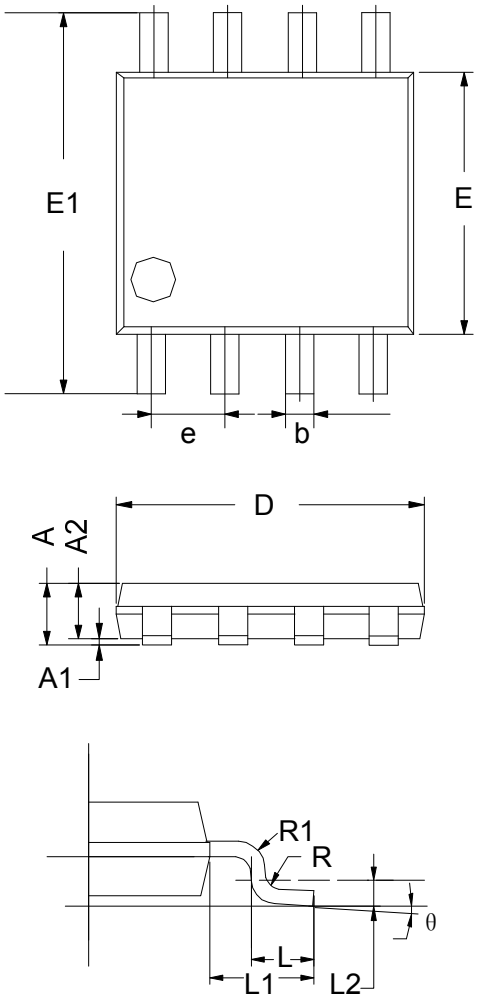
SO-8 (SOIC-8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Outline Dimensions

MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°