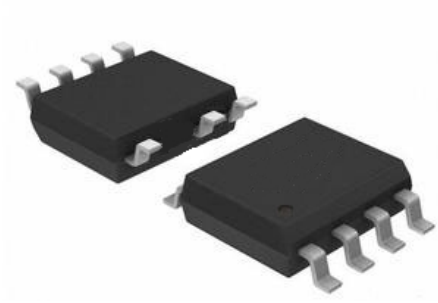
MORNSUN®

SCM1703A Opto-coupler Feedback Controller

Features

- Built-in Loop Compensation Circuit
- 700V Startup Switch
- Built-in Line Compensation
- Wide VDD Range tolerates Small Bias Capacitor
- Advanced Capacitive loading with Self-Powered during Startup
- Output Over Voltage Protection
- Output Short Circuit Protection
- Fault-protection FA PIN
- Fault-protected CS PIN
- Over Temperature Protection

Package



Product package: SOP-7.

Please see “Ordering Information” for details

Applications

- AC-DC flyback converter designs in the 5W max power range using opto-coupler feedback.

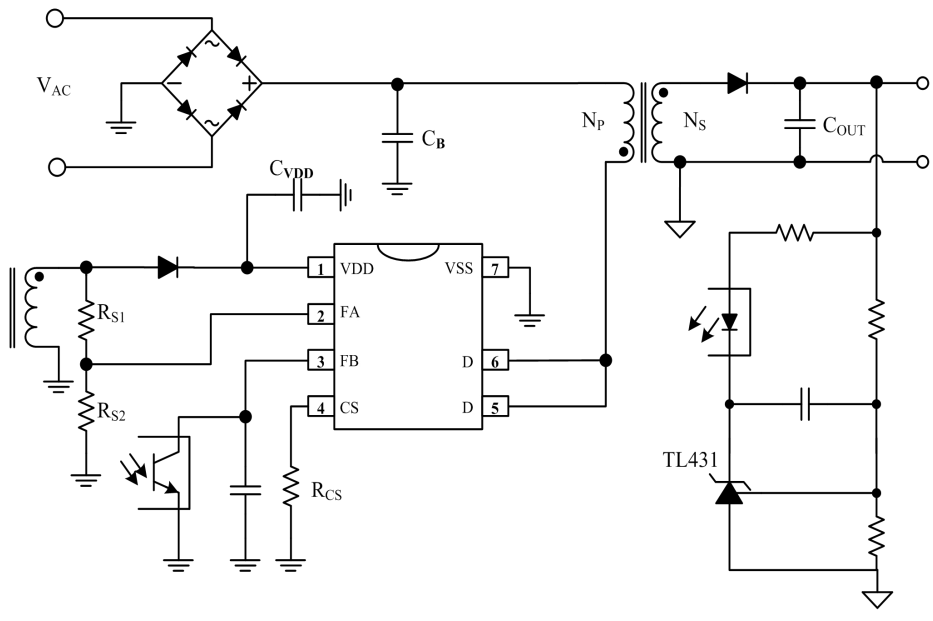
Functional Description

The SCM1703A controller for isolated flyback power supply designs provides a voltage control using an opto-coupler feedback to improve transient response time to large load steps. Current control is accomplished through Primary Side Regulation (PSR) techniques. This device processes information from opto-coupler feedback and an auxiliary flyback winding for precise high-performance control of output voltage and current.

A combination of an internal 700 Volt startup switch, dynamically controlled operating states and a tailored modulation profile support the ultra-low standby power without sacrifices regarding startup time or output transient response time. The chip integrated loop compensation circuit provides precise high-performance control of output voltage and great output transient response.

SCM1703A integrates functions that provide protection in case of output over voltage, FA pin fault, CS pin fault, output short circuit and over temperature in addition to other protection, all easily meeting all safety requirements.

Typical application circuit



Absolute Maximum Ratings

Test conditions: Free-air, normal operating temperature range (unless otherwise specified), voltage reference is ground.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Bias Supply Voltage, VDD	V_{VDD}		22	V
Input Voltage Range, VIN	V_{IN}		700	V
Voltage Range	V_{FB},V_{CS},V_{FA}	-0.6	6	
Operation junction temperature	T_J	-40	150	℃
Storage Temperature	T_{STG}	-40	150	
Lead Temperature 0.6mm from Case	Soldering for 10 seconds		260	
Electro Static Discharge (ESD) rating	Human Body Model（HBM）	-2000	2000	V
	Charged Device Model（CDM）	-1000	1000	

Important: Exposure to absolute-maximum-rated conditions for extended periods may severely affect device reliability, stress levels exceeding the “Absolute Maximum Ratings” may result in permanent damage. Currents specified are positive when flowing into and negative flowing out of specified terminals.

Recommended Operating Conditions

Test conditions: Free-air, normal operating temperature range (unless otherwise specified), V_{VDD}=12V，GATE=no load.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Bias-supply operating voltage	V_{VDD}	9	20	V
VDD bypass capacitor	C_{VDD}	0.047	20	uF
Operating Frequency	F_{SW}	68	110	kHz
Operating junction temperature	T_J	-40	125	℃

Electrical Characteristics

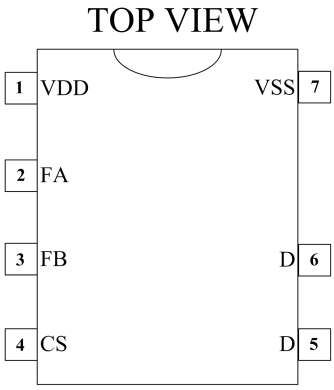
Test conditions: Free-air, normal operating temperature range (unless otherwise specified), V_{VDD}=12V，GATE=no load.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-voltage start up						
I_{ST}	I_{STL}：Startup Current, Low Limit	V_D=40V，V_{VDD}=0V，start sate, current from VDD PIN	200		550	uA
	I_{STH}：Startup Current, High Limit	V_D=40V，V_{VDD}=5V，current from VDD PIN	0.8		4	mA
I_{STLKG}	Leakage Current at D PIN	V_D=400V，run state, T_J=25℃		1		uA
Bias supply input						
I_{VDD_STAT}	Supply Current, run state	I_{GATE}=0，FB floating	400	550	700	uA
Under-voltage lockout						
V_{VDD_ON}	VDD Turn-on Threshold	VDD low to high	15	16.25	17.5	V
V_{VDD_OFF}	VDD Turn-off Threshold	VDD high to low	7.8	8.4	9	V
FA pin						
V_{FANC}	Negative Clamp Level	IFA = –300μA (in mV below ground)		-35		mV
CS pin						
R_{LC}	Internal Line-compensation Resistor			2.4		kΩ
V_{CST_MAX}	Maximum CS Threshold Voltage		0.77	0.8	0.83	V
V_{CST_MIN}	Minimum CS Threshold Voltage		0.26	0.27	0.28	V
K_{AM}	AM-control Ratio	V_{CST_MAX}/V_{CST_MIN}		3		V/V
K_{LC}	Line-compensation Current Ratio	I_{FA} = –300μA, I_{FA}/current out of CS pin		2/23		A/A
K_{DE}	The Maximum Ratio of T_{dem}/T	V_{FA}=2V		0.5		s /s
T_{CS_LEB}	Leading-edge Blanking Time	DRV output duration, (V_G=8V)，V_{CS}=1V		228		ns
FB pin						
V_{FB_OPEN}	FB Open Voltage			5.4		V
Z_{FB_IN}	FB Input Resistance			10.5		kΩ
I_{FB_SHORT}	FB Short to Ground Current	FB short-to-ground		0.51		mA
Protection						
V_{OVP}	Output Overvoltage Protection Threshold	At FA input, T_J=25℃		4.32		V
V_{CSF}	CS Fault Protection Threshold	At CS input		1.60		V
T_{J_STOP}	Thermal Shutdown Temperature	Internal junction temperature		155		℃
$T_{J\_RESTART}$	Restart Temperature	Internal junction temperature		98		℃
Timing						
$F_{SW\_STARTUP}$	Startup Frequency		17.8	20.9	24.0	kHz
F_{SW_MIN}	Minimum Switching Frequency	V_{FB}=1V	595	700	805	Hz
T_{PD}	Maximum Turn-on Time	CS short-to-ground	10.149	11.94	13.731	us
$T_{VDD\_STOP\_MAX}$	Protection Delay Time	FA、CS input protection、over temperature or V_{FAS}=V_{OVP}		6		T_{SW}
T_{ON_MAX}	Maximum Self Power-supply Time			3072		T_{SW}

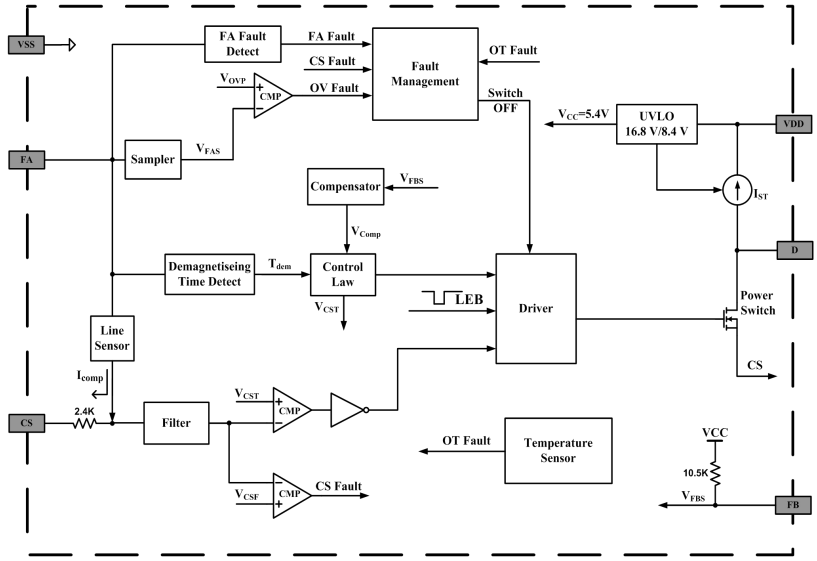
Internal MOSFET						
R_{DS_ON}	Internal MOSFET R_{DS_ON}	V_{GS} =10V, ID =0.5A	-	-	16	Ω

NOTE ： T_{SW} is switching period.

Internal Block Diagram



Pin Configuration



Pin Description

PIN NO.	NAME	I/O	DESCRIPTION
1	VDD	P	The VDD input pin is the bias-supply of the controller. It requires a bypass capacitor to GND.
2	FA	I	The FA input provides the demagnetization timing feedback to the controller limiting frequency, controlling constant-current operation and providing output overvoltage detection. It also detects AC mains input voltage, for primary peak current compensation. A voltage divider connected from the auxiliary winding to GND feeds this pin. The upper resistor value of this divider programs the threshold of AC mains run and stop, also factoring in the line compensation at the CS pin.
3	FB	I	The feedback (FB) input receives its current signal from the opto-coupler's output transistor. The voltage at this resistor directly drives the control law function, which determines the switching frequency and the switching currents peak amplitude.
4	CS	I	The current sense (CS) input is connected to ground via a current sense resistor. The resulting voltage monitors and controls the primary peak current.
5	D	M	The high voltage (D) pin may be connect directly to the transformer, providing the charge current to the VDD capacitor C_{VDD} for starting up the power supply.
6			
7	VSS	P	The VSS ground (GND) pin is both, the controller reference pin and the drive outputs low-side return. Special care must be taken to keep all AC-decoupling capacitors returns as close as possible to this pin and avoiding any lengthy common traces with analog signal return paths.

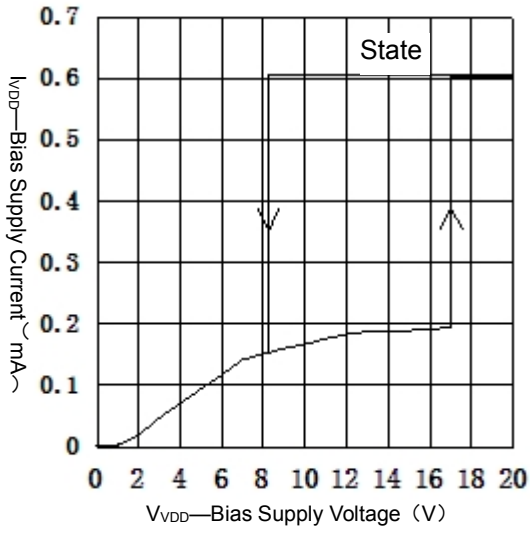


Figure 1 Bias Supply Current vs. Bias Supply Voltage

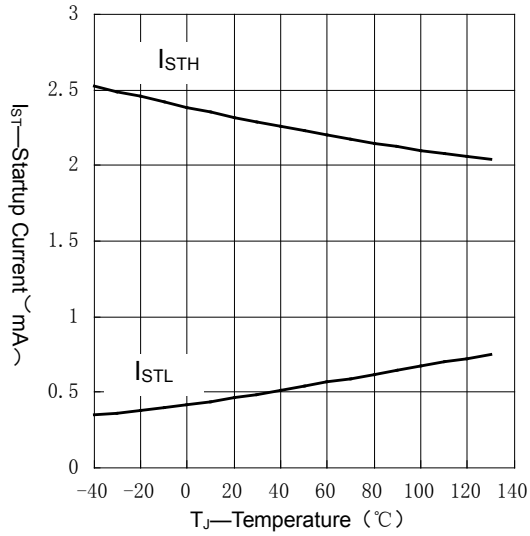


Figure 2 Startup Current vs. Temperature

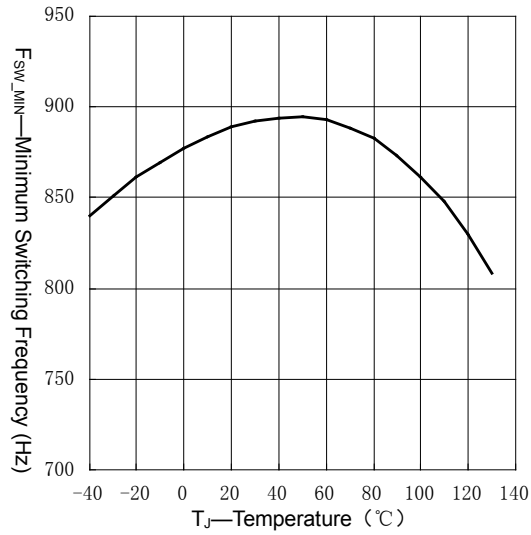


Figure 3 Minimum Switching Frequency vs. Temperature

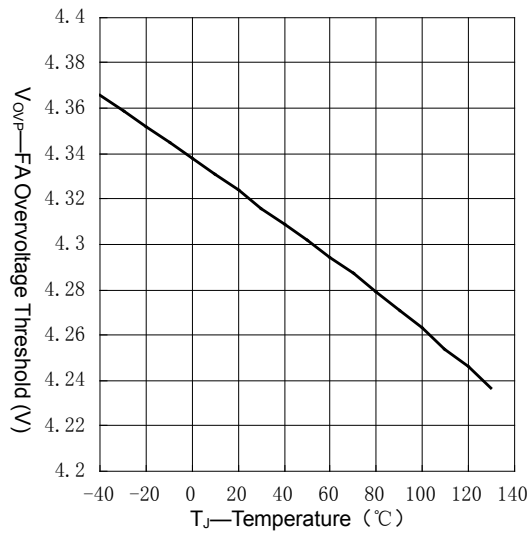


Figure 4 FA Overvoltage Threshold vs. Temperature

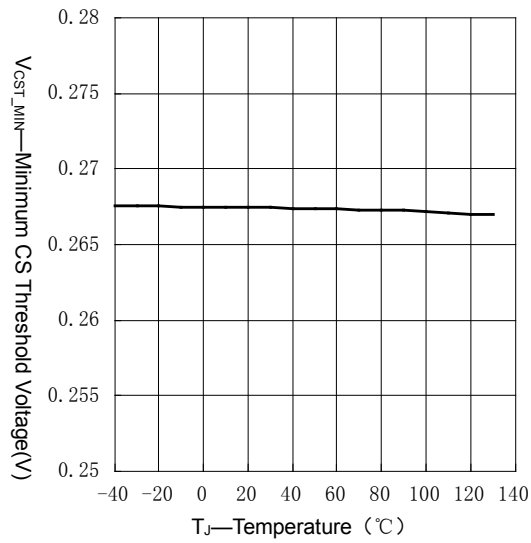


Figure 5 Minimum CS Threshold vs. Temperature

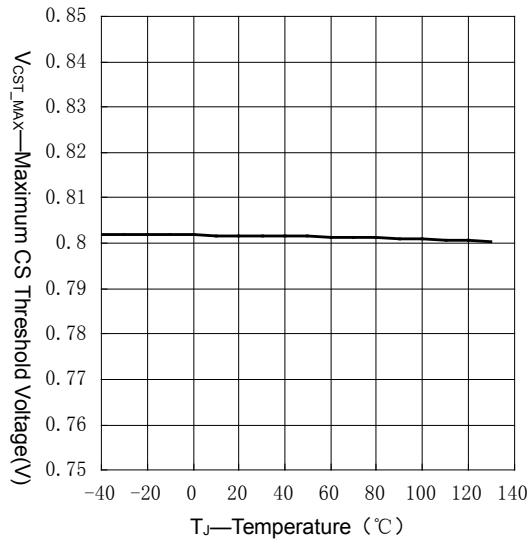


Figure 6 Maximum CS Threshold vs. Temperature

High Voltage Startup Operation

An internal high voltage startup switch is connected to the primary side of the transformer and continuously charges the VDD capacitor C_{VDD} from the voltage of the bulk capacitor C_B, see also figure 7. This start up switch acts like a current source by providing low limited current to the VDD capacitor C_{VDD}. under 2.4 Voltage of VDD. When VDD reaches the UVLO turn on threshold, the controller is enabled, the converter starts switching and the high-voltage startup switch continues charging the VDD capacitor C_{VDD} until the VDD voltage reaches 20.8V. The VDD voltage starts to drop once the controllers run state current becomes larger than the high limit of the startup current. The controller is self-powered and independent from the VDD voltage slope. The maximum self-powered on time of the supply is $T_{VDD\_STOP\_MAX}$ and self-power stops either when the converter output voltage reaches its target of V_{OUT_CV} or the converter enters into a protected state. For the values of I_{STL}、I_{STH}、V_{VDD_ON} and $T_{VDD\_STOP\_MAX}$, also refer to Electrical Characteristics.

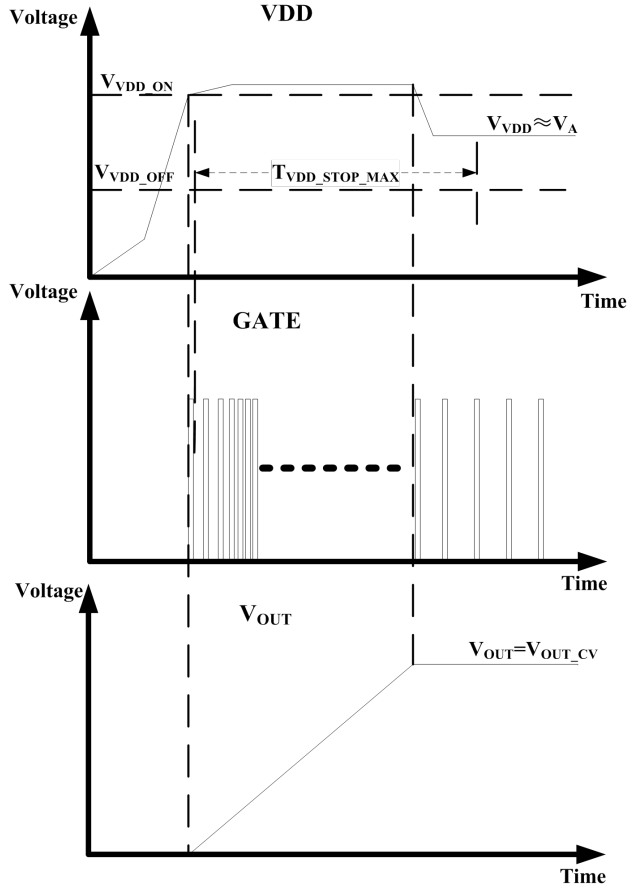


Figure 7 startup timing

Over Current point (constant current point) Design

The ratio (K_{DS}) between demagnetization time T_{DEM} and switching period T_{SW} is set within the SCM1703A controller. The secondary average output current I_{O_MAX} is determined by the primary peak current, the turns-ratio, the demagnetization time T_{DEM} and the switching period T_{SW}:

$$I_{O\_MAX} = \frac{1}{2} \cdot \frac{N_P}{N_S} \cdot K_{DS} \cdot \eta_{XFMR} \cdot I_{PEAK\_MAX} \qquad (1)$$

where
NP/NS is the transformer primary to secondary turns ratio
K_{DS} is the ratio of demagnetization time T_{DEM} and switching period T_{SW} (see electrical characteristics)
η_{XFMR} is the transformer efficiency at full power
I_{PEAK_MAX} is the maximum of primary peak current
The over current point design is modulated through N_P/N_S and I_{PEAK_MAX}
In CC mode, K_{DS} (the ratio of demagnetization time T_{DEM} and switching period T_{SW}) is set within the controller. The over current point is confirmed, once the parameters of the transformer and the maximum primary peak current are established.

$$I_{PEAK\_MAX} = \frac{V_{CST\_MAX}}{R_{CS}} \qquad (2)$$

Example：With a transformer core and winding loss of 5%, a primary to secondary leakage inductance of 1.5% and a bias power to output power ratio of 1.5%, the η_{XFMR} value at full power is approximately: η_{XFMR} = 1-0.05-0.035-0.015 = 0.9.
A 3W converter design with 5Vout has an over current capacity of 10% and the transformer primary to secondary turns ratio is 14. The current sense resistor is:

$$R_{CS} = \frac{V_{CST\_MAX}}{2I_{O\_MAX}} \cdot \frac{N_P}{N_S} \cdot K_{DS} \cdot \eta_{XFMR}$$
$$= \frac{0.8}{2 \times 0.66} \times 14 \times 0.5 \times 0.9 \qquad (3)$$
$$= 3.8\Omega$$

Modulation Mode

During CV regulation, the frequency and amplitude modulation modes are shown in figure 8, where I_{PP} and F_{SW} are normalized curves relative to the output of the error amplifier. The feedback signal FB is filtered by compensation filter and results in the output of the error amplifier. The value of the output of EA is approximately equal to the FB voltage in steady state. The controller limits the maximum switching frequency F_{SW_MAX} and the minimum switching frequency F_{SW_MIN} (see electrical characteristics). The recommended operating switching frequency range is between 68kHz and 110kHz and higher switching frequencies affect the converters efficiency and EMI performance. The maximum switching frequency is defined by the primary inductor and the primary peak current (see switching frequency design).

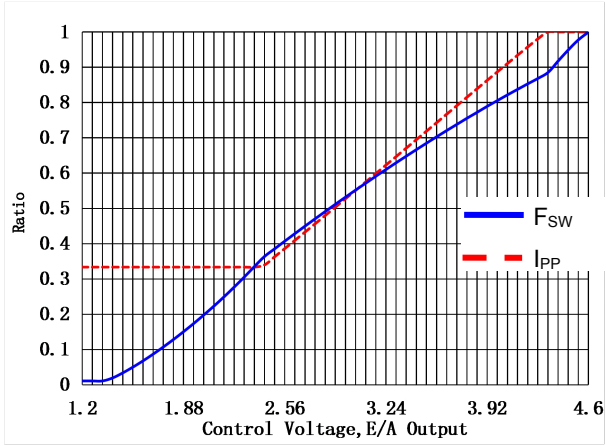


Figure 8 Frequency and Amplitude Modulation Modes（During CV Regulation）

Switching Frequency

Once the constant current and over current points are established, then both the maximum primary peak current I_{PEAK_MAX} and the over power point P_{O_MAX} are confirmed. The maximum switching frequency of the converter is calculated as follows:

$$F_{SW\_MAX} = \frac{2 \cdot P_{O\_MAX}}{L_M \cdot I^2_{PEAK\_MAX} \cdot \eta_{XFMR}} \qquad (4)$$

Modulate L_M to acquire F_{SW_MAX}, SCM1703A's maximum frequency is limited to 168kHz.

Line Sensor Compensation

The waveform of the auxiliary winding consists of three parts as shown in figure 9. First part is the MOSFET switch on time T_{ON}, where the voltage is $-V_{BULK}/N_{PA}$. Second part is demagnetization time T_{DEM}, the voltage is $(V_O+V_F)\ N_{AS}$. Third part is primary inductance and capacitance resonance time T_{RING}.

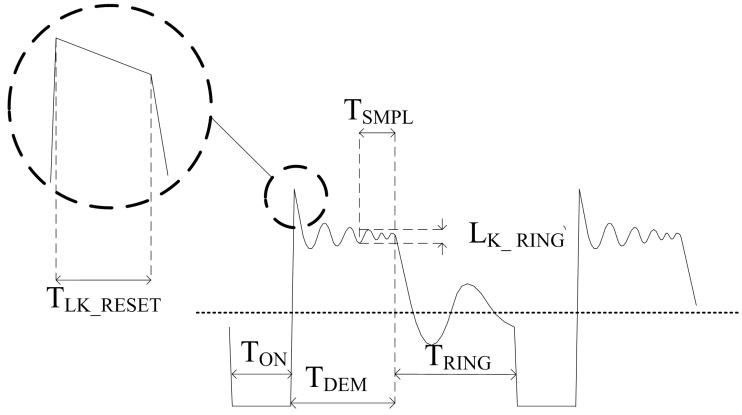


Figure 9 Auxiliary winding, detailed waveform

According to the flyback converter concept, the voltage is $-V_{BILK}/N_{PA}$ when the MOSFET switch is on and T_{ON} time and T_{DEM} time are two separate parts. The line sensor uses the FA pin voltage during the T_{ON} time.

This patented method (patent pending), simply works by clamping the FA voltage with an NPN bipolar transistor during the MOSFET on-time. This pin also senses the FA current generated through R_{S1} by the reflected bulk capacitor C_B voltage to provide run and stop thresholds for AC-input and to compensate the current sense threshold across the AC input range. The line sensor current is given by

$$I_{COMP} = \frac{1}{K_{LC}} \cdot \frac{\frac{N_A}{N_P} \cdot V_{VIN} - V_{FANC}}{R_{S1}} \qquad (5)$$

The line sensor voltage V_{RLC} realizes the feed forward compensation and ensures the consistency of the over current point at the high and low voltage. The voltage of feed forward resistance R_{LC} can be calculated by the following formula:

$$V_{RLC} = I_{COMP} \times R_{LC} = \frac{V_{VIN} \times T_D}{L_P} \times R_{CS} \qquad (6)$$

Where

- T_D is the total current sense delay consisting of the MOSFET turnoff delay, plus an internal delay of approximately 50ns
- L_P is the transformer primary inductance

R_{LC} is the value of the SCM1703A controllers internal line sensor resistor (see electrical characteristics).

Fault Protection

The SCM1703A controller provides extensive fault protection including the following:

- Output short-to-ground protection
- Output over voltage protection
- FA-pin fault protection
- CS-pin fault protection
- Internal over temperature protection

Output Short protection

During the first stage shown in figure 10, the controller can't get power from auxiliary winding if the output is shorted, then the VDD bypass capacitor voltage starts to drop, the controller can't output any gate pulse until the VDD bypass capacitor voltage drops to V_{VDD_OFF} level (see electrical characteristics).

In the second stage, the controller stops to generate gate pulses when V_{DD}=V_{VDD_OFF}, the internal high voltage startup device is active until V_{VDD} exceeds the UVLO turn-on threshold and at that time, the high voltage startup device turns off. The typical startup current I_{STH} as per electrical characteristics provides fast charging of the VDD capacitor C_{VDD}. The controllers power consumption causes VDD to fall below V_{VDD_OFF} again and the GATE can't output a driver signal during this time. Because the power consumption is smaller, the time of the second stage is longer then the first stage.

In the third stage, the device returns to the start state and a startup sequence is initiated. The internal high voltage startup device is active until V_{VDD} exceeds the UVLO turn-on threshold V_{VDD_ON} and at that time the high voltage startup device turns off.

The converter uses the time between the second and third stage to cool down. If the output to ground short remains, the above process, also called UVLO process, repeats itself periodically until the short is removed.

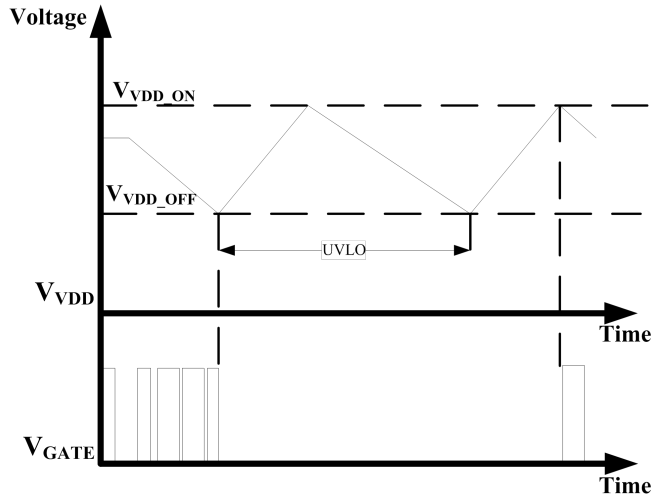


Figure 10: Timing and wave form with output short circuit

The over current point is limited by the chip, meaning that if the converter is over loaded, then the output voltage will drop to maintain the output power constant. The controller cannot get any power from the auxiliary winding because the output has dropped to the lower limit and the controller will repeat the same process.

Output Overvoltage Protection

The output overvoltage function is determined by the voltage feedback on the FA pin. If the FA sampler voltage exceeds V_{OVP} for the time T_{PD}, the output overvoltage protection will be triggered. The device stops switching and the internal current consumption becomes I_{FAULT} which discharges the VDD capacitor C_{VDD} to the turn-off threshold of the UVLO. Following, the device returns to the start state with a startup sequence, shown in figure 11.

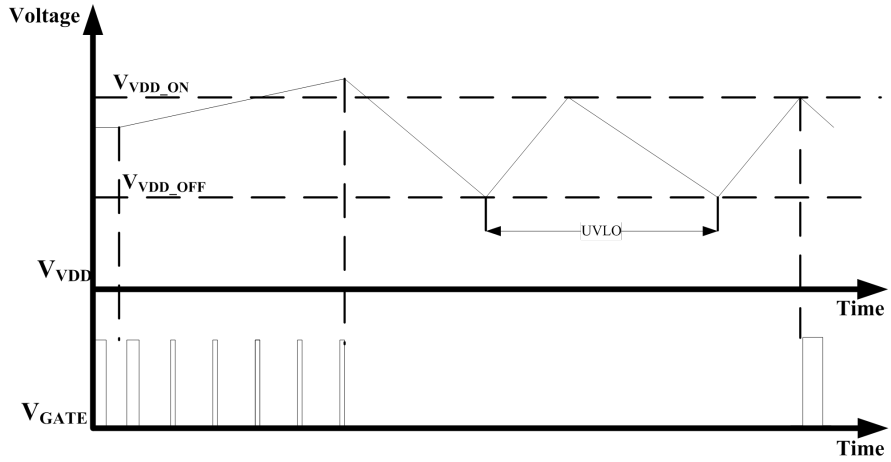


Figure 11: Timing wave form of output over voltage protection

Fault Protection, FA Pin

This protection prevents damage in the event of a component failure. If the feedback information on the FA pin is lost because of such a failure, the controller stops switching after a T_{PD} delay time, which triggers an UVLO reset/restart sequence as described under output over voltage protection

Fault Protection, CS Pin

The SCM1703A always operates with cycle-by-cycle primary peak current control with a normal operating voltage range on the CS pin of 0.8V to 0.27V. Once the voltage on the CS pin reaches 1.6 V, an additional protection that is not filtered by leading-edge blanking sets in and goes through a delay time defined as T_{PD}, which results in a UVLO reset/restart sequence, see also output over voltage protection.

Over Temperature Protection

The device initiates an UVLO reset cycle if the junction temperature reaches the internal over temperature protection threshold T_{J_STOP} as described in Electrical Characteristics. When the temperature remains above the threshold at the end of the UVLO cycle, the protection cycle repeats itself and only once the temperature falls below the $T_{J\_RESTART}$ value, (see electrical characteristics), the device exits the protection mode and resumes normal operation.

Ordering Information

Part Number	Package Type	No. of Pins	Silk Screen Marking	Reel information
SCM1703ASA	SOP7	7	SCM 1703ASA YM	3K/REEL

Product marking

SCM1703XYZ：

(1) SCM1703 = Product designation.

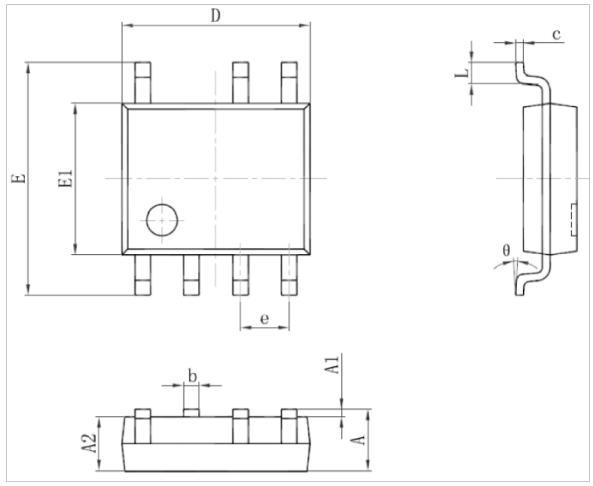
(2) X = Version information (Letter from A-Z).

(3) Y = Package definition; (S = SOP package).

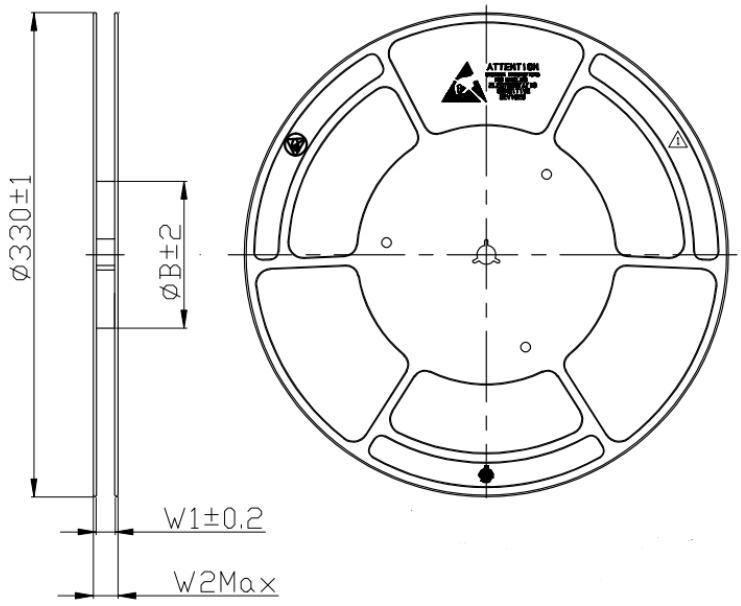
(4) Z = Operating temperature range (C = 0℃ to +70℃, I =-40℃ to +85℃, A =-40℃ to +125℃, M = -55℃ to +125℃) .

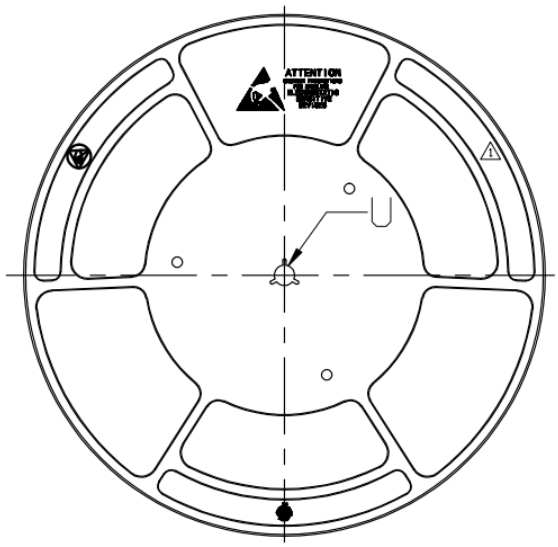
(5) YM = Date code for product traceability; Y = code for production year; M = code for production month.

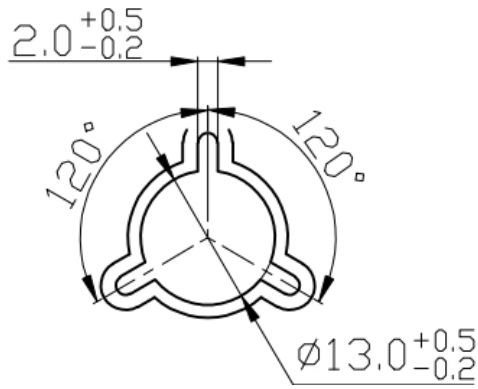
Mechanical Package Information



SOP7				
标识	Dimensions in millimeters		Dimensions in inches	
	Min	Max	Min	Max
A	1.350	17.50	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
e	1.270（BSC）		0.050（BSC）	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°







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Basic Disk Dimensions（mm）				
Package Type	Load Band Width	B	W1	W2Max
SOP8	12	180	12.4	18.4

Technical requirement：

1. Color：Blue（Reference color number：
   PANTONE DS 196-1 C ; C100 M70 Y0 K0
   PANTONE DS 197-1 C; C100 M70 Y0 K10
   PANTONE DS 205-1 C; C100 M60 Y0 K20
   PANTONE DS 205-2 C; C85 M50 Y0 K20
   PANTONE DS 206-2 C; C85 M50 Y0 K35
   PANTONE DS 219-1 C; C90 M50 Y5 K15）
2. Dimensions and tolerances according to ANSI/EIA-481-C-2003;
3. Disk surface good finish, no warping deformation；
4. External packing in good condition, no damage or pollution;

Mornsun Guangzhou Science & Technology Co., Ltd.

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