

ULN2803 *series High-voltage* *High-current Darlington Transistor Arrays*

Features

- 500-mA-Rated Collector Current(single output)
- High-Voltage Outputs:50V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

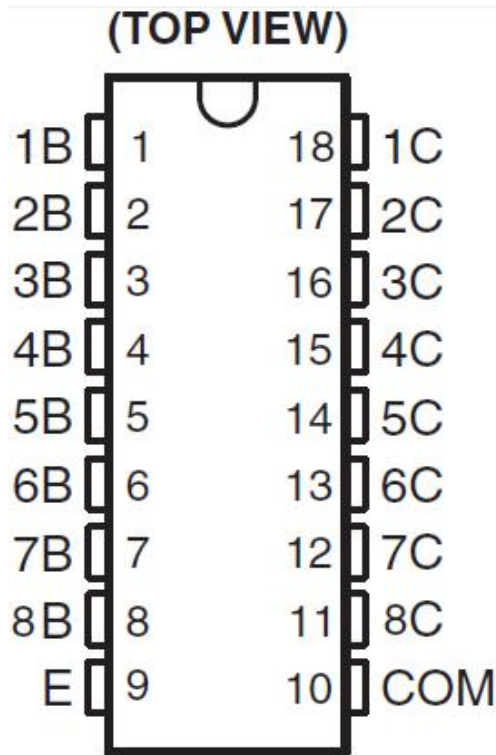
General Description

The TX2803 is high-voltage high-current Darlington transistor arrays each containing eight open collector common emitter pairs. Each pair is rated at 500mA. Suppression diodes are included for inductive load driving, the inputs and outputs are pinned in opposition to simplify board layout.

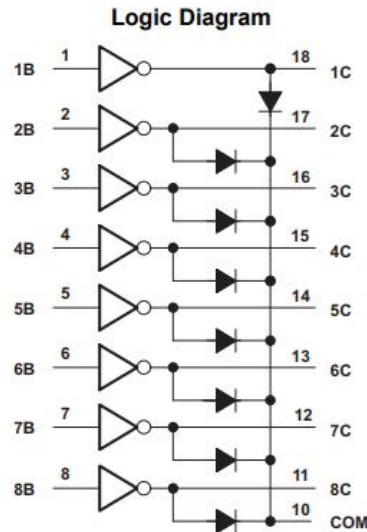
These devices are capable of driving a wide range of loads including solenoids, relays, DC motors, LED displays, filament lamps, thermal print-heads and high-power buffers.

The TX2803 is available in both a small outline 18-pin package (SOP18).

Pin Assignments



Connection Diagram

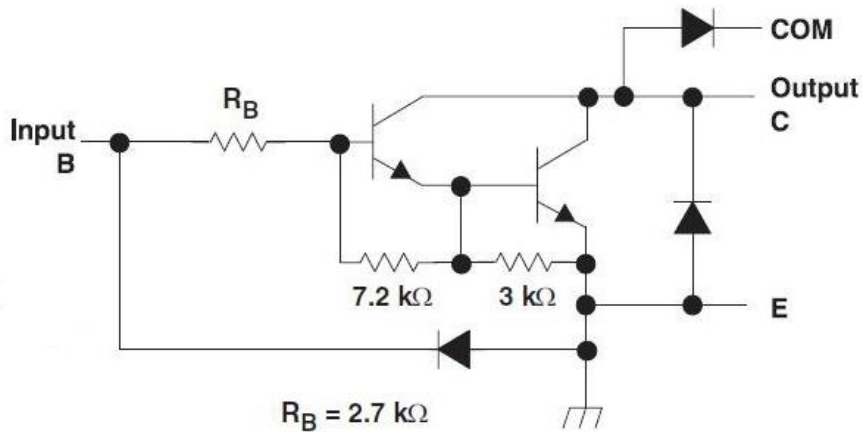


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Pin Descriptions

Pin Number	Pin Name	Function
1	1B	Input pair1
2	2B	Input pair2
3	3B	Input pair3
4	4B	Input pair4
5	5B	Input pair5
6	6B	Input pair6
7	7B	Input pair7
8	8B	Input pair8
9	E	Common Emitter (ground)
10	COM	Common Clamp Diodes
11	8C	Output pair8
12	7C	Output pair7
13	6C	Output pair6
14	5C	Output pair5
15	4C	Output pair4
16	3C	Output pair3
17	2C	Output pair2
18	1C	Output pair1

Functional Block Diagram



Note: All resistor values shown are nominal.

The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collector(s) go below ground an external Schottky diode should be added to clamp negative undershoots.

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Absolute Maximum Ratings ⁽¹⁾

At 25°C free-air temperature (unless otherwise noted)

Symbol	Parameter		Min	Max	Unit
V _{CC}	Collector to emitter voltage			50	V
V _R	Clamp diode reverse voltage(2)			50	V
V _I	Input voltage(2)			30	V
I _{CP}	Peak collector current	See typical characteristics		500	mA
I _{OK}	Output clamp current			500	mA
I _{TE}	Total emitter-terminal current			-2.5	A
T _A	Operating free-air temperature range	TX2003	-30	+105	°C
θ _{JA}	Thermal Resistance Junction-to-Ambient(3)			63	°C/W
θ _{JC}	Thermal Resistance Junction-to-Case(4)			12	
T _J	Operating virtual junction temperature			150	°C
T _{STG}	Storage temperature range		-40	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
- (3) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $PD = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) Maximum power dissipation is a function of T_{J(max)}, θ_{JC}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $PD = (T_J(max) - T_A)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V _{CC}	Collector to Emitter voltage	-	50	V
T _A	Operating Ambient Temperature	-30	+105	°C

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Electrical Characteristics (TA=+25°C, unless otherwise specified)

Parameter		Test Figure	Test Conditions		MIN	TYP	MAX	Unit
V _{I(on)}	On-state input voltage	Figure 6	V _{CE} = 2 V	I _C = 200 mA	--	--	2.4	V
				I _C = 250 mA	--	--	2.7	
				I _C = 300 mA	--	--	3	
V _{CE(sat)}	Collector-emitter saturation voltage	Figure 5	I _I = 250 μA, I _C = 100 mA	--	0.9	1.1	V	
			I _I = 350 μA, I _C = 200 mA	--	1	1.3		
			I _I = 500 μA, I _C = 350 mA	--	1.2	1.6		
I _{CEX}	Collector cutoff current	Figure 1	V _{CE} = 50 V, I _I = 0	--	--	50	μA	
		Figure 2	V _{CE} = 50 V, T _A = +105°C, I _I = 0	--	--	100		
V _F	Clamp forward voltage	Figure 8	I _F = 350 mA	--	1.7	2	V	
I _{I(off)}	Off-state input current	Figure 3	V _{CE} = 50 V, I _C = 500 μA	50	65	--	μA	
I _I	Input current	Figure 4	V _I = 3.85 V	--	0.93	1.35	mA	
			V _I = 5 V	--	--	--		
			V _I = 12 V	--	--	--		
I _R	Clamp reverse current	Figure 7	V _R = 50 V		--	--	50	μA
				T _A = 70°C	--	--	100	
C _i	Input capacitance		V _I = 0, f = 1 MHz	--	15	25	pF	

Switching Characteristics (TA = +25°C, unless otherwise specified)

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	See Figure 9		0.25	1	μs
t _{PHL}	Propagation delay time, high- to low-level output	See Figure 9		0.25	1	μs
V _{OH}	High-level output voltage after switching	V _S = 50 V, I _O = 300 mA, See Figure 9	V _S -20			mV

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Parameter Measurement Information

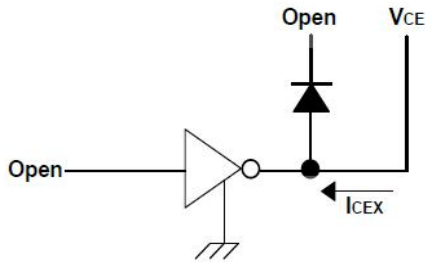


Fig.1 ICEX Test Circuit

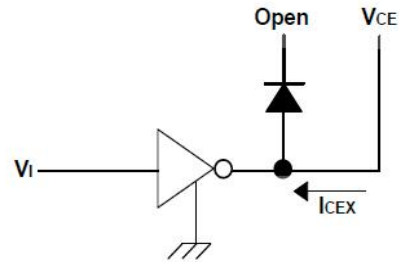


Fig.2 ICEX Test Circuit

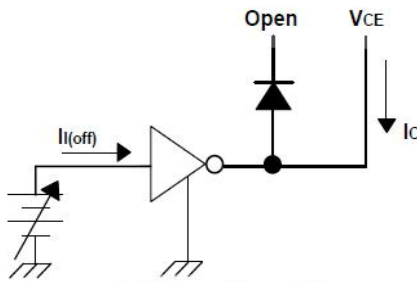


Fig.3 I(off) Test Circuit

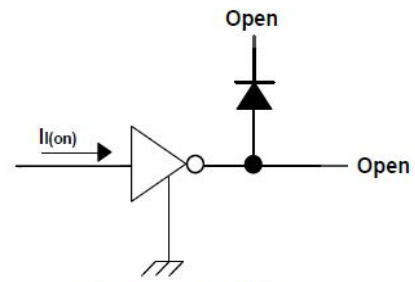


Fig.4 I(on) Test Circuit

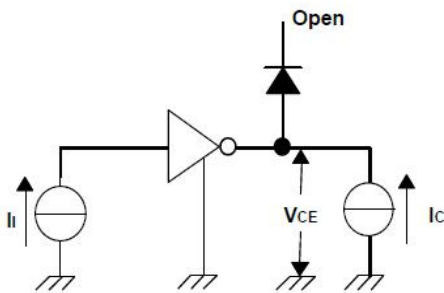


Fig. 5 h_{FE} , $V_{CE(sat)}$ Test Circuit

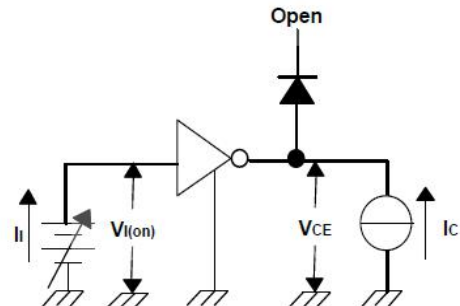


Fig. 6 $V_{(on)}$ Test Circuit

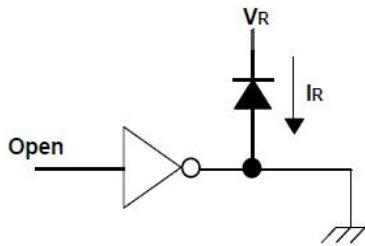


Fig. 7 I_R Test Circuit

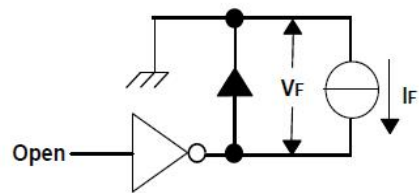


Fig. 8 V_F Test Circuit

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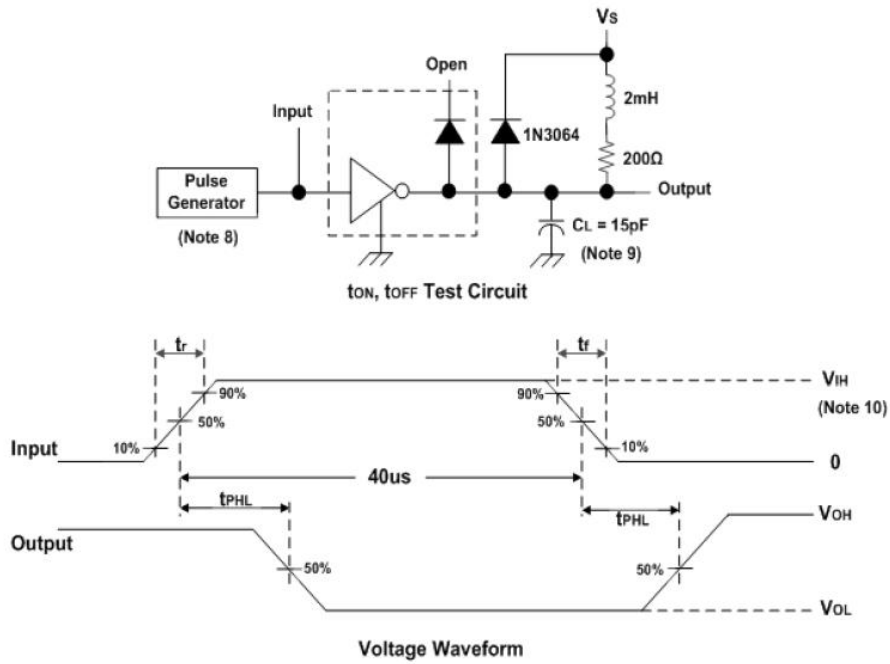


Fig. 9 Latch-Up Test Circuit and Voltage Waveform

Notes: 9. C_L includes probe and jig capacitance.

10. $V_{IH}=3V$

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SOP18 Outline Dimensions

