OTOMO

Otomo Semiconductor (Shenzhen) Co., Ltd.

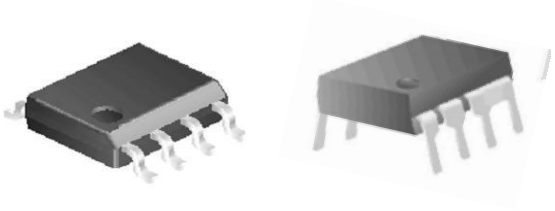
KA3842B/KA3843B/KA3844B/KA3845B high -performance current mode controller

Overview and characteristics

KA3842B/KA3843B/KA3844B/KA3845B is a high -performance frequency frequency current mode controller. They are designed for the application of offline converters and DC-DC converters, providing designers with low-cost solutions with the least external components. These integrated circuits have a fine -tuning oscillator, temperature compensation reference power supply, high -gain error placing large device, current detection comparator, and high -current MOSFET output. It also includes the protection function, including input and under pressure locking, cycle -by -cycle current limit, programmable output dead zone time, and locks used for single pulse measuring.

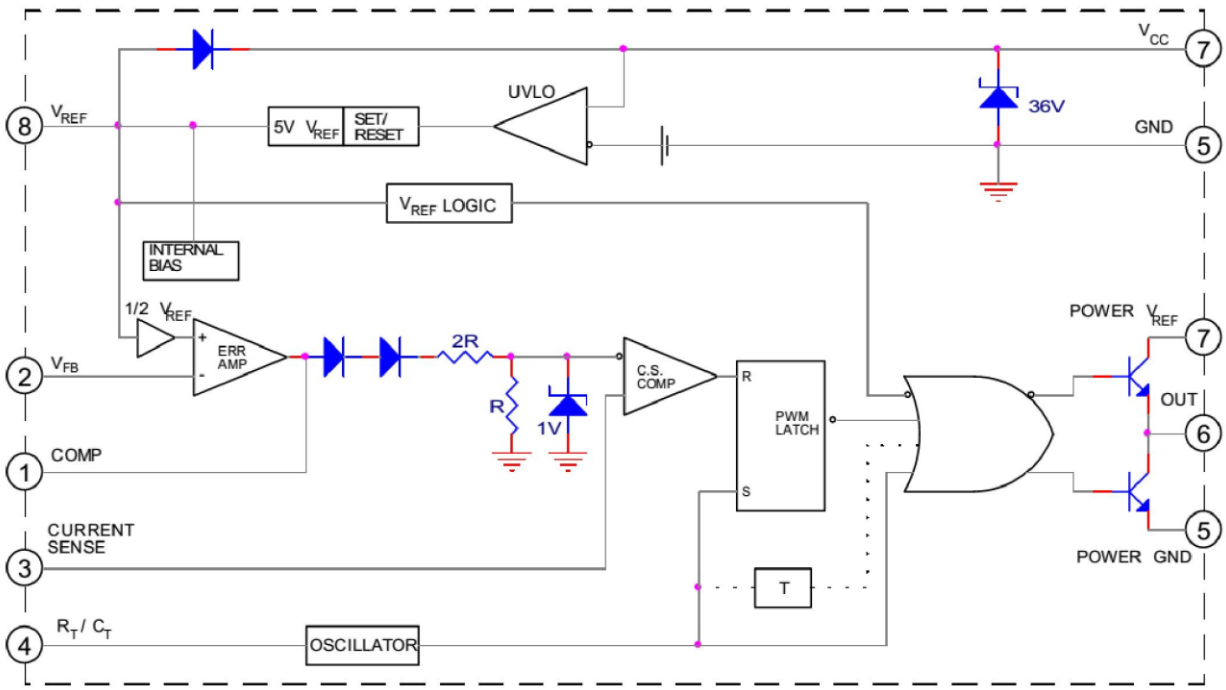
Main features

1. Owacing voltage lock circuit
2. low start current (<0.3mA)
3. Stable internal band gap benchmark voltage source
4. Large -current chart column output (drive current reaches 1A) 5. The operating frequency can reach 500kHz
6. Automatic negative feedback compensation circuit
7. Pulse current limit
8. Enhanced load response characteristics

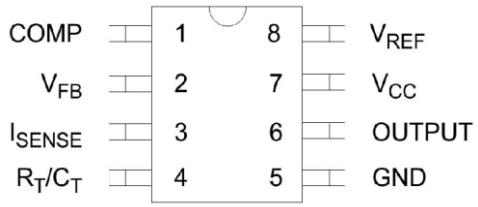


SOP-8 DIP-8

Frame diagram



Discover end function



序号	符号	功能	序号	符号	功能
1	COMP	比较端	5	GND	地
2	V_{FB}	负反馈	6	OUTPUT	输出
3	I_{SENSE}	电流灵敏度	7	V_{CC}	电源
4	R_T/C_T	振荡端	8	V_{REF}	参考电压

The maximum rated value (unless special explanation, tamb = 25 ℃)

Parameter name	Symbol	Value	Unit
Voltage	Vcc	30	V
Output current	Io	±1	A
Error amplifier current	Isink (EA)	10	mA
Error amplifier input voltage	Vin (EA)	-0.3 ~ +6.3	V
Power consumption	PD(DIP)	1	W
Working temperature	Tamb	0 ~ 70	℃
Storage temperature	Tstg	-55 ~ 150	℃

Electric special (unless specifically explained, VCC = 15V Note 1, RT = 10kΩ, CT = 3.3NF, TAMB = 0 ℃ ~ 70 ℃)

Parameter name	Symbol	Test condition	Mini	Typical	Max	Unit
The benchmark power part						
The reference voltage	V_{ref}	Tj=25C, I_{ref}=1mA	4.9	5	5.1	V
Linear adjustment rate	Reg_{line}	12V≤Vcc≤25V	-	6	20	mV
Load adjustment rate	Reg_{load}	1mA≤ I_{ref} ≤20mA	-	6	25	mV
Short -circuit output current	Isc	Tamb=25℃	-30	-80	-180	mA
Oscillating part						
Oscillation frequency	f_{OSC}	Tj=25℃	47	52	57	kHz
Frequency voltage characteristics	Δf/ΔV	12V≤Vcc≤25V	-	0.2	1	%
Amplitude of oscillation	V_{OSC}	Pin4 Foot peak value	-	1.6	-	Vpp
Error amplifier part (EA)						
Input bias current	I_{IB}	V_{FB}=5.0V	-	-0.1	-2	μA
Feedback input voltage	V_{FB}	V_{FB}=V_{comp}	2.42	2.5	2.58	V
Open-loop voltage gain	A_{VOL}	2V≤V_O≤4V	60	90	-	dB
Power rejection ratio	PSRR	12V≤V_{CC}≤25V	60	70	-	dB
Output irrigation current	I_{SINK}	V_{FB} =2.7V, V_{comp} =1.1V	2	6.5	-	mA
Output source current	I_{SOURCE}	V_{FB} =2.3V, V_{comp} =5.0V	-0.5	-0.9	-	mA
Output high level	V_{OH}	V_{FB} =2.3V,R_L=15kΩ to GND	5	6.4	-	V
Output low level	V_{OL}	V_{FB} =2.7V,R_L=15kΩ to Vref	-	0.87	1.1	V

Current sensitivity part

Gain	A_V	(Notes 2 and 3)	2.85	3	3.15	V/V
Maximum input threshold	Vth	V_{comp} =5.0V (Notes 2)	0.9	1	1.1	V
Power supply voltage suppression ratio	PSRR	12V≤V_{CC}≤25V (Notes 2)	-	70	-	dB
Input bias current	I_{IB}		-	-2	-10	μA

Output part

Output low level	V_{OL}	I_{SINK}=20mA	-	0.1	0.4	V
		I_{SINK}=200mA	-	1.5	2.2	V
Output high level	V_{OH}	I_{SOURCE}=20mA	13	13.5	-	V
		I_{SOURCE}=200mA	12	13	-	V
Rise time	tr	C_L=1.0 nF	-	50	150	ns
Descent time	tf	C_L=1.0 nF	-	50	150	ns

UVLO circuit

Starting threshold	V_{start}	KA3842B/KA3844B	14.5	15.5	17.5	V
		KA3843B/KA3845B	7.8	8.3	9	V
Maintain voltage	V_{hold}	KA3842B/KA3844B	8.5	9.8	11.5	V
		KA3843B/KA3845B	7	7.6	8.2	V

PWM part

Maximum duty ratio	DC_{max}	KA3842B/KA3843B	90	94	-	%
		KA3844B/KA3845B	45	48	50	%
Minimum duty ratio	DC_{min}		-	-	0	%

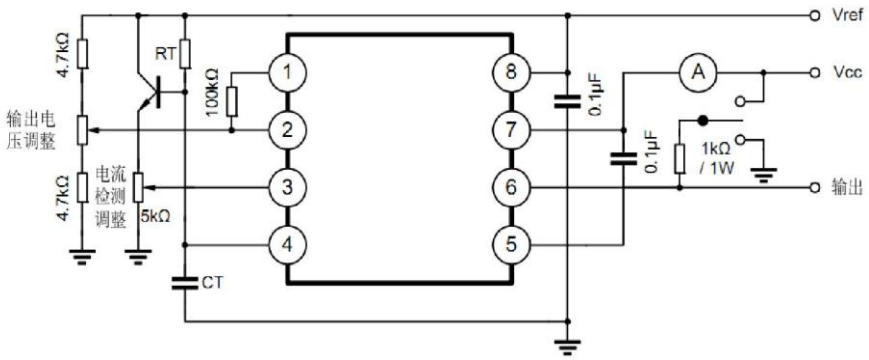
Quiescent Current

Starting current	I_{ST}	KA3842B/KA3844B	-	0.26	0.5	mA
		KA3843B/KA3845B	-	0.13	0.5	mA
Working current	Icc	V_{FB} =V_{sense} =0V	-	11	17	mA
ZENER voltage	V_Z	Icc=25mA	-	34	-	V

Note:

1. Adjust the VCC to the circuit to start and set it to 15V
2. Parameters measured at the lock -jump point of jumping point
3. Definition of gain as: a v = Δvcomp/ΔvSense; 0 ≤ VSense ≤ 0.8V

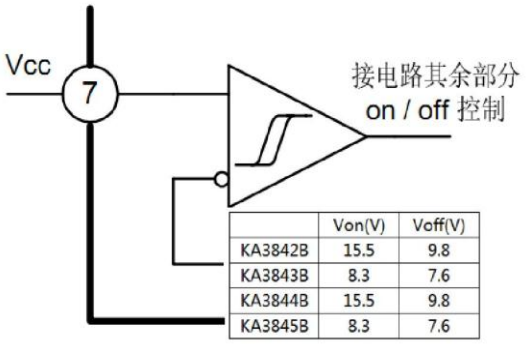
Test circuit



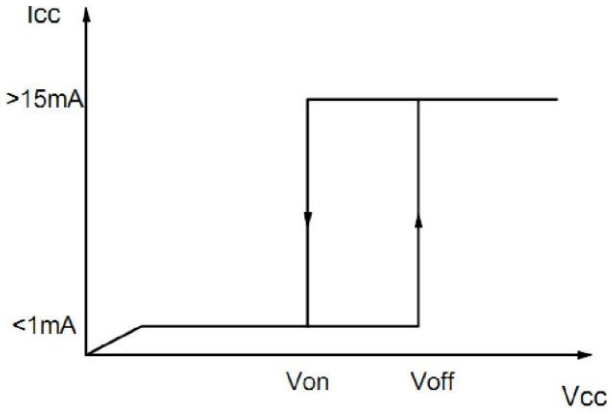
When there is a peak current related to capacity load, you need to consider the groundingtechnology carefully. Timing a nd bypass capacitors must be installed at 5 feet and grounded.

The transistor and a 5KΩ potentiometer are used to sampling the waveform and send the sloping waveform to the 3 pin

Impurd pressure control (UVLO)



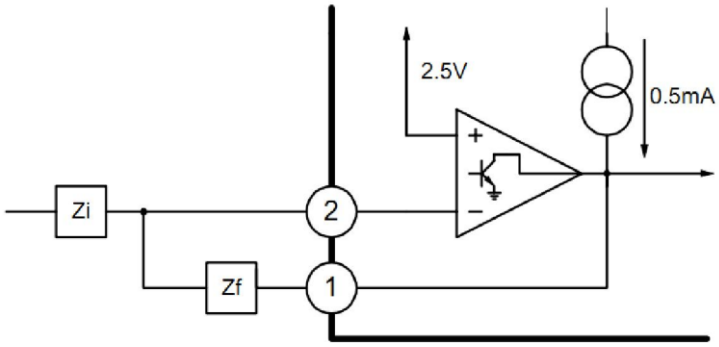
	Von(V)	Voff(V)
KA3842B	15.5	9.8
KA3843B	8.3	7.6
KA3844B	15.5	9.8
KA3845B	8.3	7.6



When entering the underwriting, the output driver is placed in a high resistance state. The 6 foot must use a leakage resi

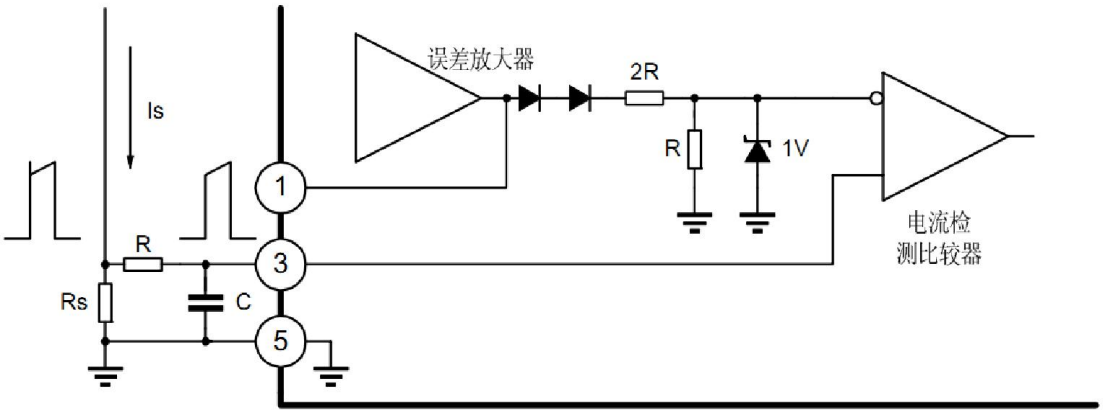
stance to prevent the leakage current from driving the power switch.

Error Putting Large Connection



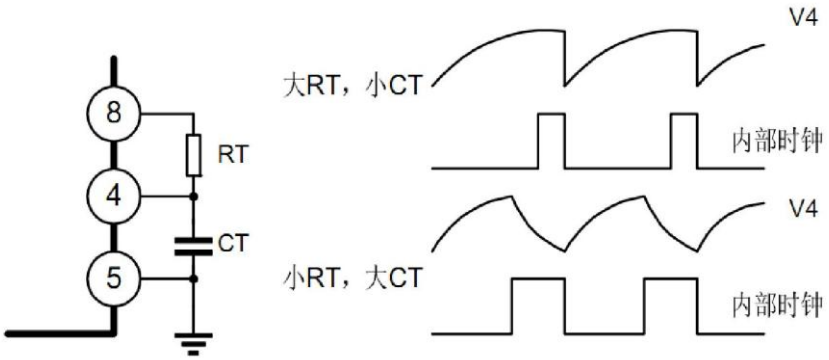
Error amplifier can push and output 0. 5mA current

Current detection line



Peak current (IS) is defined as: IS (MAX) ≈1.0V/R S A small RC filtering network is required to suppress the transient response of the switch

Oscillator waveform and maximum duty cycle, period



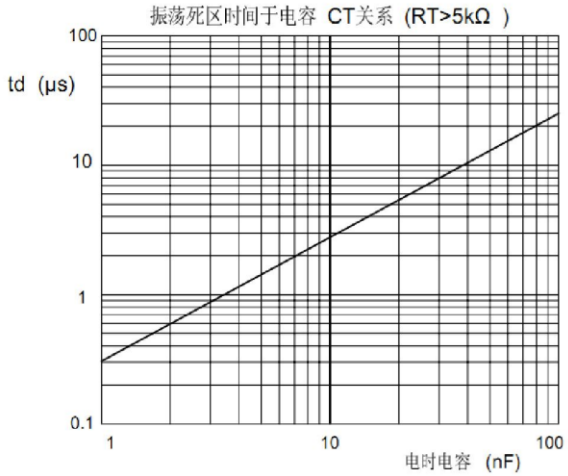
The oscillating timing capacitor CT is charged by the VREF by RT and discharged by an internal current source. The internal clock signal is output driven to a low level during discharge. The selection of RT and CT can simultaneously determine the oscillation period and the maximum duty cycle. The time of charge and discharge is determined by the following formula

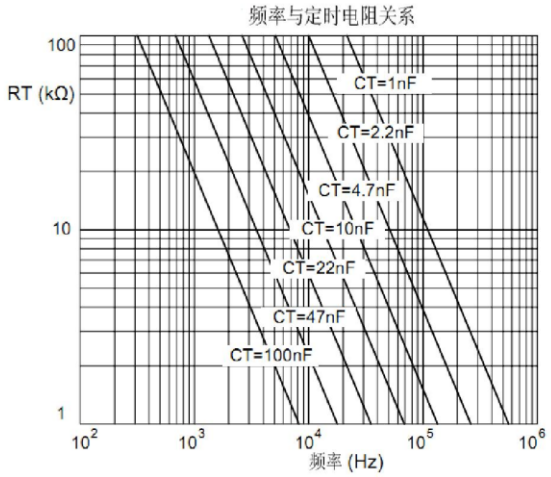
$$t_c \approx 0.55 R_T * C_T$$

$$t_d \approx R_T * C_T * \ln\left(\frac{0.063 R_T - 2.7}{0.063 R_T - 4}\right)$$

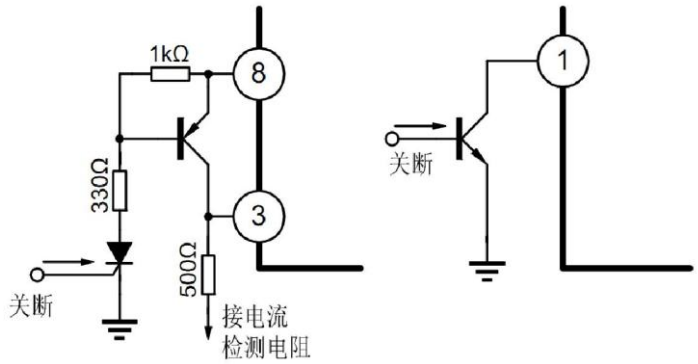
这时频率为：$f=(tc+td)^{-1}$

当$R_T>5K\Omega$时，$f \approx \frac{1.8}{R_T * C_T}$



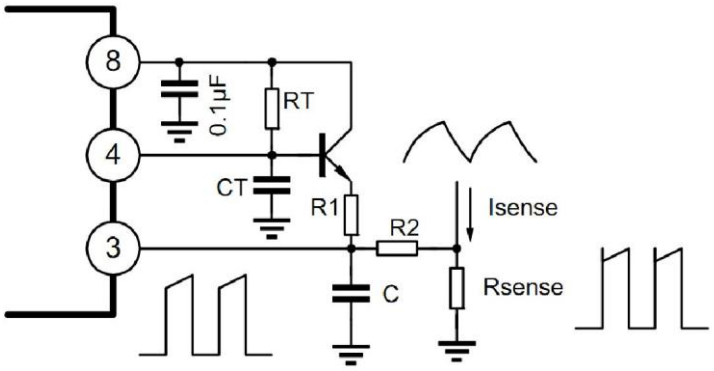


Turn-off technique



KA384xB can be turned off in two ways: by raising the 3-pin voltage above 1V or by lowering the 1-pin voltage to the ground level of the two diodes
Both methods make the output of the PWM comparator high within the forward voltage drop (refer to the internal block diagram). The PWM latch trigger is reset prefertively to keep the output low until the next clock cycle after the pin 1 or pin 3 off signal is removed. An example of an external latch-off is achieved by adding a unidirectional thyristor (SCR), which will reset when the supply voltage VCC falls below the UVLO threshold. At this point, the SCR is allowed to reset when the reference voltage is turned off.

Slope compensation



A portion of the oscillator slope can be corrected with a current detection signal to allow slope compensation in converter s requiring more than 50% duty cycle. Capacitor C and resistor R2 form a filter to suppress switching spikes on rising edg