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June 2014

74LVX08
Low Voltage Quad 2-Input AND Gate

Features

- Input Voltage Level Translation from 5 V to 3 V
- Ideal for Low-power / Low-Noise 3.3 V Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic threshold Performance

Description

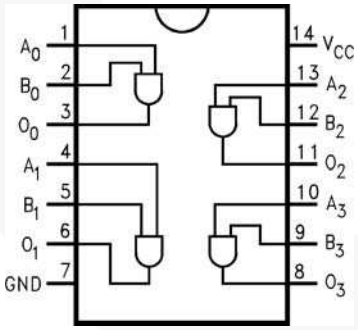
The LVX08 contains four 2-input AND gates. The inputs tolerate voltages up to 7 V allowing the interface of 5 V systems to 3 V systems.

Ordering Information

Part Number	Top Mark	Package	Packing Method	Packing Description
74LVX08M	LVX08	SOIC 14L	Rail	14-Lead Small Outline Integrated Circuit, JEDEC MS-012, 0.150 inch Narrow
74LVX08MX	LVX08	SOIC 14L	Tape and Reel	14-Lead Small Outline Integrated Circuit, JEDEC MS-012, 0.150 inch Narrow
74LVX08MTCX	LVX08	TSSOP 14L	Tape and Reel	14-Lead Thin Shrink Small Outline Package, JEDEC MO-153, 4.4 mm Wide

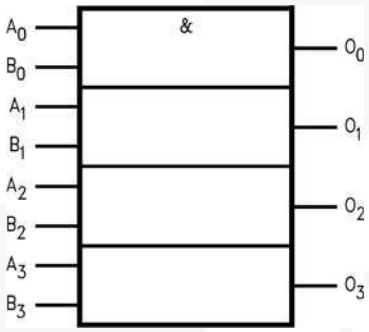
All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol

IEEE/IEC



Pin Description

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Rating
V_{CC}	Supply Voltage		-0.5 V to 7.0 V
I_{IK}	DC Input Diode Current, V_I = -0.5 V		-20 mA
V_I	DC Input Voltage		-0.5 V to 7.0 V
I_{OK}	DC Output Diode Current	V_O = -0.5 V	-20 mA
		V_O = V_{CC} + 0.5 V	+20 mA
V_O	DC Output Voltage		-0.5 V to V_{CC} + 0.5 V
I_O	DC Output Source or Sink Current		±25 mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		±50 mA
T_{STG}	Storage Temperature		-65°C to 150°C
P	Power Dissipation		180 mW
T_L	Lead Temperature (Soldering, 10 seconds)		240°C

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0 V to 3.6 V
V_I	Input Voltage	0 V to 5.5 V
V_O	Output Voltage	0 V to V_{CC}
T_A	Operating Temperature	-40°C to 85°C
$\Delta t / \Delta V$	Input Rise and Fall Time	0 ns/V to 100 ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

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DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A = 25°C			T_A = -40°C to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	2.0		1.5			1.5		V
		3.0		2.0			2.0		
		3.6		2.4			2.4		
V_{IL}	LOW Level Input Voltage	2.0				0.5		0.5	V
		3.0				0.8		0.8	
		3.6				0.8		0.8	
V_{OH}	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = -50 µA	1.9	2.0		1.9		V
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = -50 µA	2.9	3.0		2.9		
			$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = -4 mA	2.58			2.48		
V_{OL}	LOW Level Output Voltage	2.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = -50 µA		0.0	0.1		0.1	V
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = -50 µA		0.0	0.1		0.1	
			$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = -4 mA			0.36		0.44	
I_{IN}	Input Leakage Current	3.6	V_{IN} = 5.5 V or GND			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	3.6	$V_{IN} = V_{CC}$ or GND			2.0		20.0	µA

Noise Characteristics(2)

Symbol	Parameter	V_{CC} (V)	C_L (pF)	T_A = 25°C		Unit
				Typ.	Limit	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	50	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	50	-0.3	-0.5	V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	3.3	50		2.0	V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	3.3	50		0.8	V

Note:

2. Input $t_r = t_f$ = 3 ns

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AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	C_L (pF)	T_A = 25°C			T_A = -40°C to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7	15		6.3	11.4	1.0	13.5	ns
			50		8.8	14.9	1.0	17.0	
		3.3 ± 0.3	15		4.8	7.1	1.0	8.5	
			50		7.3	10.6	1.0	12.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew(3)	2.7	50			1.5		1.5	ns
		3.3				1.5		1.5	

Note:

3. Parameter guaranteed by design $t_{OSLH} = | t_{PLHm} - t_{PLHn} |$, $t_{OSHL} = | t_{PHLm} - t_{PHLn} |$.

Capacitance

Symbol	Parameter	T_A = 25°C			T_A = -40°C to +85°C		Unit
		Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance(4)		18				pF

Note:

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
   Average operating current can be obtained by the eqation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{4 \text{ (per Gate)}}$

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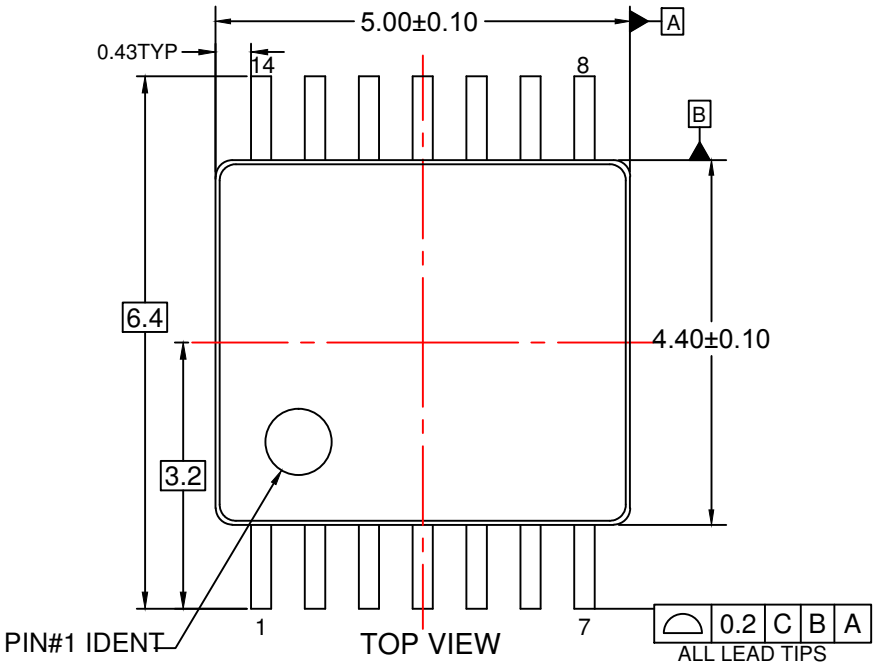
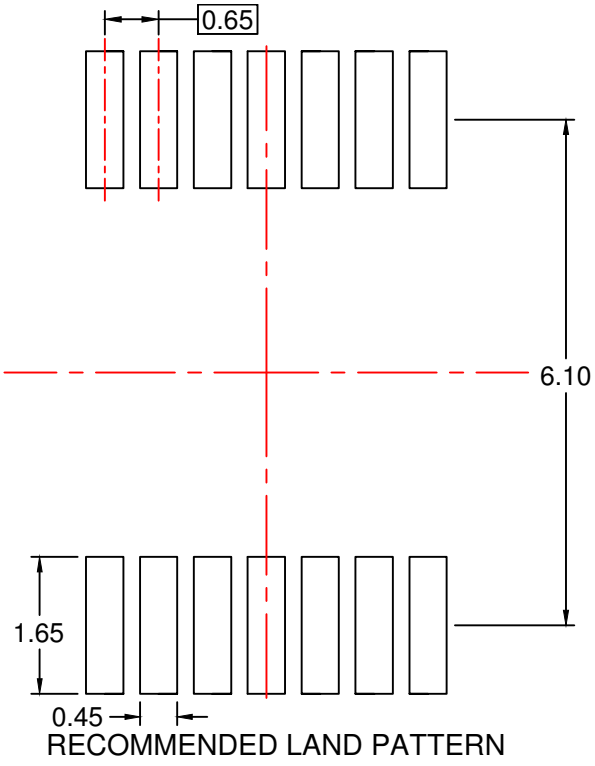
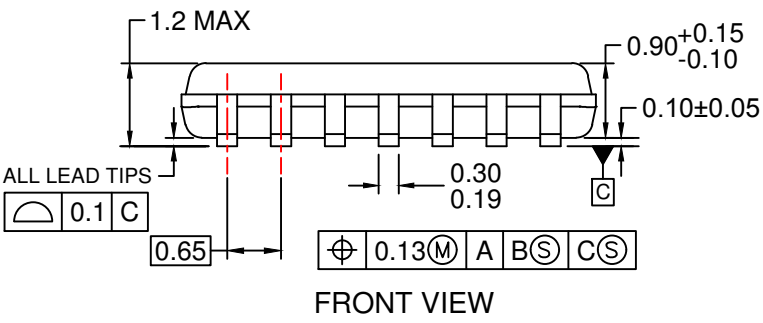
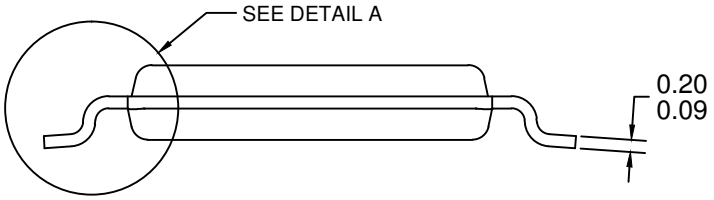
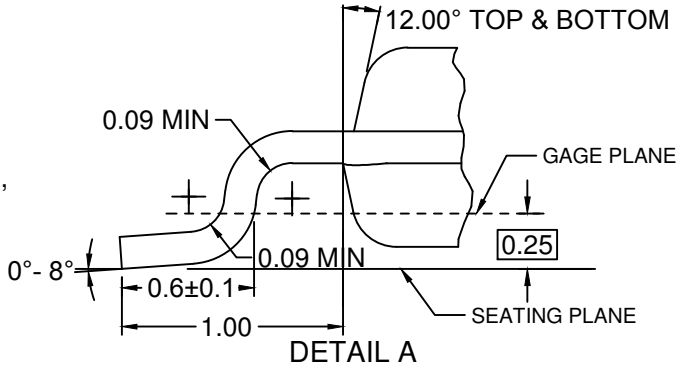










NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS.

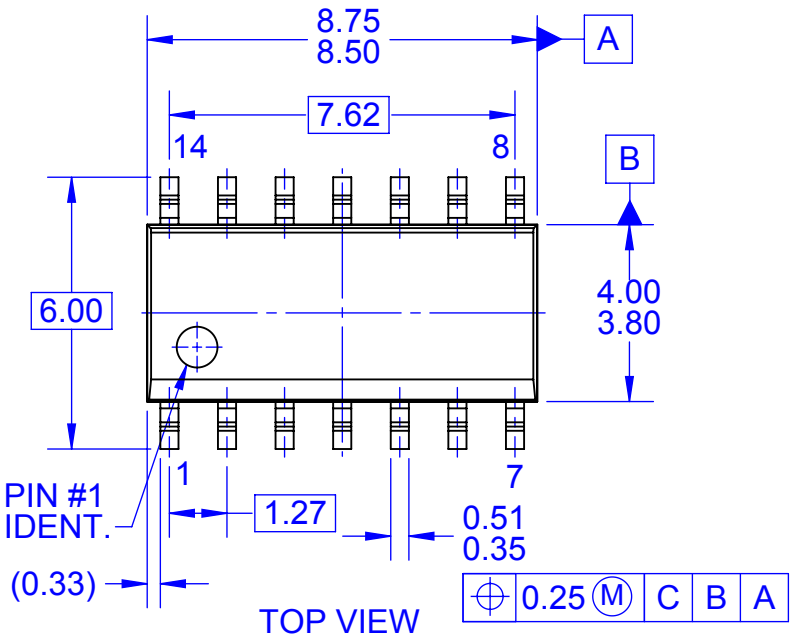
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

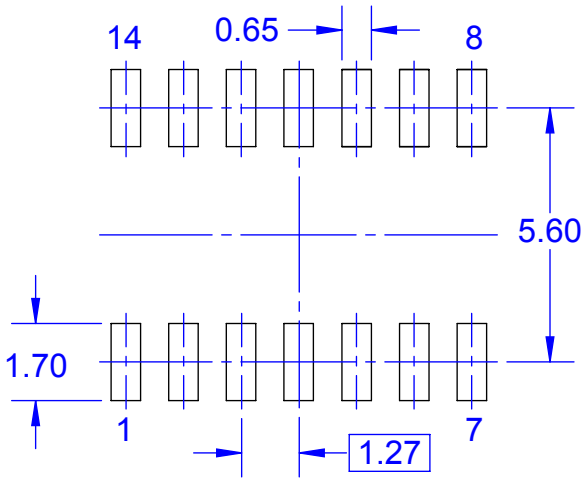
E. LANDPATTERN STANDARD: SOP65P640X110-14M.

F. DRAWING FILE NAME: MKT-MTC14rev7.

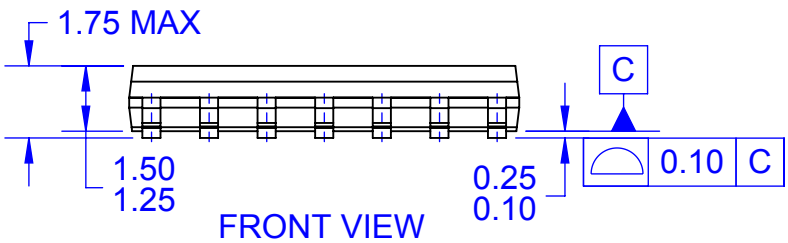
FAIRCHILD



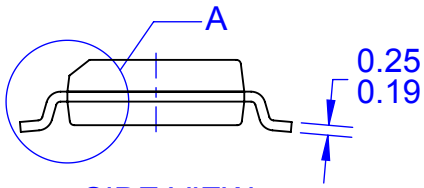
TOP VIEW



LAND PATTERN RECOMMENDATION



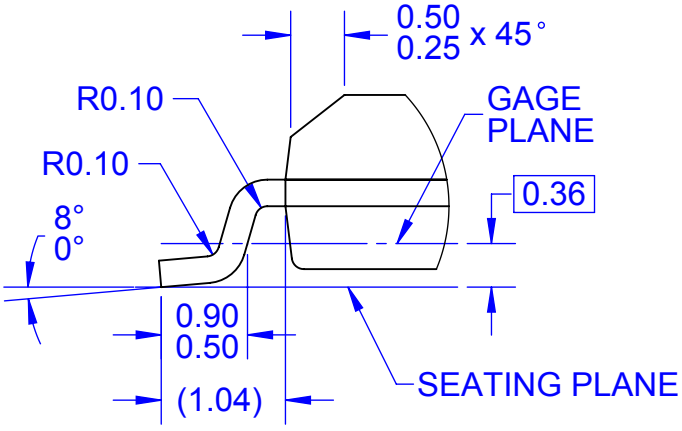
FRONT VIEW



SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14



DETAIL A
SCALE 16 : 1

FAIRCHILD ™

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