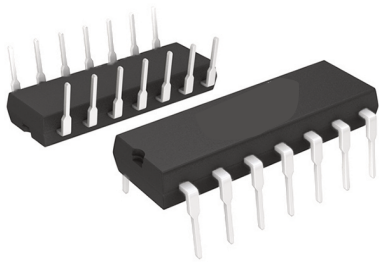


Description

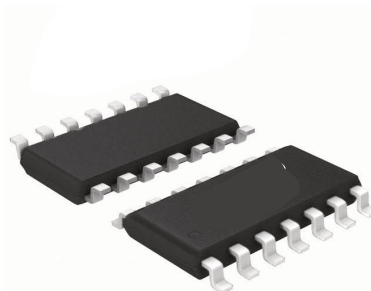
The SN74LS164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (DSA and DSB), eight parallel data outputs (Q0 to Q7). Data is entered serially through DSA or DSB and either input can be used as an active HIGH enable for data entry through the other input. Data is shifted on the LOW-to-HIGH transitions of the clock (CP) input. A LOW on the master reset input (MR) clears the register and forces all outputs LOW, independently of other inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Features

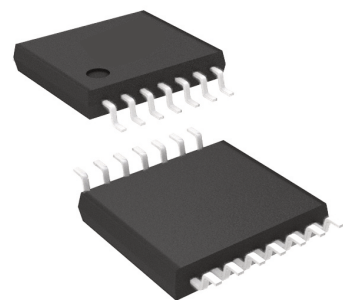
- Gated serial data inputs
- Asynchronous master reset
- Specified from -20°C to +85°C
- Packaging information: DIP-14/SOP-14/TSSOP-14



DIP-14



SOP-14



TSSOP-14

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74LS164N	DIP-14	74LS164N	Tube	1000Pcs/Box
XBLW SN74LS164DTR	SOP-14	74LS164	Tape	2500Pcs/Reel
XBLW SN74LS164TDTR	TSSOP-14	74LS164	Tape	3000Pcs/Reel

Block Diagram

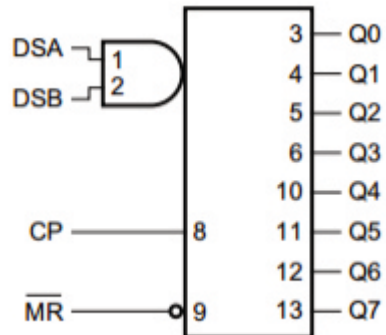


Figure 1. Logic symbol

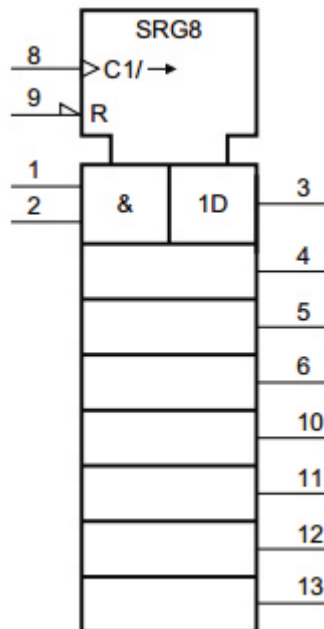


Figure 2. IEC logic symbol

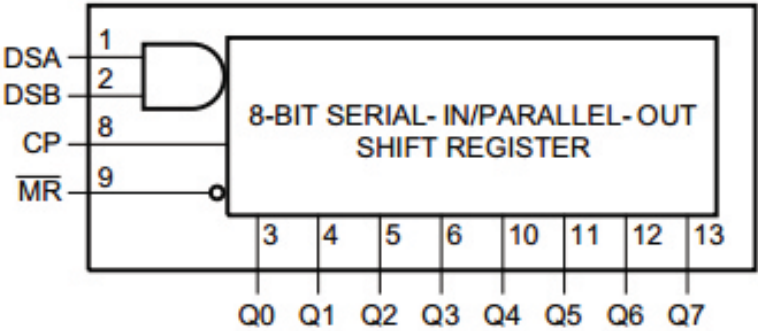


Figure 3. Logic diagram

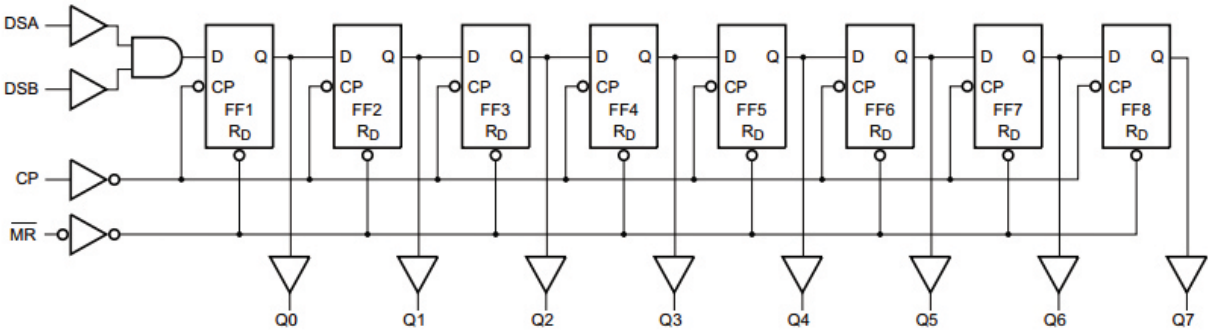
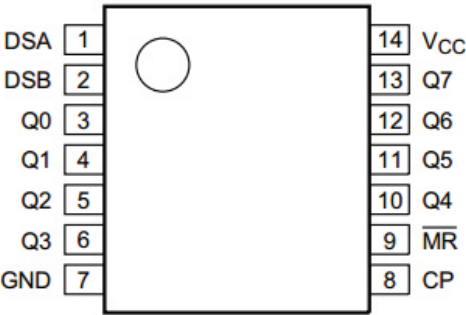


Figure 4. Functional diagram

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	DSA	data input
2	DSB	data input
3	Q0	output
4	Q1	output
5	Q2	output
6	Q3	output
7	GND	ground (0V)
8	CP	clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{\text{MR}}$	master reset input (active LOW)
10	Q4	output
11	Q5	output
12	Q6	output
13	Q7	output
14	V _{CC}	supply voltage

Function Table

Operating modes	Input				Output	
	$\overline{\text{MR}}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	Lto L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

Note:

H=HIGH voltage level; L=LOW voltage level; ↑=LOW-to-HIGH clock transition;

h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

q=lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V _{CC}	-		-0.5	+7	V
input clamping current	I _{IK}	V _I < -0.5V or V _I > V _{CC} +0.5V		-	±20	mA
output clamping current	I _{OK}	V _O < -0.5V or V _O > V _{CC} +0.5V		-	±20	mA
output current	I _O	-0.5V < V _O < V _{CC} +0.5V		-	±25	mA
supply current	I _{CC}	-		-	50	mA
ground current	I _{GND}	-		-50	-	mA
total power dissipation	P _{tot}	-		-	500	mW
storage temperature	T _{stg}	-		-65	+150	°C
Soldering temperature	T _L	10s	DIP	245		°C
			SOP/TSSOP	260		

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
ambient temperature	T_{amb}	-	-20	-	+85	°C

Electrical Characteristics**DC Characteristics 1**(T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	V _{CC} =2.0V		1.5	1.2	-	V
		V _{CC} =4.5V		3.15	2.4	-	V
		V _{CC} =6.0V		4.2	3.2	-	V
LOW-level input voltage	V _{IL}	V _{CC} =2.0V		-	0.8	0.5	V
		V _{CC} =4.5V		-	2.1	1.35	V
		V _{CC} =6.0V		-	2.8	1.8	V
HIGH-level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	2.0	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	4.5	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	6.0	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.98	4.32	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.48	5.81	-	V
LOW-level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	0	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	0	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	0	0.1	V
			I _O =4.0mA; V _{CC} =4.5V	-	0.15	0.26	V
			I _O =5.2mA; V _{CC} =6.0V	-	0.16	0.26	V
input leakage current	I _I	V _I = V _{CC} or GND; V _{CC} =6.0V		-	-	±1	uA
supply current	I _{CC}	V _I = V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	8	uA
input capacitance	C _I	-		-	3.5	-	pF

DC Characteristics 2(T_{amb}=-20°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	V _{CC} =2.0V		1.5	-	-	V
		V _{CC} =4.5V		3.15	-	-	V
		V _{CC} =6.0V		4.2	-	-	V
LOW-level input voltage	V _{IL}	V _{CC} =2.0V		-	-	0.5	V
		V _{CC} =4.5V		-	-	1.35	V
		V _{CC} =6.0V		-	-	1.8	V
HIGH-level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	-	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	-	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	-	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.84	-	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.34	-	-	V
LOW-level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	-	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	-	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	-	0.1	V
			I _O =4.0mA; V _{CC} =4.5V	-	-	0.33	V
			I _O =5.2mA; V _{CC} =6.0V	-	-	0.33	V
input leakage current	I _I	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	± 1	uA
supply current	I _{CC}	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	80	uA

AC Characteristics 1

($T_{amb}=25^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CP to Qn propagation delay	t_{pd}	see Figure 6	$V_{CC}=2.0V$	-	41	170 ns
			$V_{CC}=4.5V$	-	15	34 ns
			$V_{CC}=5.0V; C_L=15pF$	-	12	- ns
			$V_{CC}=6.0V$	-	12	29 ns
$\bar{MR}$ to Qn propagation delay	t_{PHL}	see Figure 7	$V_{CC}=2.0V$	-	39	140 ns
			$V_{CC}=4.5V$	-	14	28 ns
			$V_{CC}=5.0V; C_L=15pF$	-	11	- ns
			$V_{CC}=6.0V$	-	11	24 ns
transition time	t_t	see Figure 6	$V_{CC}=2.0V$	-	19	75 ns
			$V_{CC}=4.5V$	-	7	15 ns
			$V_{CC}=6.0V$	-	6	13 ns
CP pulse width	t_w	see Figure 6	$V_{CC}=2.0V$	80	14	- ns
			$V_{CC}=4.5V$	16	5	- ns
			$V_{CC}=6.0V$	14	4	- ns
$\bar{MR}$ pulse width	t_w	see Figure 7	$V_{CC}=2.0V$	60	17	- ns
			$V_{CC}=4.5V$	12	6	- ns
			$V_{CC}=6.0V$	10	5	- ns
$\bar{MR}$ to CP recovery time	t_{rec}	see Figure 7	$V_{CC}=2.0V$	60	17	- ns
			$V_{CC}=4.5V$	12	6	- ns
			$V_{CC}=6.0V$	10	5	- ns
DSA and DSB to CP set-up time	t_{su}	see Figure 8	$V_{CC}=2.0V$	60	8	- ns
			$V_{CC}=4.5V$	12	3	- ns
			$V_{CC}=6.0V$	10	2	- ns
DSA and DSB to CP hold time	t_h	see Figure 8	$V_{CC}=2.0V$	+4	-6	- ns
			$V_{CC}=4.5V$	+4	-2	- ns
			$V_{CC}=6.0V$	+4	-2	- ns
CP maximum frequency	f_{max}	see Figure 6	$V_{CC}=2.0V$	6	23	- MHz
			$V_{CC}=4.5V$	30	71	- MHz
			$V_{CC}=5.0V; C_L=15pF$	-	78	- MHz
			$V_{CC}=6.0V$	35	85	- MHz
power dissipation capacitance	C_{PD}	per package; $V_I = GND \text{ to } V_{CC}$	-	40	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = (C_{PD} \times V_{CC}^2 \times f_i \times N) + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where: f_i =input

frequency in MHz;

f_o =output frequency in MHz;

C_L =output load capacitance in pF;

V_{CC} =supply voltage in V;

N =number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

AC Characteristics 2(T_{amb} = -20°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CP to Q _n propagation delay	t _{pd}	see Figure 6	V _{CC} =2.0V	-	215	ns
			V _{CC} =4.5V	-	43	ns
			V _{CC} =6.0V	-	37	ns
$\overline{\text{MR}}$ to Q _n propagation delay	t _{PHL}	see Figure 7	V _{CC} =2.0V	-	175	ns
			V _{CC} =4.5V	-	35	ns
			V _{CC} =6.0V	-	30	ns
transition time	t _t	see Figure 6	V _{CC} =2.0V	-	95	ns
			V _{CC} =4.5V	-	19	ns
			V _{CC} =6.0V	-	16	ns
CP pulse width	t _w	see Figure 6	V _{CC} =2.0V	100	-	ns
			V _{CC} =4.5V	20	-	ns
			V _{CC} =6.0V	17	-	ns
$\overline{\text{MR}}$ pulse width	t _w	see Figure 7	V _{CC} =2.0V	75	-	ns
			V _{CC} =4.5V	15	-	ns
			V _{CC} =6.0V	13	-	ns
$\overline{\text{MR}}$ to CP recovery time	t _{rec}	see Figure 7	V _{CC} =2.0V	75	-	ns
			V _{CC} =4.5V	15	-	ns
			V _{CC} =6.0V	13	-	ns
DSA and DSB to CP set-up time	t _{su}	see Figure 8	V _{CC} =2.0V	75	-	ns
			V _{CC} =4.5V	15	-	ns
			V _{CC} =6.0V	13	-	ns
DSA and DSB to CP hold time	t _h	see Figure 8	V _{CC} =2.0V	4	-	ns
			V _{CC} =4.5V	4	-	ns
			V _{CC} =6.0V	4	-	ns
CP maximum frequency	f _{max}	see Figure 6	V _{CC} =2.0V	5	-	MHz
			V _{CC} =4.5V	24	-	MHz
			V _{CC} =6.0V	28	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.[2] t_t is the same as t_{THL} and t_{TLH}.**Measurement Points**

Type	Input	Output		
	V _M	V _M	V _X	V _Y
SN74LS164	0.5×V _{CC}	0.5×V _{CC}	0.1×V _{CC}	0.9×V _{CC}

Test Data

Type	Input		Load	Test
	V _I	t _r , t _f	C _L	
SN74LS164	V _{CC}	6.0ns	15pF, 50pF	t _{PLH} , t _{PHL}

Testing Circuit

AC Testing Circuit

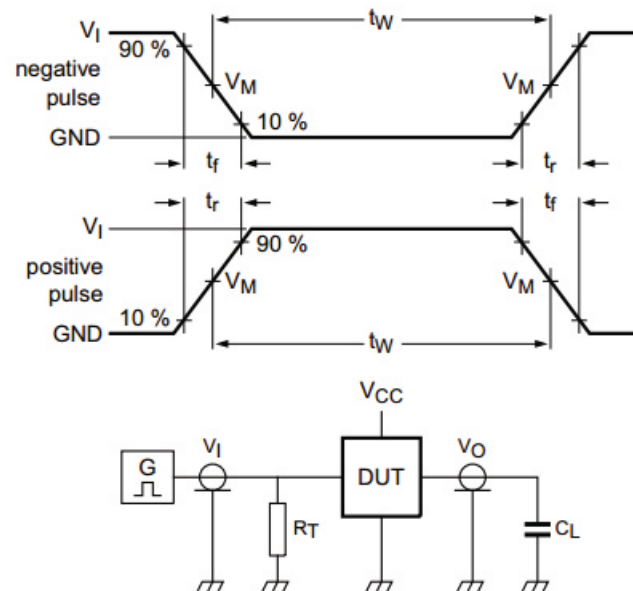


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

C_L =load capacitance including jig and probe capacitance.

R_T =termination resistance should be equal to the output impedance Z_o of the pulse generator.

AC Testing Waveforms

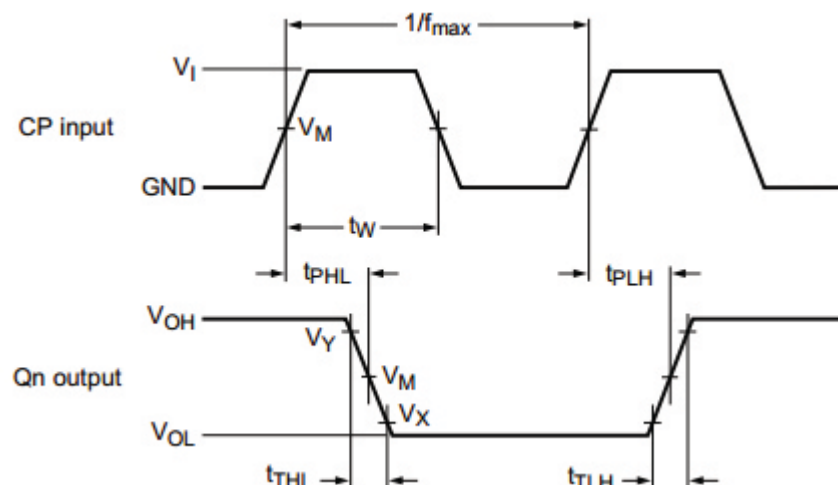


Figure 6. Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency

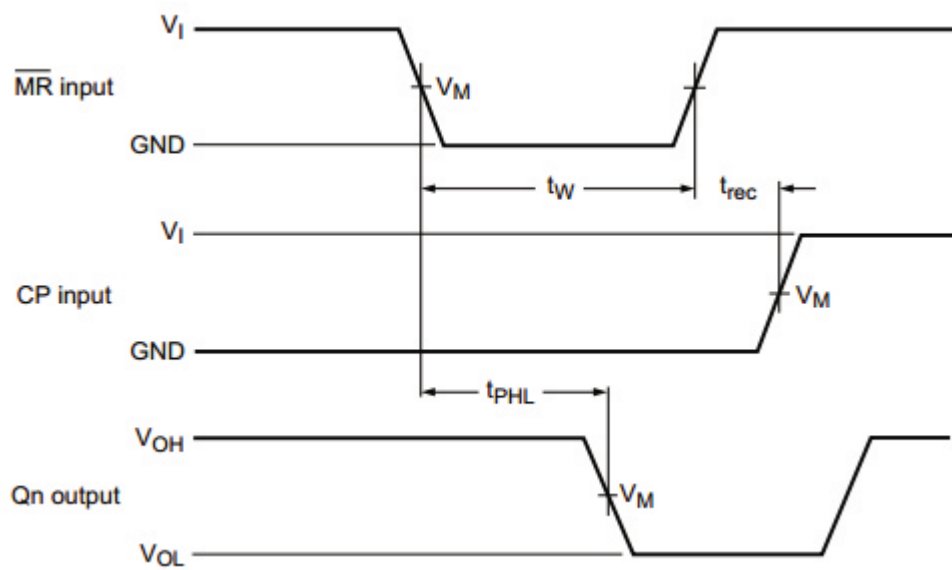


Figure 7. Waveforms showing the master reset (MR) pulse width, the master reset to output Q_n propagation delays and the master reset to clock (CP) removal time

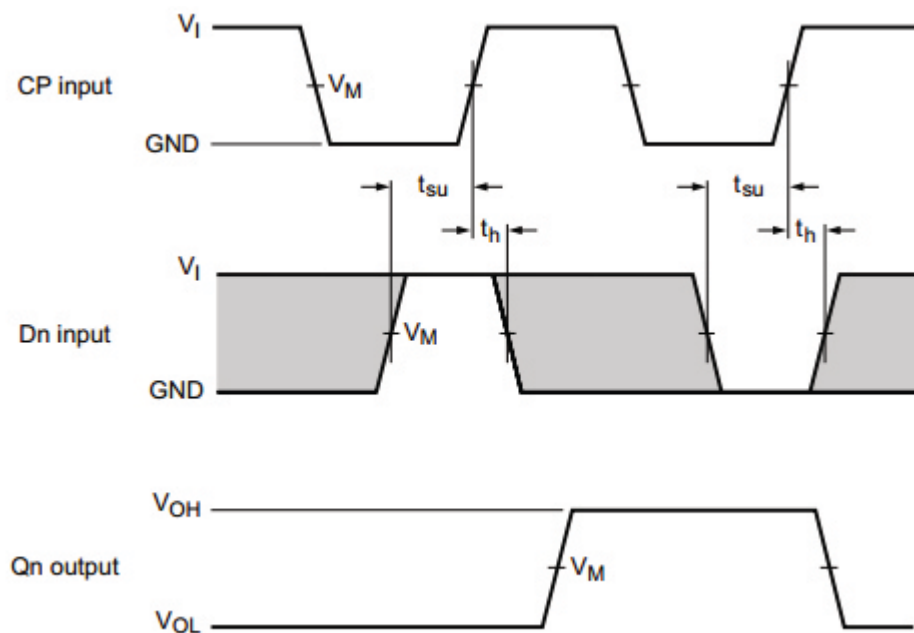
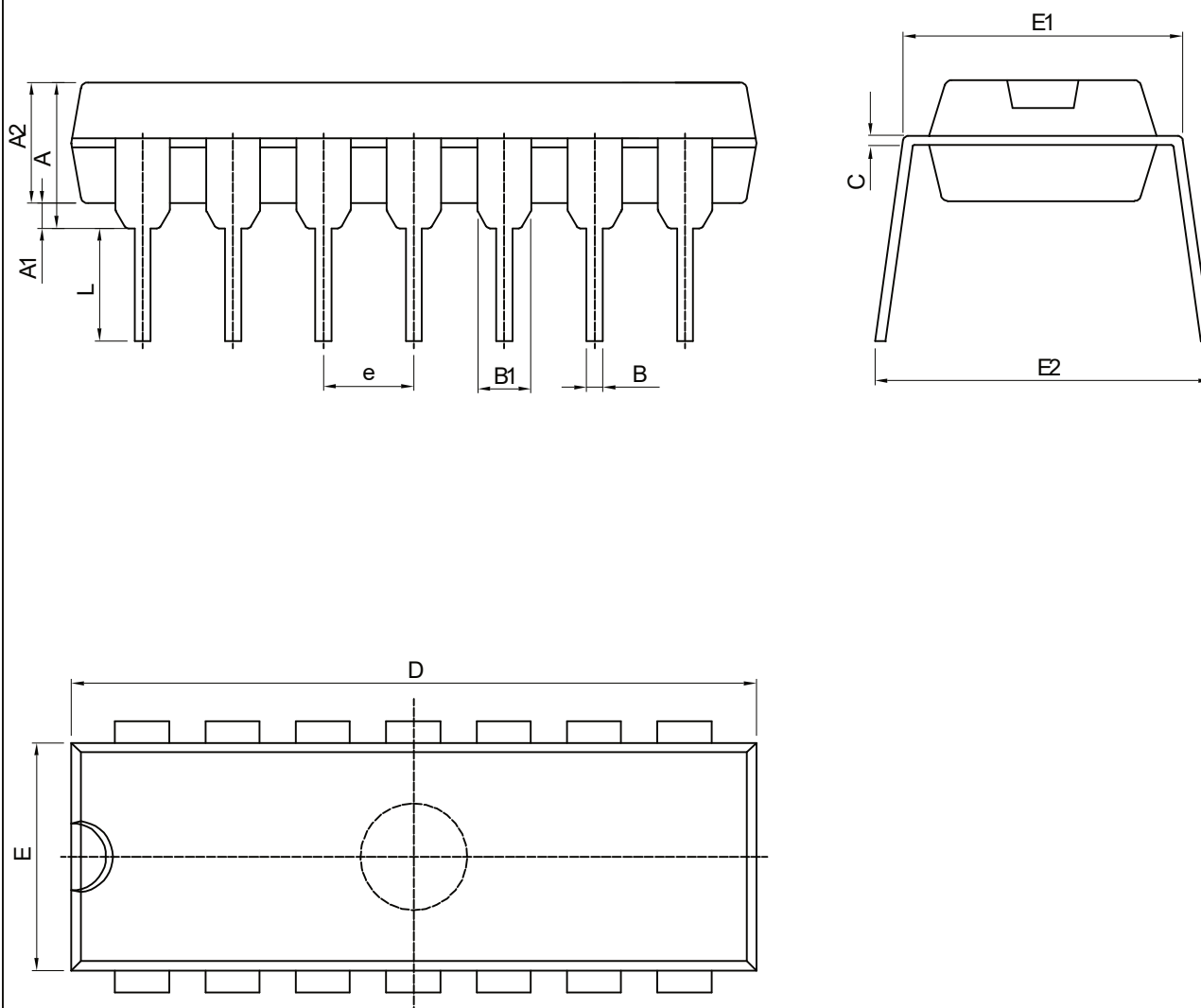


Figure 8. Waveforms showing the data set-up and hold times for Dn inputs

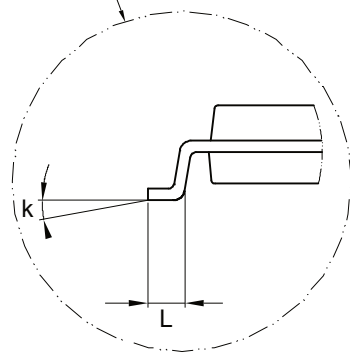
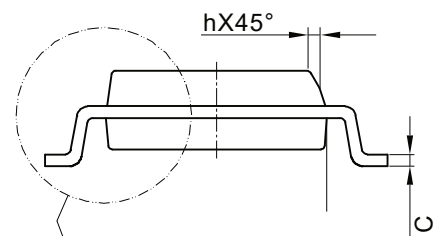
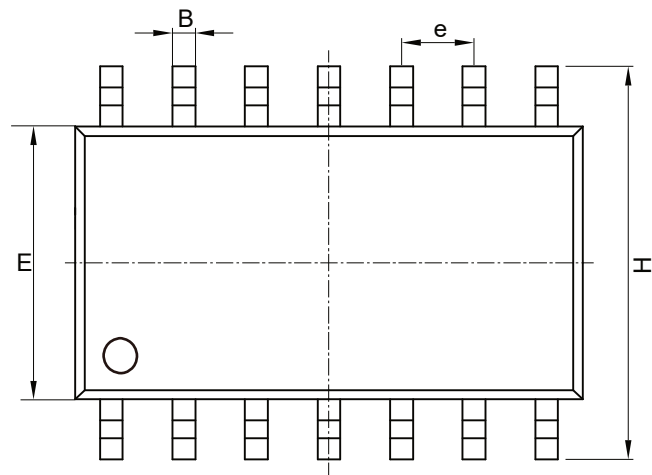
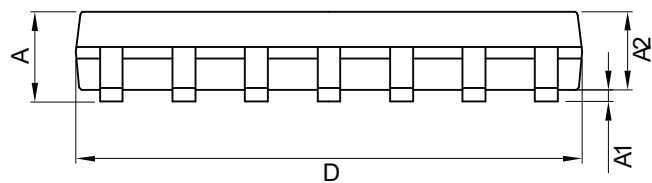
Package Information**c DIP-14**

Symbol	Size	Dimensions In Millimeters		Symbol	Size	Dimensions In Inches	
		Min(mm)	Max(mm)			Min(in)	Max(in)
A		3.710	4.310	A		0.146	0.170
A1		0.510		A1		0.020	
A2		3.200	3.600	A2		0.126	0.142
B		0.380	0.570	B		0.015	0.022
B1		1.524(BSC)		B1		0.060(BSC)	
C		0.204	0.360	C		0.008	0.014
D		18.800	19.200	D		0.740	0.756
E		6.200	6.600	E		0.244	0.260
E1		7.320	7.920	E1		0.288	0.312
e		2.540(BSC)		e		0.100(BSC)	
L		3.000	3.600	L		0.118	0.142
E2		8.400	9.000	E2		0.331	0.354



c SOP-14

Symbol \ Size	Dimensions In Millimeters		Symbol \ Size	Dimensions In Inches	
	Min (mm)	Max (mm)		Min (in)	Max (in)
A	1.350	1.750	A	0.050	0.068
A1	0.100	0.250	A1	0.004	0.009
A2	1.100	1.650	A2	0.040	0.060
B	0.330	0.510	B	0.010	0.020
C	0.190	0.250	C	0.007	0.009
D	8.550	8.750	D	0.330	0.340
E	3.800	4.000	E	0.150	0.150
e	1.27		e	0.05	
H	5.800	6.200	H	0.220	0.240
h	0.250	0.500	h	0.009	0.020
L	0.400	1.270	L	0.015	0.050
k	8° (max)		k	8° (max)	



c TSSOP-14

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.500	E1	0.169	0.176
e	0.65		e	0.0256	
L	0.450	0.750	L	0.018	0.030
L1	1.00		L1	0.039	
k	0°	8°	k	0°	8°

