Description

The 74HC/HCT4053 is a triple single-pole double-throw analog switch (3× SPDT) suitable for use in analog or digital 2:1 multiplexer/demultiplexer applications. Each switch features a digital select input (Sn), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ). A digital enable input ($\overline{E}$) is common to all switches. When $\overline{E}$ is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features:

- Wide analog input voltage range from -4.5V to +4.5V
- Wide supply voltage range
  74HC4053: from 3V to 9V
- Low ON resistance:
  – 80 Ω (typical) at V_{CC} - V_{EE} = 4.5 V
  – 70 Ω (typical) at V_{CC} - V_{EE} = 6.0 V
  – 60 Ω (typical) at V_{CC} - V_{EE} = 9.0 V
- Typical “break before make” built-in
- Specified from -40℃ to +125℃
- Packaging information: DIP16/SOP16

Applications:

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	- [1]		-0.5	+11.0	V
input clamping current	I_{IK}	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
switch clamping current	I_{SK}	$V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V		-	±20	mA
switch current	I_{SW}	-0.5 V < V_{SW} < $V_{CC} + 0.5$ V		-	±25	mA
supply current	I_{EE}	-		-	±20	mA
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-	-50	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
power dissipation	P	per switch		-	100	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP	260		℃

Note:

[1] To avoid drawing V_{CC} current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminals nYn, and in this case there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed V_{CC} or V_{EE}.

Block Diagram

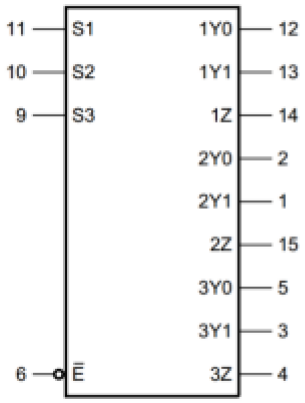


Figure 1. Logic symbol

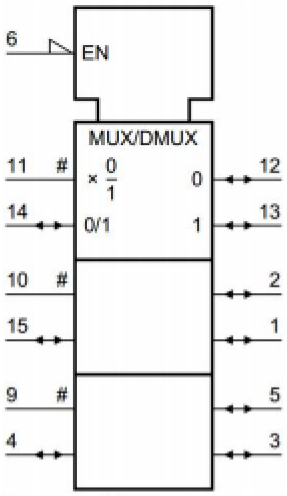


Figure 2. IEC logic symbol

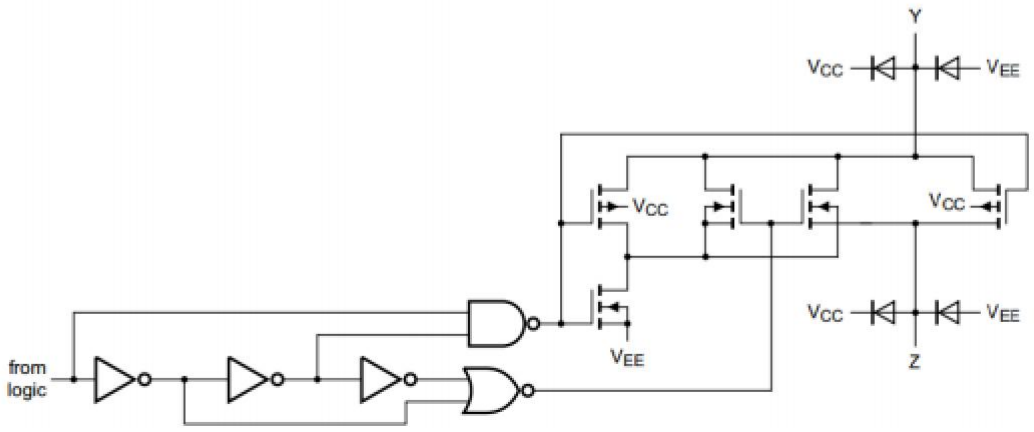


Figure 3. Schematic diagram (one switch)

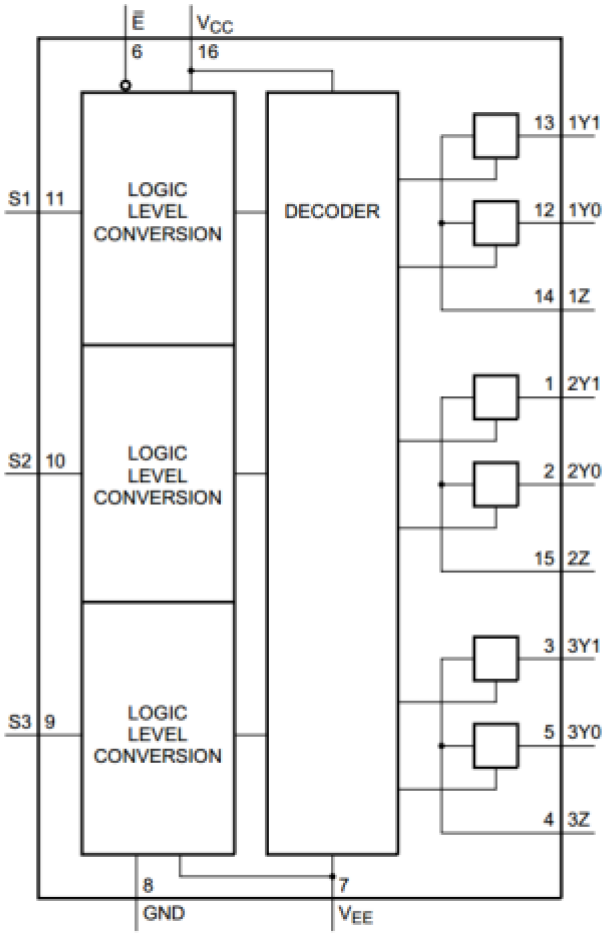
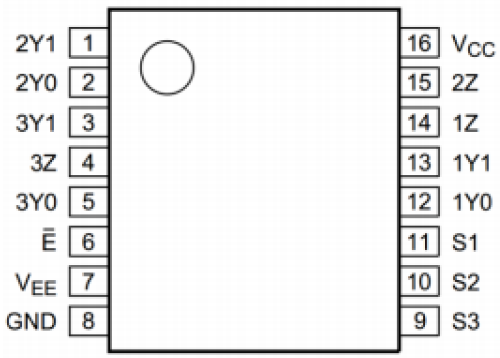


Figure 4. Functional diagram

Pin Configurations



Pin No.	Pin Name	Description
1	2Y1	independent input or output
2	2Y0	independent input or output
3	3Y1	independent input or output
4	3Z	common output or input
5	3Y0	independent input or output
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	supply voltage
8	GND	ground supply voltage
9	S3	select input
10	S2	select input
11	S1	select input
12	1Y0	independent input or output
13	1Y1	independent input or output
14	1Z	common output or input
15	2Z	common output or input
16	V_{CC}	supply voltage

Function Table

Input		Channel ON
$\overline{E}$	Sn	
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	switches off

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	V_{CC} - GND	3.0	5.0	9.0	V
		V_{CC} - V_{EE}	3.0	5.0	9.0	V
input voltage	V_I	-	0	-	V_{CC}	V
switch voltage	V_{SW}	-	V_{EE}	-	V_{CC}	V
ambient temperature	T_{amb}	in free air	-40	-	+125	℃
input transition rise and fall rate	$\Delta t/\Delta V$	V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V
		V_{CC} = 9.0 V	-	-	31	ns/V

DC Characteristics

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
ON resistance (peak)	$R_{ON(peak)}$	V_{is} = V_{CC} to V_{EE}; I_{SW} = 1000 uA	V_{CC} = 4.5 V; V_{EE} = 0 V	-	100	180	Ω
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	90	160	Ω
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	70	130	Ω
ON resistance (rail)	$R_{ON(rail)}$	V_{is} = V_{EE}; I_{SW} = 1000 uA	V_{CC} = 4.5 V; V_{EE} = 0 V	-	80	140	Ω
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	70	120	Ω
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	60	105	Ω
		V_{is} = V_{CC}; I_{SW} = 1000 uA	V_{CC} = 4.5 V; V_{EE} = 0 V	-	90	160	Ω
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	80	140	Ω
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	65	120	Ω
ON resistance mismatch between channels	ΔR_{ON}	V_{is} = V_{CC} to V_{EE}	V_{CC} = 4.5 V; V_{EE} = 0 V	-	9	-	Ω
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	8	-	Ω
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	6	-	Ω

AC Characteristics

(T_{amb}=25℃, GND = 0 V; t_r= t_f= 6 ns; C_L= 50 pF; unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	V_{is} to V_{os}; R_L = ∞ Ω; see Figure 9[1]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	5	12	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	4	10	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	4	8	ns
turn-on time	t_{on}	$\overline{E}$ to V_{os}; R_L = ∞ Ω; see Figure 10[2]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	20	44	ns
			V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF	-	17	-	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	16	37	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	15	31	ns
		Sn to V_{os}; R_L = ∞ Ω; see Figure 10[2]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	25	44	ns
			V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF	-	21	-	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	20	37	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	15	31	ns
turn-off time	t_{off}	$\overline{E}$ to V_{os}; R_L = 1 kΩ; see Figure 10[3]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	21	42	ns
			V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF	-	18	-	ns
			V_{CC} = 6.0 V; V_{EE} = 0 V	-	17	36	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	15	29	ns
		Sn to V_{os}; R_L = 1 kΩ; see Figure 10[3]	V_{CC} = 4.5 V; V_{EE} = 0 V	-	20	42	ns
			V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF	-	17	-	ns

			V_{CC} = 6.0 V; V_{EE} = 0 V	-	16	36	ns
			V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	15	29	ns
power dissipation capacitance	C_{PD}	per switch; V_I = GND to V_{CC} [4]		-	36	-	pF

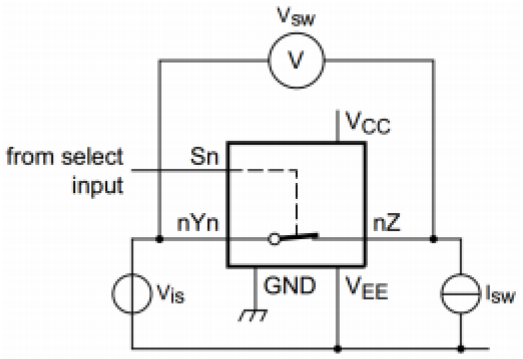
[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_{en} is the same as t_{PZH} and t_{PZL}.
[3] t_{off} is the same as t_{PHZ} and t_{PLZ}.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{SW}) \times V_{CC}^2 \times f_O\}$ where:

f_i = input frequency in MHz;
f_O = output frequency in MHz;
N = number of inputs switching;
$\Sigma\{(C_L + C_{SW}) \times V_{CC}^2 \times f_O\}$ = sum of outputs;
C_L = output load capacitance in pF;
C_{SW} = switch capacitance in pF;
V_{CC} = supply voltage in V.

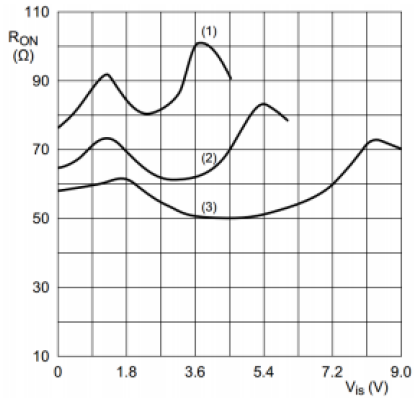
Testing Circuit

DC Testing Circuit



V_{is} = 0V to (V_{CC} -V_{EE})
$R_{ON} = V_{sw}/I_{sw}$

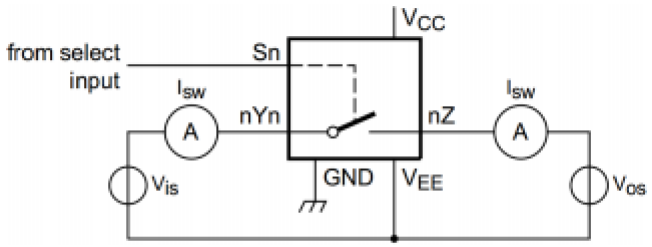
Figure 5. Test circuit for measuring R_{ON}



V_{is} = 0V to (V_{CC} -V_{EE})
(1) V_{CC} = 4.5V
(2) V_{CC} = 6V
(3) V_{CC} = 9V

Figure 6. Typical R_{ON} as a function of input voltage V_{is}

DC Testing Circuit 2



V_{is} = V_{CC} and V_{os} = V_{EE}.
V_{is} = V_{EE} and V_{os} = V_{CC}.

Figure 7. Test circuit for measuring OFF-state current

AC Testing Waveforms

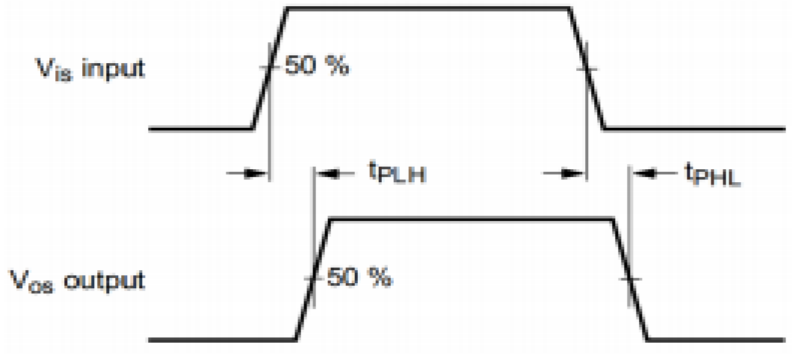
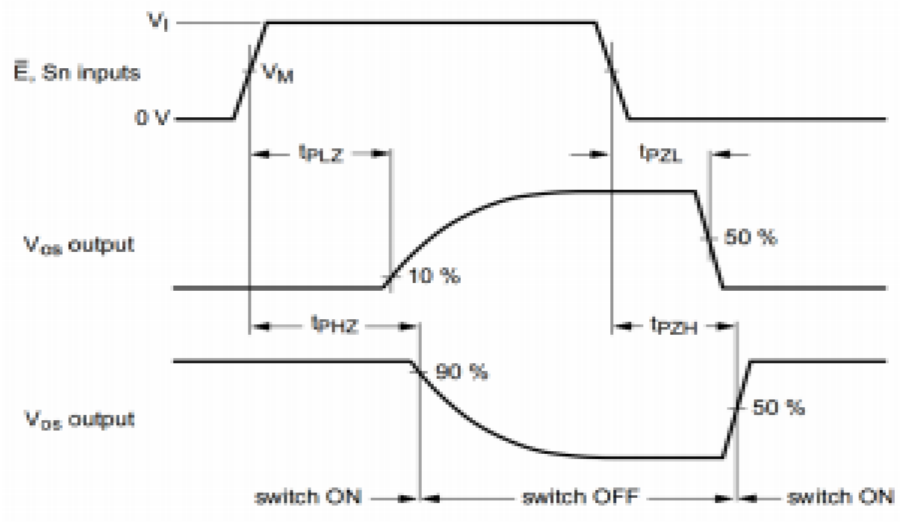


Figure 9. Input (V_{is}) to output (V_{os}) propagation delays



74HC4053: $V_M = 0.5 \times V_{CC}$.