

Quad op amp IC

Overview

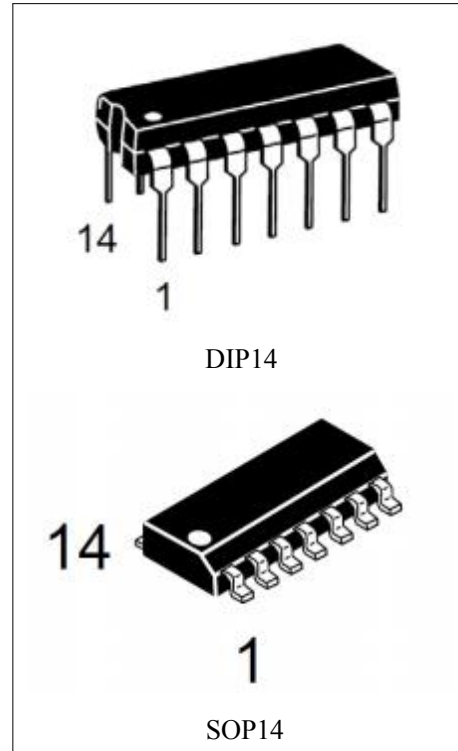
This circuit is a high-performance, with four independent operational amplifiers, including a phase compensation circuit, suitable for tape recorders and tone systems as tone equalization network, and also used in other occasions. Adopt 14-lead dual in-line plastic package DIP14, power consumption 720mW, and SMD SOP14 package, power consumption 400mW.

Main feature

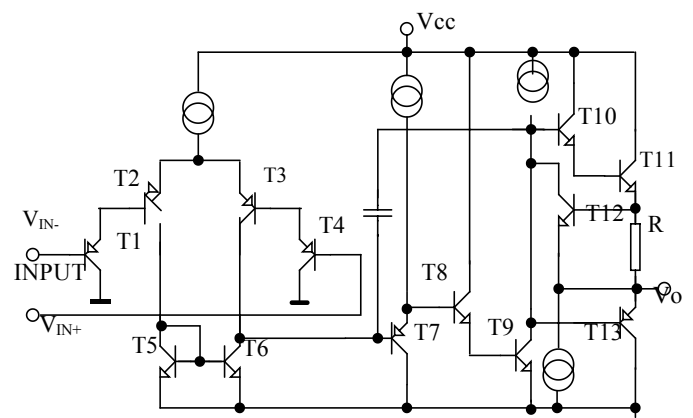
- No external phase compensation circuit required
- Wide supply voltage range: when single supply, $V_{cc}=3\sim 32V$, when dual power supply, $V_{cc}=\pm 1.5V\sim 16V$
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- Low power consumption: $I_{cc}=0.6mA$ (typical) ($R_L=\infty$)
- Input voltage range close to ground

Introduction

LM324 is composed of four identical operational amplifiers. The unit circuit is shown in the figure, and its working principle is briefly described as follows: The input signal is applied to the bases of T1 and T4, and then differentially amplified; T8 and T9 are compositely amplified to form an intermediate stage; The output stage consists of T10~T13. Among them, T12 is a protection tube. When the output current is too large, the voltage drop on R increases to make T12 saturate and conduct, and the collector potential of T12 drops, which is close to $1/2V_{cc}$, so that the push-pull tubes T10, T11 and T13 are cut off, thus protecting effect. Capacitor C is a phase compensation capacitor.



Internal circuit diagram



Pin end function symbol

Terminal serial number	Function	Symbol	Terminal serial number	Function	Symbol
1	output 1	OUT1	8	output 3	OUT3
2	reverse input 1	IN- (1)	9	reverse input 3	IN- (3)
3	Positive input 1	IN+(1)	10	Positive input 3	IN+(3)
4	power supply	Vcc	11	land	GND
5	Positive input 2	IN+(2)	12	Positive input 4	IN+(4)
6	reverse input 2	IN- (2)	13	reverse input 4	IN- (4)
7	output 2	OUT2	14	output 4	OUT4

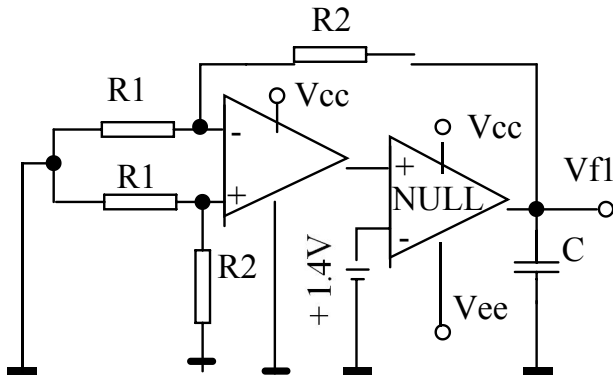
Limiting Parameters (Absolute Maximum Ratings, if not otherwise specified, Tamb=25°C)

Parameter	Symbol	Test Conditions	Rated value	Unit
voltage	Vcc		32	V
Differential input voltage	V _{ID}		32	V
Maximum input voltage	V _{IN}		-0.3~32	V
allowable power consumption	P _D	DIP SOP	720 400	mW
Operating temperature	T _{opr}		0~+70	°C
Storage temperature	T _{stg}		-55~+125	°C

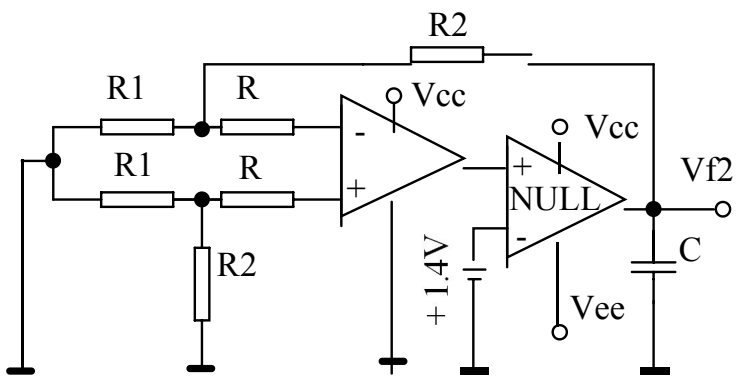
Electrical Characteristics (Vcc=5V, Tamb=25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min Value	Typ Value	Max value	Unit
Offset input voltage	V _{IO}			±2	±5	mV
Input offset current	I _{IO}	I _{in(+)} /I _{in(-)}		±5	±50	nA
Input bias current	I _{BA}			45	250	nA
Common Mode Input Voltage Range	V _{ICM}		0		Vcc-1.5	V
Common Mode Rejection Ratio	K _{CMR}		65	80		dB
Strong signal voltage gain	G _V	Vcc=15V, R _L ≥ 2 kΩ	25	100		V/mV
Output voltage range	V _O		0		Vcc-1.5	V
Power Ripple Rejection Ratio	PSRR		65	100		dB
channel separation	C _s	f=1kHz~20kHz		120		dB
Static current consumption(1)	I _{cc}	Vcc=5V		0.6	2	mA
Static current consumption(2)	I _{cc}	Vcc=30V		1.5	3	mA
output current	I _O	V _{in+} =1V, V _{in-} =0V	20	35		mA
Output sink current	I _O	V _{in+} =0V, V _{in-} =1V	10	13		mA

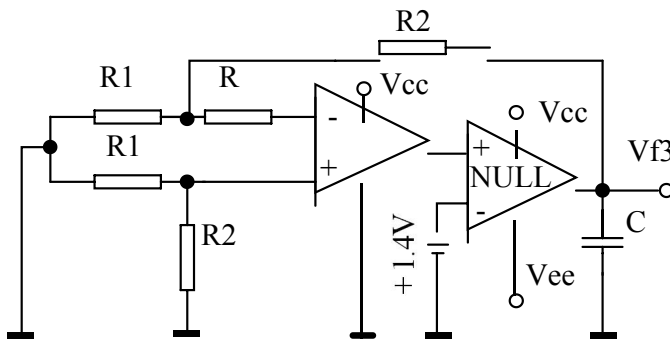
Test schematic diagram (Note: NULL refers to zero amplifier)



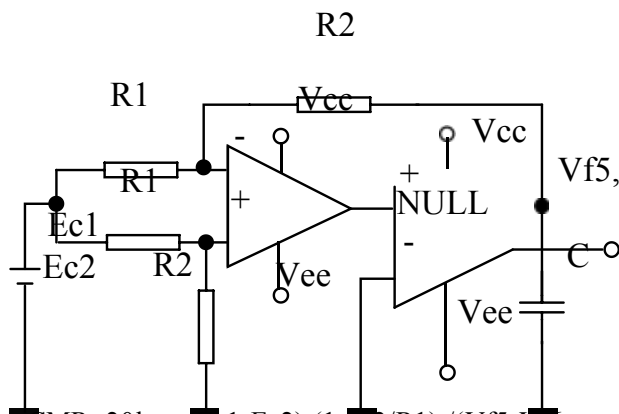
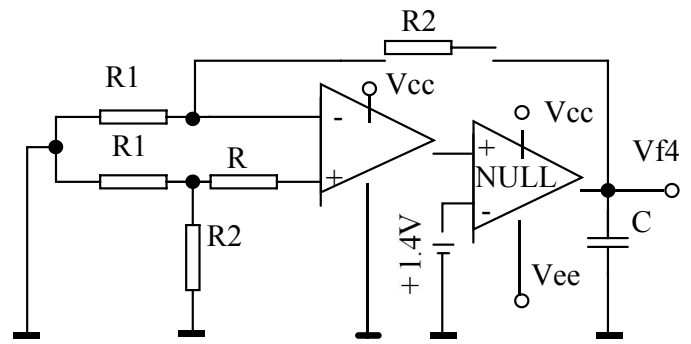
$V_{io} = V_{f1} / (1 + R2/R1)$
Input Offset Voltage V_{io} Test Chart



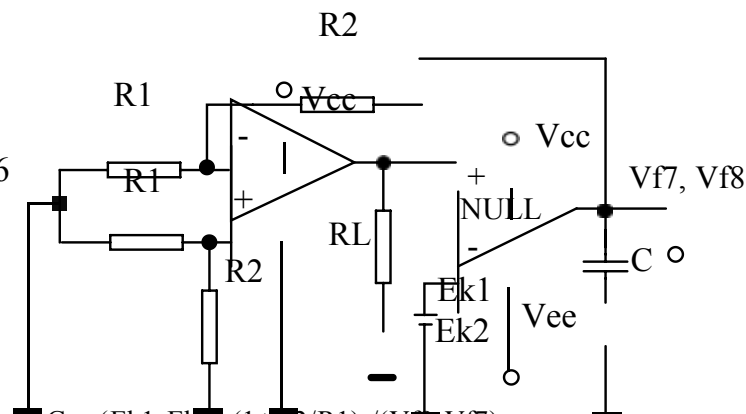
$I_{io} = (V_{f2} - V_{f1}) / R(1 + R2/R1)$
Input Offset Current I_{io} Test Chart



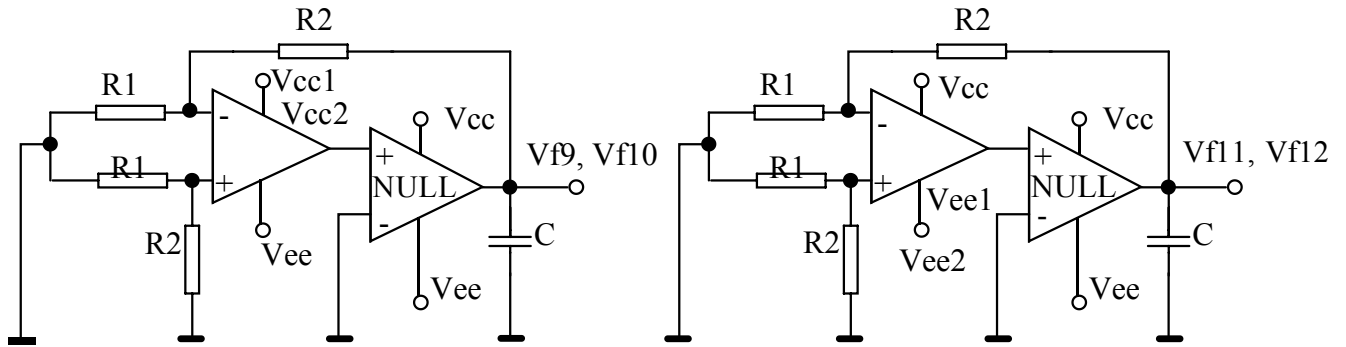
$I_{BA} = (V_{f4} - V_{f3}) / 2R(1 + R2/R1)$
Input Bias Current I_{BA} Test Chart



$CMR = 20 \log (E_{c1} - E_{c2}) (1 + R2/R1) / (V_{f5} - V_{f6})$
Common Mode Rejection Ratio CMR and Common Mode Input Voltage Range V_{ICM} Test Chart

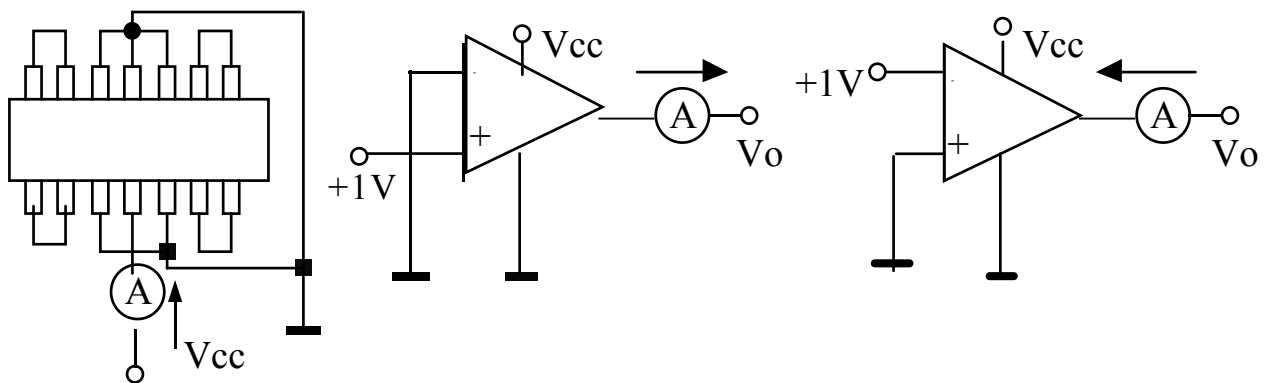


$G_v = (E_{k1} - E_{k2}) (1 + R2/R1) / (V_{f7} - V_{f8})$
Voltage Gain G_v Test Chart

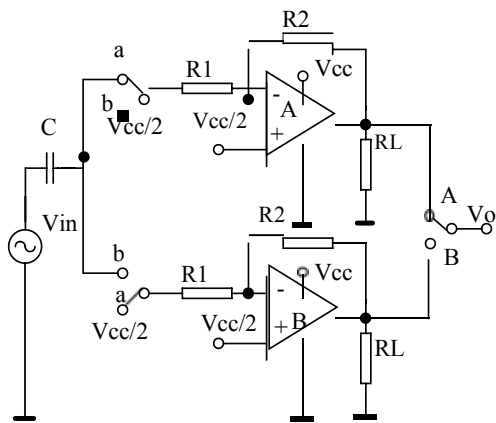


$$PSRR(+)=20\log (V_{cc1}-V_{cc2}) (1+R2/R1) / (V_{f9}-V_{f10}) \quad PSRR(-)=20\log (V_{ee1}-V_{ee2}) (1+R2/R1) / (V_{f11}-V_{f12})$$

Power Supply Ripple Rejection PSRR Test Chart



Consumption current Icc and output current Io test chart

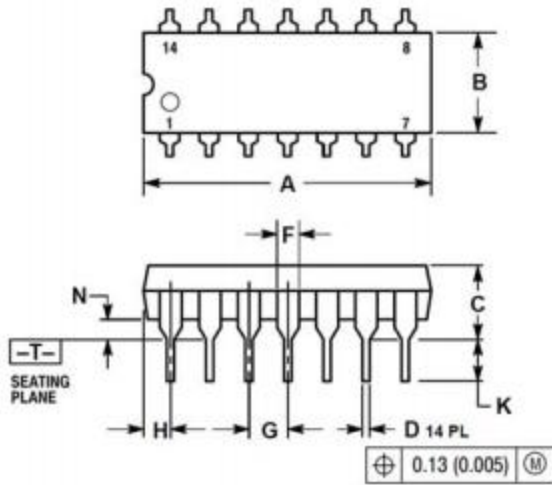


Channel Separation Cs Test Chart

SW: A
 $Cs(A \rightarrow B) = 20 \log(R2 * VOA) / (R1 * VOB)$

SW: B
 $Cs(B \rightarrow A) = 20 \log(R2 * VOB) / (R1 * VOA)$

Package information:

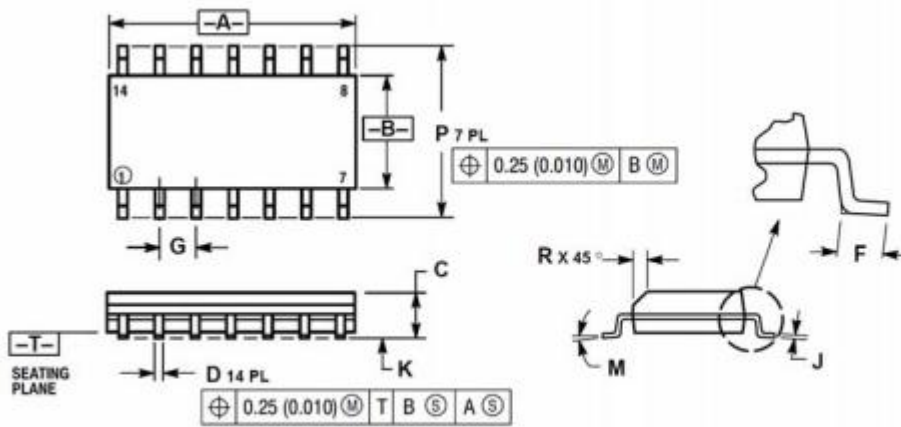


DIP14

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.60
B	0.240	0.290	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	----		10 [°]	
N	0.015	0.039	0.38	1.01



SOP14

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 [°] 7 [°]		0 [°] 7 [°]	
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019