2018 Serie

Performance Specification

Model	V_{max} (V)	I_{max} (A)	I_{hold} @25℃ (A)	I_{trip} @25℃ (A)	P_d Typ. (W)	Maximum Time To Trip Current (A)	Maximum Time To Trip Time (Sec)	Resistance Ri_{min} (Ω)	Resistance Ri_{typ} (Ω)	Resistance $R1_{max}$ (Ω)
BpS18-300-60	60	100	0.30	0.60	0.9	1.5	3.00	0.500	1.200	2.300
BpS18-500-60	60	100	0.55	1.20	1.0	2.5	3.00	0.200	0.600	1.000
BpS18A01.10-15	15	100	1.10	2.20	1.1	8.0	0.40	0.060	0.110	0.360
BpS18A01.10-33	8	40	1.60	2.80	0.8	8.0	1.00	0.040	-	0.099
BpS18A01.50-15	15	100	1.50	3.00	1.1	8.0	0.80	0.050	0.060	0.170
BpS18A02.00-10	10	100	2.00	4.00	1.1	8.0	2.40	0.030	0.045	0.100

I_{hold} = Hold Current. Maximum current device will not trip in 25℃ still air.
Itrip = Trip Current. Minimum current at which the device will always trip in 25℃ still air.
V_{max} = Maximum operating voltage device can withstand without damage at rated current (Imax).
I_{max} = Maximum fault current device can withstand without damage at rated voltage (Vmax).
Pd = Maximum power dissipation when device is in the tripped state in 25℃ still air environment at rated voltage.
Rimin/max = Minimum/Maximum device resistance prior to tripping at 25℃.
$R1_{max}$ = Maximum device resistance is measured one hour post reflow.
CAUTION : Operation beyond the specified ratings may result in damage and possible arcing and flame.

Environmental Specifications

Test	Conditions	Resistance change
Passive aging	+85°C, 1000 hrs.	±5% typical
Humidity aging	+85℃, 85% R.H. , 168 hours	±5% typical
Thermal shock	+85℃ to -40℃, 20 times	±33% typical
Resistance to solvent	MIL-STD-202,Method 215	No change
Vibration	MIL-STD-202,Method 201	No change
Ambient operating conditions :	- 40 ℃ to 85 ℃	
Maximum surface temperature of the device in the tripped state is 125 ℃		

AGENCY APPROVALS : UL pending.

I_{hold} versus temperature

Model	Maximum ambient operating temperature (Tmao) vs. hold current (Ihold)								
	-40℃	-20℃	0℃	25℃	40℃	50℃	60℃	70℃	85℃
BpS18-300-60	0.48	0.42	0.35	0.30	0.24	0.21	0.17	0.15	0.10
BpS18-500-60	0.87	0.77	0.67	0.55	0.46	0.41	0.36	0.31	0.23
BpS18A01.10-15	1.71	1.52	1.32	1.10	0.94	0.84	0.74	0.64	0.50
BpS18A01.50-15	2.38	2.10	1.82	1.50	1.27	1.13	0.99	0.85	0.64
BpS18A02.00-10	2.95	2.65	2.35	2.00	1.74	1.59	1.44	1.29	1.06

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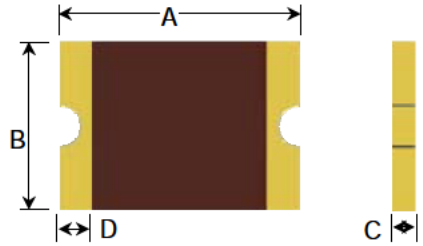
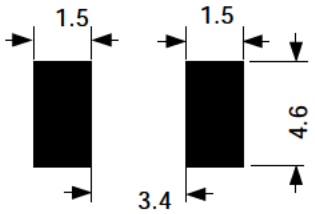
Construction and Dimension (Unit:mm)

Model	A		B		C		D
	Min.	Max.	Min.	Max.	Min.	Max.	Min.
BpS18-300-60	4.72	5.44	4.22	4.93	0.60	1.10	0.30
BpS18-500-60	4.72	5.44	4.22	4.93	0.60	1.10	0.30
BpS18A01.10-15	4.72	5.44	4.22	4.93	0.45	0.80	0.30
BpS18A01.10-33	4.72	5.44	4.22	4.93	0.45	0.80	0.30
BpS18A01.50-15	4.72	5.44	4.22	4.93	0.45	0.80	0.30
BpS18A02.00-10	4.72	5.44	4.22	4.93	0.45	0.80	0.30

Dimensions & Marking



Recommended pad layout (mm)



Termination pad characteristics

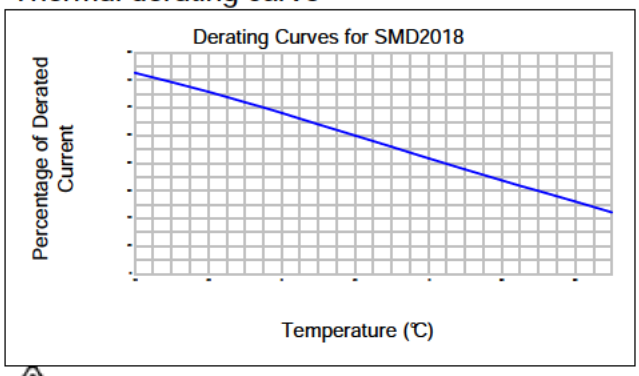
Terminal pad materials： Tin-Plated Nickle-Copper or Gold-Plated Nickle-Copper

Terminal pad solderability： Meets EIA specification RS186-9E and ANSI/J-STD-002 Category 3.

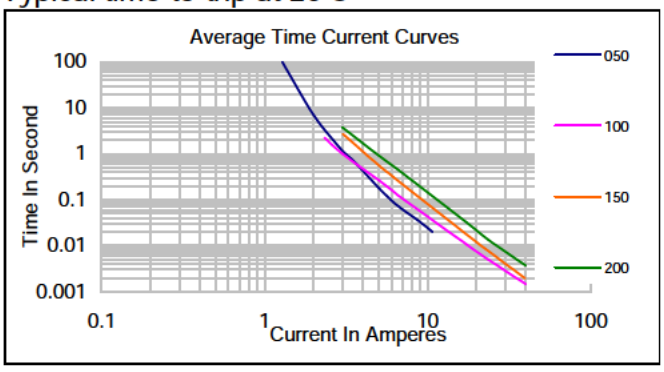
Rework

Use standard industry practices, the removal device must be replaced with a fresh one.

Thermal derating curve



Typical time-to-trip at 25℃



WARNING:

· Use PPTC beyond the maximum ratings or improper use may result in device damage and possible electrical arcing and flame.
· PPTC are intended for protection against occasional over current or over temperature fault conditions and should not be used when repeated fault conditions or prolonged trip events are anticipated.
· Device performance can be impacted negatively if devices are handled in a manner inconsistent with recommended electronic, thermal, and mechanical procedures for electronic components.
· Use PPTC with a large inductance in circuit will generate a circuit voltage (L di/dt) above the rated voltage of the PPTC.
· Avoid impact PPTC device its thermal expansion like placed under pressure or installed in limited space.
· Contamination of the PPTC material with certain silicon based oils or some aggressive solvents can adversely impact the performance of the devices. PPTC SMD can be cleaned by standard methods.
· Requests that customers comply with our recommended solder pad layouts and recommended reflow profile. Improper board layouts or reflow profile could negatively impact solderability performance of our devices.