Features

- Industry-standard Architecture
- 12ns Maximum Pin-to-pin Delay
- Zero Power 100μA Maximum Standby Power (Input Transition Detection)
- CMOS and TTL Compatible Inputs and Outputs
- Advanced Electrically ErasableTechnology
 - Reprogrammable
 - 100% Tested
- Latch Feature Holds Inputs to Previous Logic State
- High-reliability CMOS Process
 - 20 Year Data Retention
 - 100 Erase/Write Cycles
 - 2,000V ESD Protection
 - 200mA Latchup Immunity
- Industrial Temperature Ranges
- Dual-in-line and Surface Mount Standard Pinouts
- PCI Compliant
- Green Package Options (Pb/Halide-free/RoHS Compliant) Available

1. Description

The Atmel® ATF22V10CZ/CQZ is a high-performance CMOS (electrically erasable) programmable logic device (PLD) which utilizes The Atmel proven electrically erasable Flash memory technology. Speeds down to 12ns with zero standby power dissipation are offered. All speed ranges are specified over the full 5V $\pm 10\%$ range for industrial temperature ranges; 5V $\pm 5\%$ for commercial range 5-volt devices. The ATF22V10CZ/CQZ provides a low voltage and edge-sensing "zero" power CMOS PLD solution with "zero" standby power (5 μ A typical). The ATF22V10CZ/CQZ provides a "zero" power CMOS PLD solution with 5V operating voltages, powering down automatically to the zero power-mode through The Atmel patented Input Transition Detection (ITD) circuitry when the device is idle, offering "zero" (100 μ A worst case) standby power. This feature allows the user to manage total system power to meet specific application requirements and enhance reliability. Pin "keeper" circuits on input and output pins eliminate static power consumed by pull-up resistors. The "CQZ" combines the low high-frequency I_{CC} of the "Q" design with the "Z" feature.

The ATF22V10CZ/CQZ incorporates a superset of the generic architectures, which allows direct replacement of the 22V10 family and most 24-pin combinatorial PLDs. Ten outputs are each allocated 8 to 16 product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.



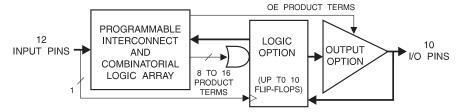
High-performance Electrically Erasable Programmable Logic Device

Atmel ATF22V10CZ Atmel ATF22V10CQZ





Figure 1-1. Block Diagram



2. Pin Configurations

Table 2-1. Pin Configurations (All Pinouts Top View)

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bi-directional Buffers
VCC	+5V Supply

Figure 2-1. TSSOP

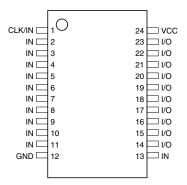
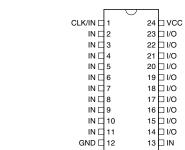
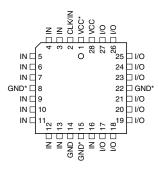


Figure 2-3. PLCC



DIP/SOIC

Figure 2-2.



Note: For PLCC, P1, P8, P15 and P22 can be left unconnected. For superior performance, connect VCC to pin 1 and GND to 8, 15, and 22

3. Absolute Maximum Ratings*

Temperature Under Bias40°C to +85°C
Storage Temperature65°C to +150°C
Voltage on Any Pin with Respect to Ground2.0V to +7.0V ⁽¹⁾
Voltage on Input Pins with Respect to Ground
During Programming2.0V to +14.0V ⁽¹⁾
Programming Voltage with Respect to Ground2.0V to +14.0V ⁽¹⁾

*NOTICE:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

 Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20ns.

4. DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0·C - 70·C	-40·C - 85·C
V _{CC} Power Supply	5V ± 5%	5V ± 10%

4.1 DC Characteristics

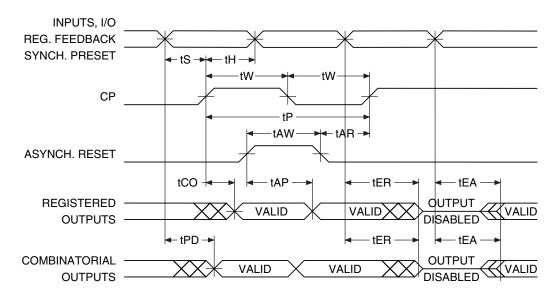
Symbol	Parameter	Condition			Min	Тур	Max	Units	
I _{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$ (Max)					-10	μА	
I _{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$	···				10	μА	
			CZ-12, 15	Com		90	150	mA	
	Clocked Power	V _{CC} = Max	CZ-15	Ind		90	180	mA	
I _{CC}	Supply Current	Outputs Open, f = 15MHz	CQZ-20	Com		40	60	mA	
			CQZ-20	Ind		40	80	mA	
	Power Supply Current,			CZ-12, 15	Com		5	100	μA
. F		rent, $V_{CC} = Max$ $V_{IN} = MAX$ Outputs Open	CZ-15	Ind		5	120	μA	
I _{SB}	Standby		CQZ-20	Com		5	100	μA	
			CQZ-20	Ind		5	120	μA	
I _{OS} ⁽¹⁾	Output Short Circuit Current	V _{OUT} = 0.5V					-130	mA	
V _{IL}	Input Low Voltage				-0.5		0.8	V	
V _{IH}	Input High Voltage				2.0		V _{CC} + 0.75	V	
V _{OL}	Output Low Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = \text{Min},$ $I_{OL} = 16\text{mA}$					0.5	V	
V _{OH}	Output High Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CCIO} = \text{Min},$ $I_{OH} = -4.0\text{mA}$			2.4			V	

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec





4.2 AC Waveforms



4.3 AC Characteristics⁽¹⁾

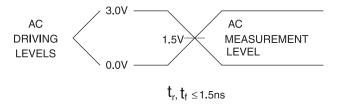
		-	12		15	-2	20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
t _{PD}	Input or Feedback to Non-registered Output	3	12	3	15	3	20	ns
t _{CF}	Clock to Feedback		6		4.5		8	ns
t _{CO}	Clock to Output	2	8	2	8	2	12	ns
t _S	Input or Feedback Setup Time	10		10		14		ns
t _H	Input Hold Time	0		0		0		ns
t _W	Clock Width	6		6		10		ns
f _{MAX}	External Feedback $1/(t_S + t_{CO})$ Internal Feedback $1/(t_S + t_{CF})$ No Feedback $1/(t_P)$		55.5 62 83.3		55.5 69 83.3	38.5 45.5 50.0		MHz MHz MHz
t _{EA}	Input to Output Enable - Product Term	3	12	3	15	3	20	ns
t _{ER}	Input to Output Disable - Product Term	2	15	3	15	3	20	ns
t _{PZX}	OE Pin to Output Enable	2	12	2	15	2	20	ns
t _{PXZ}	OE Pin to Output Disable	2	15	2	15	2	20	ns
t _{AP}	Input or I/O to Asynchronous Reset of Register	3	10	3	15	3	22	ns
t _{SP}	Setup Time, Synchronous Preset	10		10		14		ns
t _{AW}	Asynchronous Reset Width	7		8		20		ns
t _{AR}	Asynchronous Reset Recovery Time	5		6		20		ns
t _{SPR}	Synchronous Preset to Clock Recovery Time	10		10		14		ns

Note: 1. See ordering information for valid part numbers

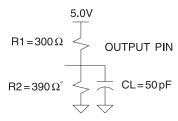
4

4.4 Input Test Waveforms

4.4.1 Input Test Waveforms and Measurement Levels



4.4.2 Output Test Loads



Note: Similar competitors devices are specified with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel devices are tested with sufficient margins to meet compatible device specification conditions.

4.5 Pin Capacitance

Table 4-1. Pin Capacitance (f = 1MHz, $T = 25C^{(1)}$

	Тур	Max	Units	Conditions
C _{IN}	8	10	pF	$V_{IN} = 0V; f = 1.0MHz$
C _{I/O}	8	10	pF	V _{OUT} = 0V; f = 1.0MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested

4.6 Power-up Reset

The registers in the Atmel[®] ATF22V10CZ/CQZ are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST} , all registers will be reset to the low state. The output state will depend on the polarity of the buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

- 1. The V_{CC} rise must be monotonic and start below 0.7V
- 2. The clock must remain stable during T_{PR}
- 3. After T_{PR} occurs, all input and feedback setup times must be met before driving the clock pin high

4.7 Preload of Register Outputs

The ATF22V10CZ/CQZ's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.



5. Electronic Signature Word

There are 64-bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

6. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the Atmel[®] ATF22V10CZ/CQZ fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible. The security fuse should be programmed last, as its effect is immediate.

7. Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See CMOS PLD Programming Hardware and Software Support for information on software/programming.

Figure 7-1. Programming/Erasing Timing

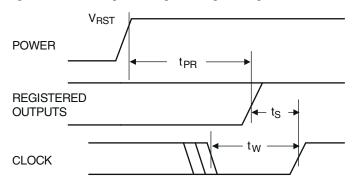


 Table 7-1.
 Programming/Erasing

Parameter	Parameter Description		Max	Units
T _{PR}	Power-up Reset Time	600	1000	ns
V _{RST}	Power-up Reset Voltage	3.8	4.5	V

8. Input and I/O Pull-ups

All Atmel[®] ATF22V10CZ/CQZ family members have internal input and I/O pin-keeper circuits. Therefore, whenever inputs or I/Os are not being driven externally, they will maintain their last driven state. This ensures that all logic array inputs and device outputs are at known states. These are relatively weak active circuits that can be easily overridden by TTL-compatible drivers (see input and I/O diagrams below).

Figure 8-1. Input Diagram

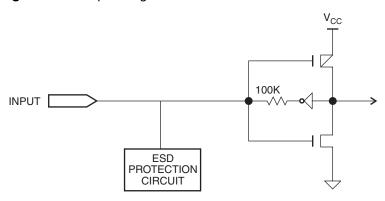
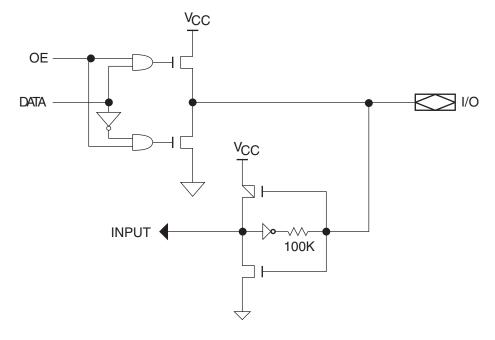


Figure 8-2. I/O Diagram





9. Compiler Mode Selection

Table 9-1. Compiler Mode Selection

	PAL Mode (5828 Fuses)	GAL Mode (5892 Fuses)
Synario	Atmel ATF22V10C (DIP) Atmel ATF22V10C (PLCC)	Atmel ATF22V10C DIP (UES) Atmel ATF22V10C PLCC (UES)
WINCUPL	P22V10 P22V10LCC	G22V10 G22V10LCC

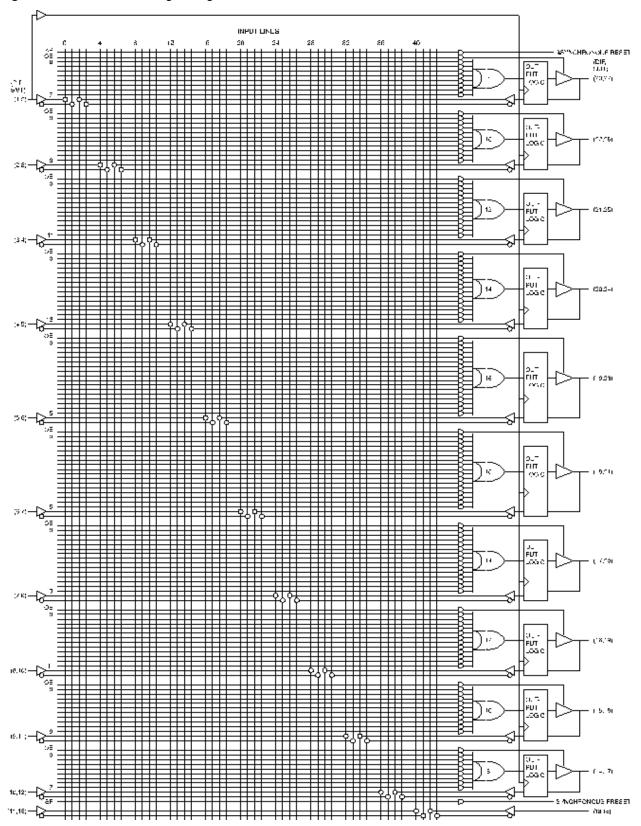
10. Functional Logic Diagram Description

The Functional Logic Diagram describes the Atmel® ATF22V10CZ/CQZ architecture.

The ATF22V10CZ/CQZ has 12 inputs and 10 I/O macrocells. Each macrocell can be configured into one of four output configurations: active high/low, registered/combinatorial output. The universal architecture of the ATF22V10CZ/CQZ can be programmed to emulate most 24-pin PAL devices.

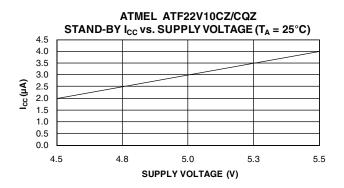
Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF22V10CZ/CQZ. Eight bytes (64-fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

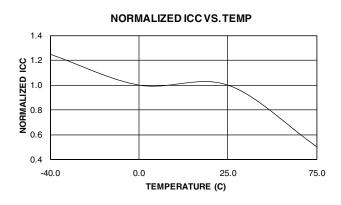
Figure 10-1. Functional Logic Diagram

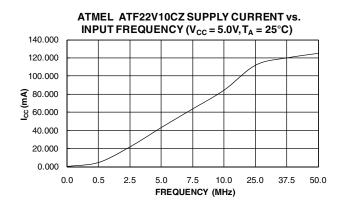


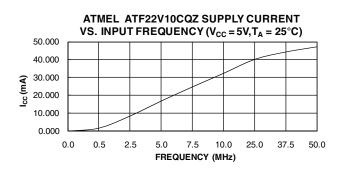


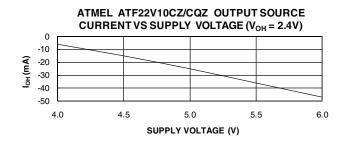


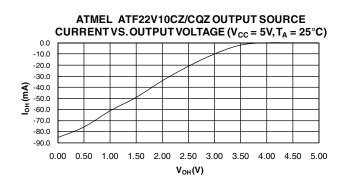


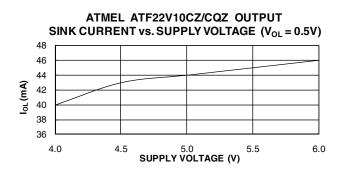


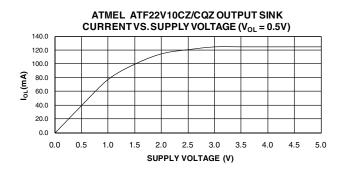




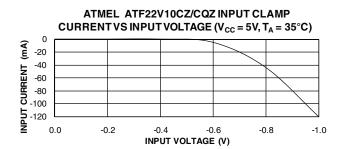


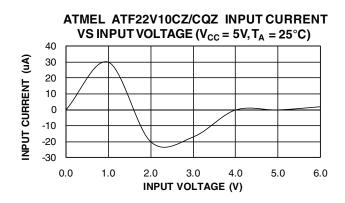


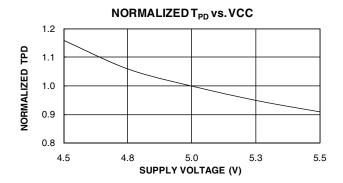


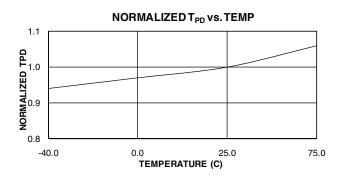


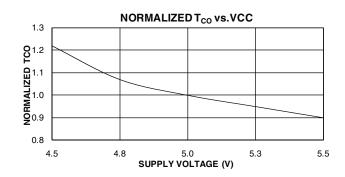
Atmel ATF22V10C(Q)Z

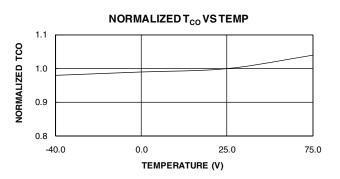


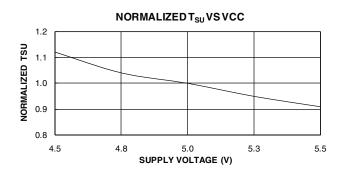


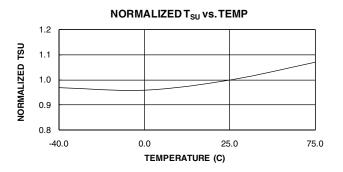






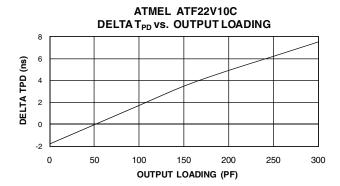


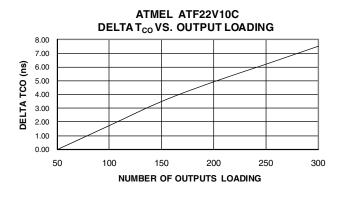


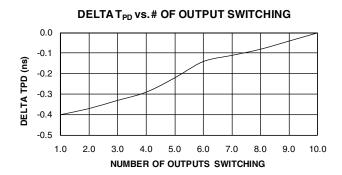


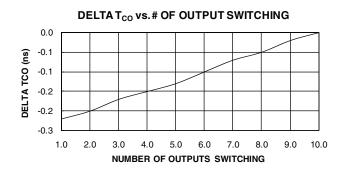












11. Ordering Information

11.1 Standard Package Options

t _{PD} (ns)	t _s (ns)	t _{co} (ns)	Ordering Code	Package	Operation Range
12	10	8	ATF22V10CZ-12JC ATF22V10CZ-12PC ATF22V10CZ-12SC ATF22V10CZ-12XC	28J 24P3 24S 24X	Commercial (0·C to 70·C)
15	10	8	ATF22V10CZ-15JC ATF22V10CZ-15PC ATF22V10CZ-15SC	28J 24P3 24S	Commercial (0·C to 70·C)
15	10	0	ATF22V10CZ-15JI ATF22V10CZ-15PI ATF22V10CZ-15SI	28J 24P3 24S	Industrial (-40·C to +85·C)
20	14	10	ATF22V10CQZ-20JC ATF22V10CQZ-20PC ATF22V10CQZ-20SC ATF22V10CQZ-20XC	28J 24P3 24S 24X	Commercial (0·C to 70·C)
20	14	4 12	ATF22V10CQZ-20JI ATF22V10CQZ-20PI ATF22V10CQZ-20SI ATF22V10CQZ-20XI	28J 24P3 24S 24X	Industrial (-40⋅C to +85⋅C)

Note: Shaded parts are being obsoleted and are not recommended for new designs. Customers should transition to ROHS offering

11.2 Atmel ATF22V10CQZ Green Package Options (Pb/Halide-free/RoHS Compliant)

t _{PD} (ns)	t _s (ns)	t _{co} (ns)	Ordering Code	Package	Operation Range
20	14	12	ATF22V10CQZ-20JU ATF22V10CQZ-20PU ATF22V10CQZ-20SU ATF22V10CQZ-20XU	28J 24P3 24S 24X	Industrial (-40⋅C to +85⋅C)

11.3 Using "C" Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the "I" to the "C" device (7ns "C" = 10ns "I") and de-rate power by 30%.

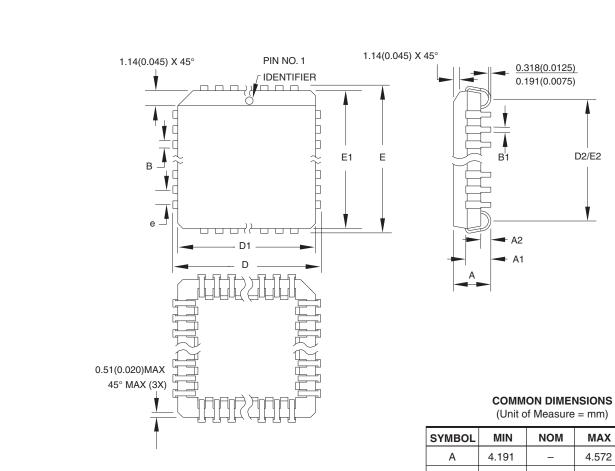
	Package Type					
28J	28-lead, Plastic J-leaded Chip Carrier (PLCC)					
24P3	24-pin, 0.300", Plastic Dual Inline Package (PDIP)					
24S	24-lead, 0.300" Wide, Plastic Gull-Wing Small Outline (SOIC)					
24X	24-lead, 4.4mm Wide, Plastic Thin Shrink Small Outline (TSSOP)					





12. **Packaging Information**

28J - PLCC 12.1



- Notes: 1. This package conforms to JEDEC reference MS-018, Variation AB.
 - 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 - 3. Lead coplanarity is 0.004" (0.102mm) maximum.

SYMBOL	MIN	NOM	MAX	NOTE
Α	4.191	_	4.572	
A1	2.286	_	3.048	
A2	0.508	_	_	
D	12.319	_	12.573	
D1	11.430	_	11.582	Note 2
Е	12.319	_	12.573	
E1	11.430	_	11.582	Note 2
D2/E2	9.906	_	10.922	
В	0.660	_	0.813	
B1	0.330	_	0.533	
е				

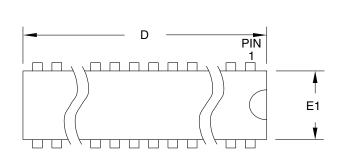
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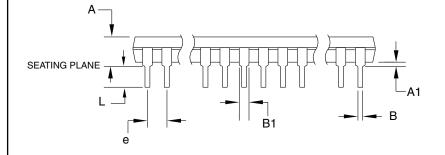
AMEL	Package Drawing Contact:
	Package Drawing Contact: packagedrawings@atmel.com

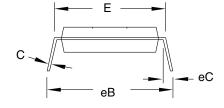
TITLE	DR
28J, 28-lead, Plastic J-leaded Chip Carrier (PLCC)	

DRAWING NO. REV. 28J В

12.2 24P3 - PDIP







Notes:

- . This package conforms to JEDEC reference MS-001, Variation AF.
- Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25mm (0.010").

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
Α	ı	-	5.334	
A1	0.381	-	_	
D	31.623	_	32.131	Note 2
Е	7.620	-	8.255	
E1	6.096	_	7.112	Note 2
В	0.356	-	0.559	
B1	1.270	_	1.651	
L	2.921	_	3.810	
С	0.203	_	0.356	
eB	_	-	10.922	
eC	0.000	_	1.524	
е		2.540 T	YP	

6/1/04

AIMEL	Package Drawing Contact:
	Package Drawing Contact: packagedrawings@atmel.com

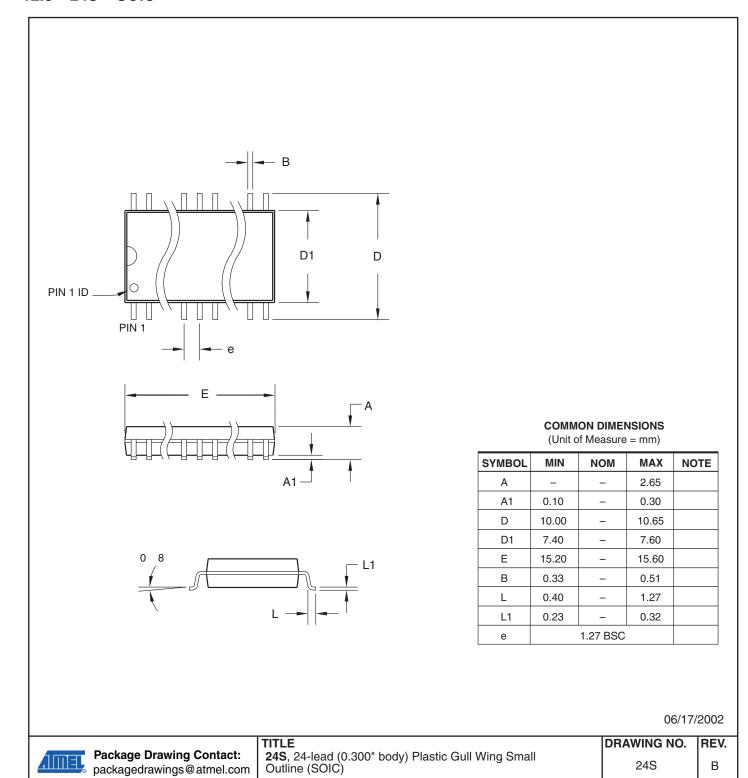
TITLE		_
	24-lead (0.300"/7.62mm Wide) Plastic Dua Package (PDIP)	al

DRAWING NO. REV. 24P3 D

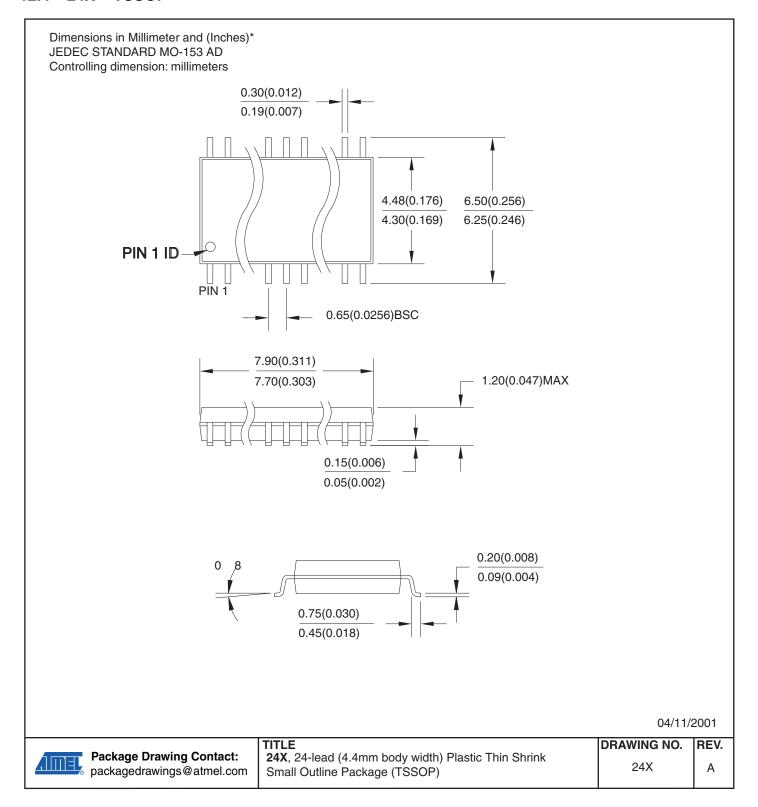




12.3 24S - SOIC



12.4 24X - TSSOP







13. Revision History

Doc. Rev.	Date	Comments
0778L	08/2010	Change t _S (ns) from 4.5 to 10 in Standard Package Options
0778K	07/2010	Remove Commercial Temperature Range For I _{SB} , change 25μA Max to 100μA max for commercial grade parts and 50μA Max to 120μA for Industrial grade parts Shade Standard Package Options and add note, "Shaded parts are not recommended for new designs. Customers should transition to ROHS offering" Remove Atmel ATF22V10CZ-15XC and Atmel ATF22V10CZ-15XI from Standard Package Options
0778J	11/2005	Add Green Package options



Headquarters

Atmel Corporation

2325 Orchard Parkway San Jose, CA 95131 USA

Tel: (+1)(408) 441-0311 Fax: (+1)(408) 487-2600

www.atmel.com

International

Atmel Asia Limited

Unit 01-5 & 16, 19/F BEA Tower, Millennium City 5 418 Kwun Tong Road Kwun Tong, Kowloon HONG KONG

Tel: (+852) 2245-6100 Fax: (+852) 2722-1369 **Atmel Munich GmbH**

Business Campus Parkring 4 D-85748 Garching b. Munich GERMANY

Tel: (+49) 89-31970-0 Fax: (+49) 89-3194621 Atmel Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 JAPAN

Tel: (+81) 3-3523-3551 Fax: (+81) 3-3523-7581

Product Contact

Technical Support

pld@atmel.com

Sales Contact

www.atmel.com/contacts

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