

IRLR3114ZPbF
IRLU3114ZPbF

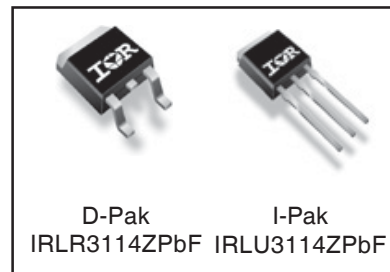
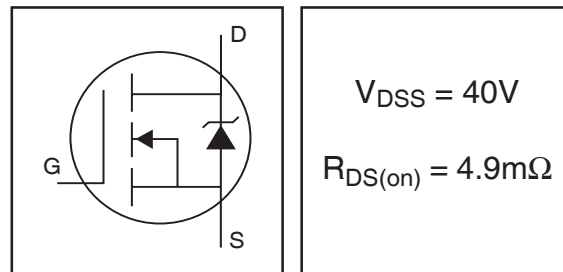
Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Logic Level

Description

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

HEXFET® Power MOSFET



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	130	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	89	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	42	
I_{DM}	Pulsed Drain Current ①	500	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	130	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ③	260	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Reflow Soldering Temperature, for 10 seconds	300	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ③	—	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) ②③	—	40	
$R_{\theta JA}$	Junction-to-Ambient ④	—	110	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.032	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.9	4.9	m Ω	$V_{GS} = 10V, I_D = 42A$ ③
		—	5.2	6.5		$V_{GS} = 4.5V, I_D = 42A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.5	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
gfs	Forward Transconductance	98	—	—	S	$V_{DS} = 10V, I_D = 42A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	40	56	nC	$I_D = 42A$
Q_{gs}	Gate-to-Source Charge	—	12	—		$V_{DS} = 20V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	18	—		$V_{GS} = 4.5V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	$V_{DD} = 20V$
t_r	Rise Time	—	140	—		$I_D = 42A$
$t_{d(off)}$	Turn-Off Delay Time	—	33	—		$R_G = 3.7\Omega$
t_f	Fall Time	—	50	—		$V_{GS} = 4.5V$ ③
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3810	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	650	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	350	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	2390	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	580	—		$V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz$
$C_{oss\ eff.}$	Effective Output Capacitance	—	820	—		$V_{GS} = 0V, V_{DS} = 0V\ to\ 32V$ ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	130	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	500		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 42A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	30	45	ns	$T_J = 25^\circ\text{C}, I_F = 42A, V_{DD} = 20V$
Q_{rr}	Reverse Recovery Charge	—	27	41	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

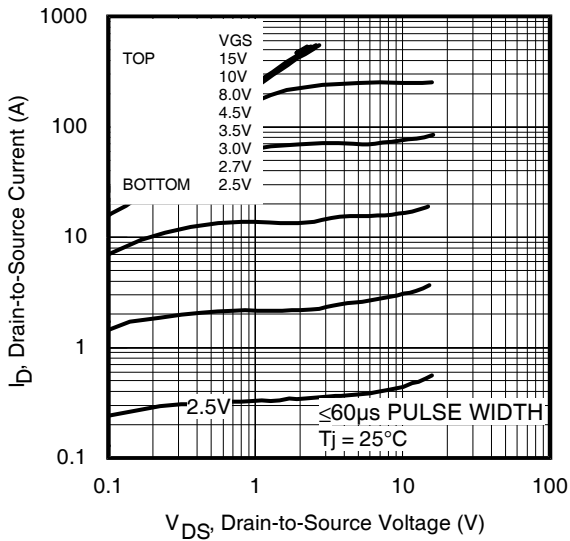


Fig 1. Typical Output Characteristics

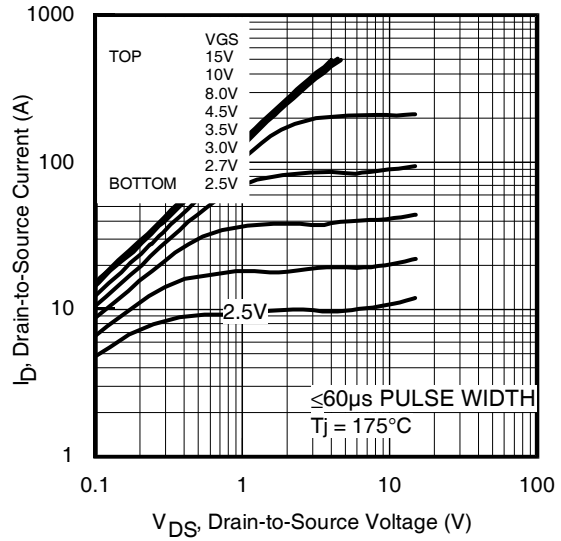


Fig 2. Typical Output Characteristics

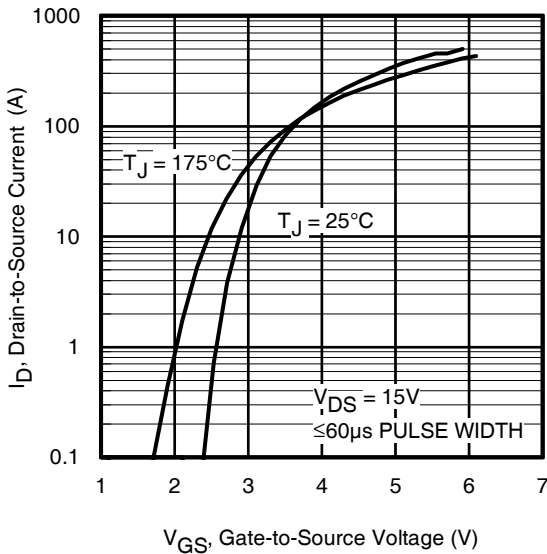


Fig 3. Typical Transfer Characteristics

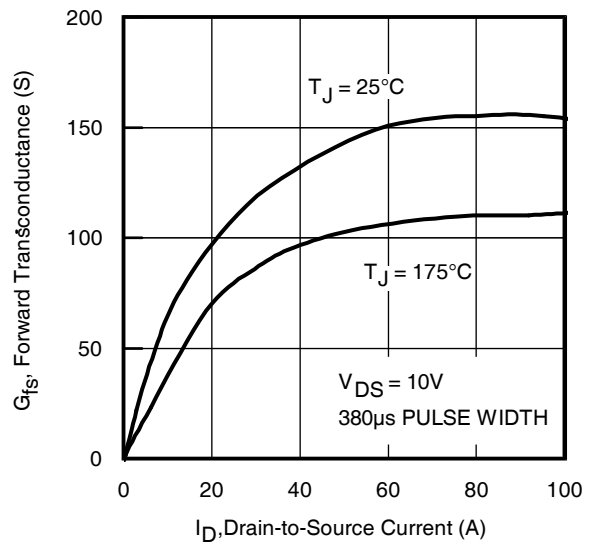


Fig 4. Typical Forward Transconductance vs. Drain Current

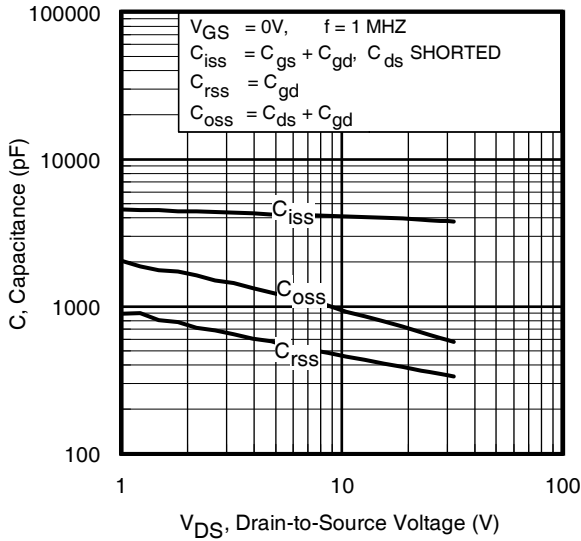


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

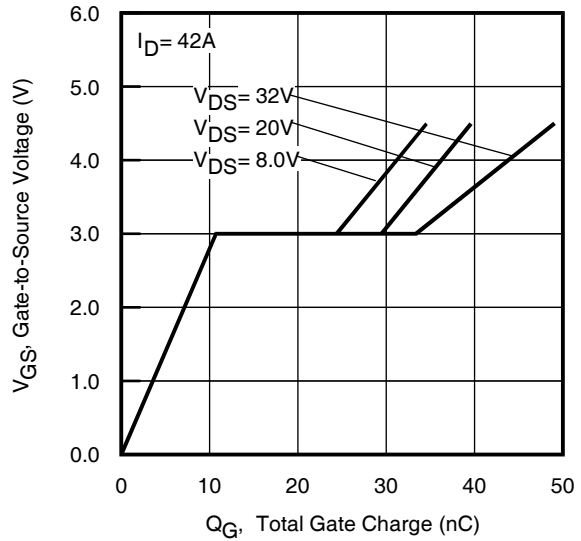


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

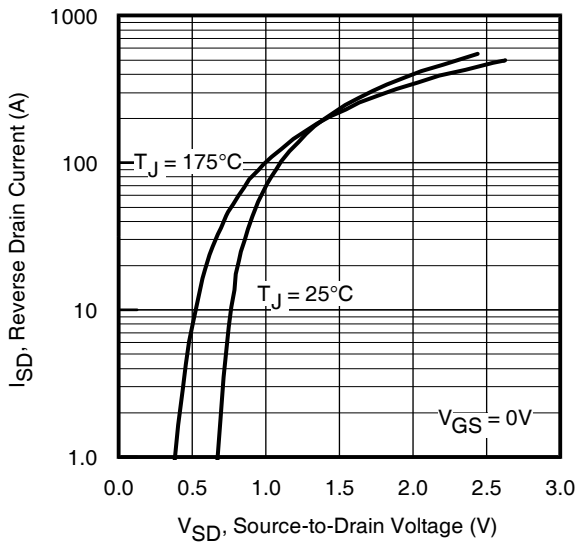


Fig 7. Typical Source-Drain Diode Forward Voltage

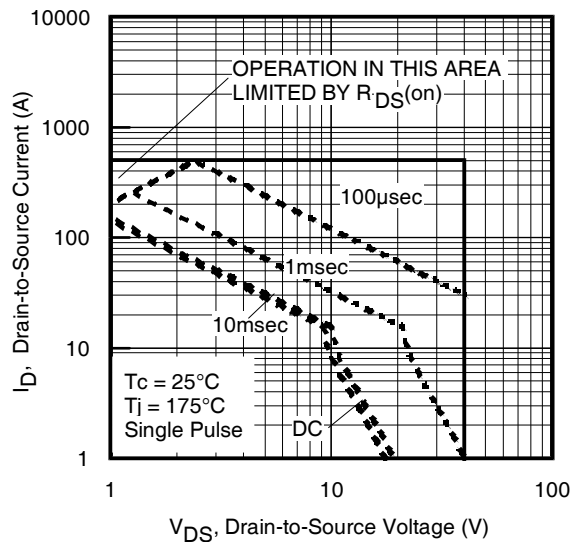


Fig 8. Maximum Safe Operating Area

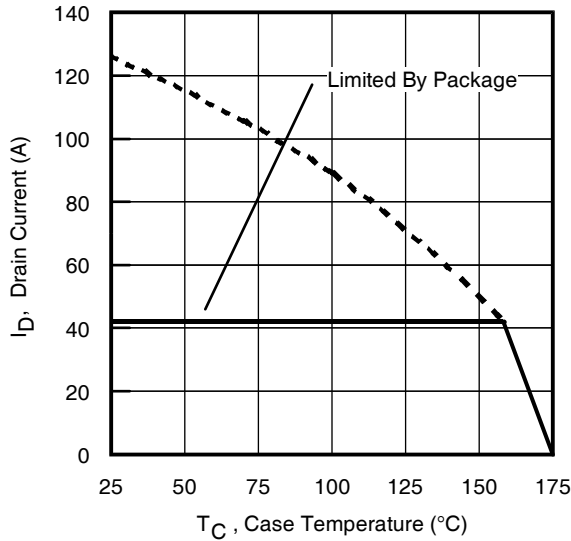


Fig 9. Maximum Drain Current vs. Case Temperature

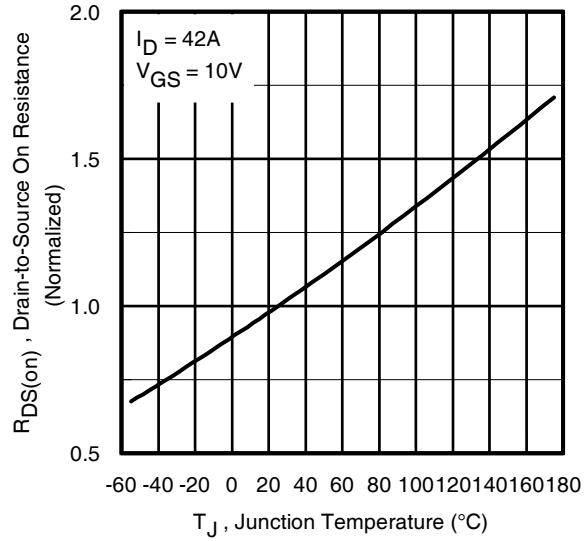


Fig 10. Normalized On-Resistance vs. Temperature

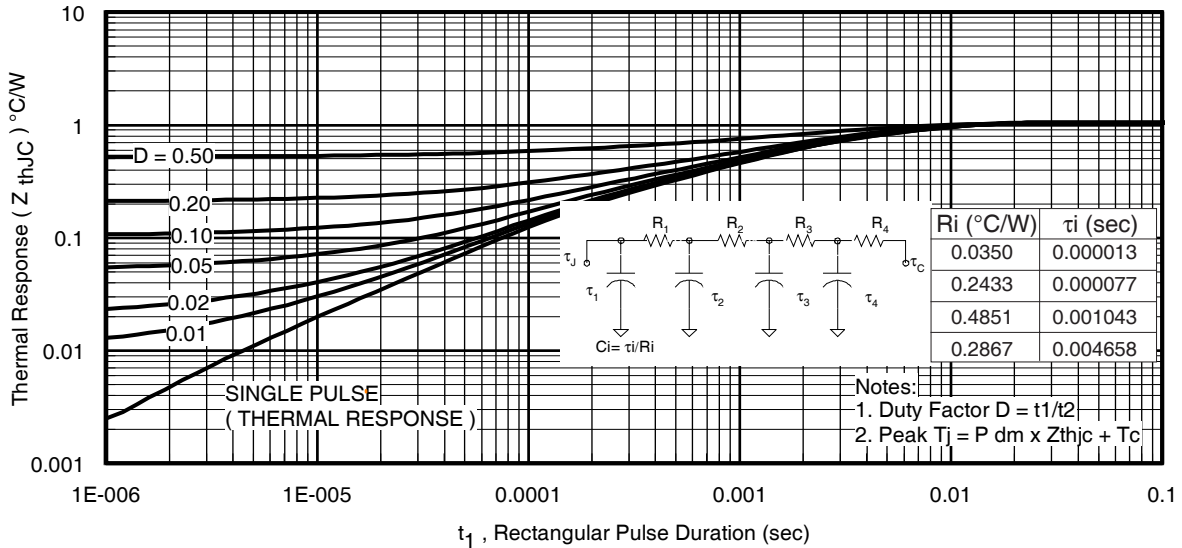


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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International
IR Rectifier



Fig 12a. Unclamped Inductive Test Circuit



Fig 12b. Unclamped Inductive Waveforms



Fig 13a. Basic Gate Charge Waveform



Fig 13b. Gate Charge Test Circuit

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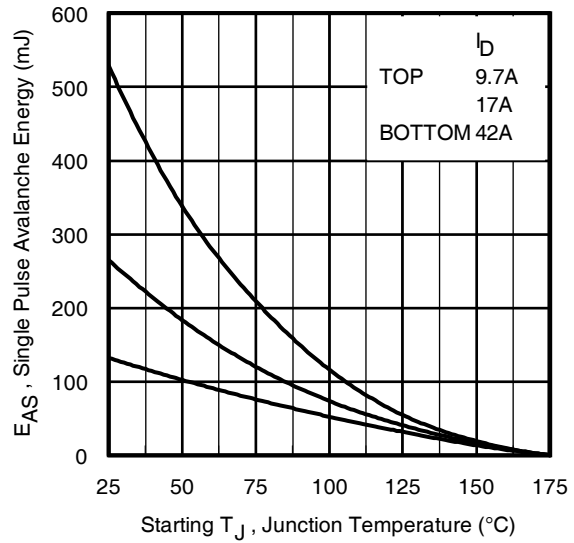


Fig 12c. Maximum Avalanche Energy vs. Drain Current

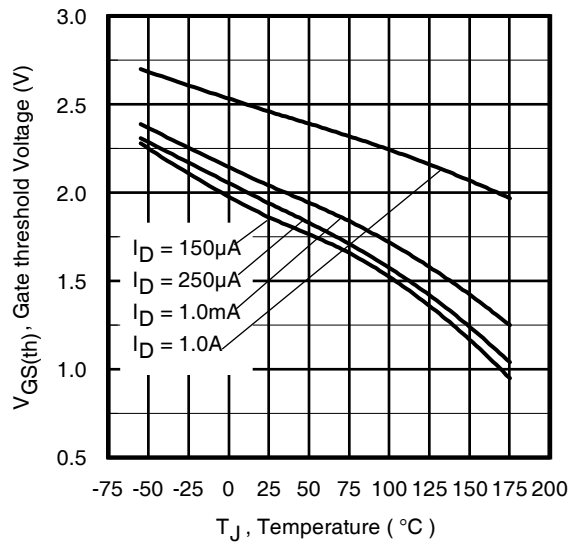


Fig 14. Threshold Voltage vs. Temperature

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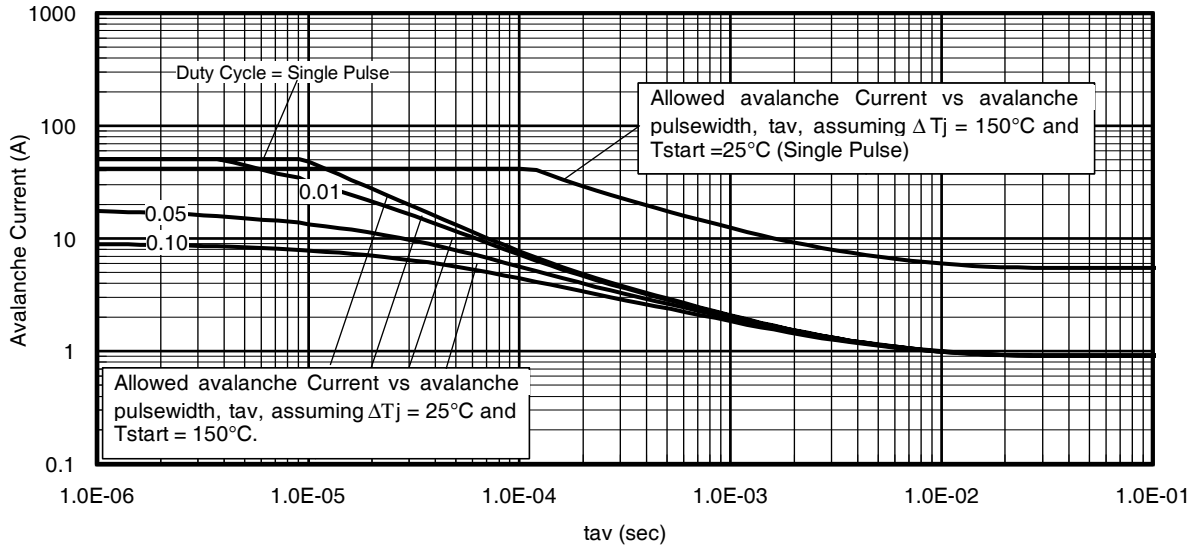


Fig 15. Typical Avalanche Current vs.Pulsewidth

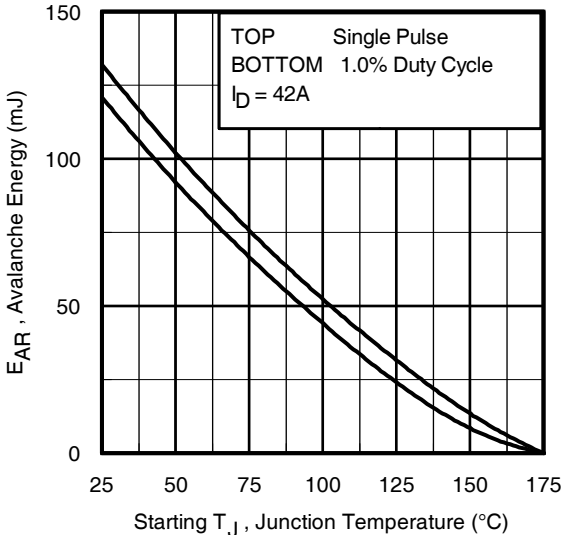


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as neither T_{jmax} nor I_{av} (max) is exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



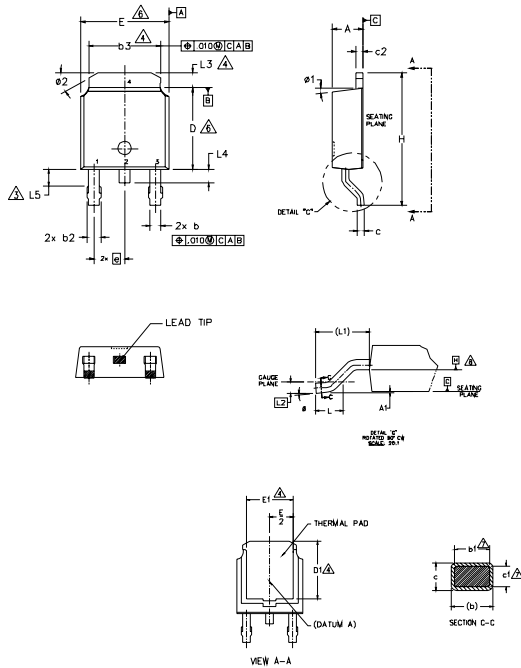
Fig 18a. Switching Time Test Circuit



Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
 - 3.- LEAD DIMENSION UNCONTROLLED IN L5.
 - 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
 - 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
 - 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 - 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
 - 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
 - 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
ø	0"	10"	0"	10"	
ø1	0"	15"	0"	15"	
ø2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

- HEXFET
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
 - 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE "A"

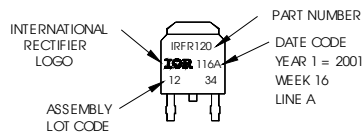
Note: "P" in assembly line position
indicates "Lead-Free"

"P" in assembly line position indicates
"Lead-Free" qualification to the consumer-level

OR

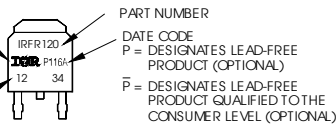
INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE



PART NUMBER

DATE CODE
YEAR 1 = 2001
WEEK 16
LINE A



PART NUMBER

DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)

P = DESIGNATES LEAD-FREE
PRODUCT QUALIFIED TO THE
CONSUMER LEVEL (OPTIONAL)

YEAR 1 = 2001
WEEK 16
A = ASSEMBLY SITE CODE

Notes:

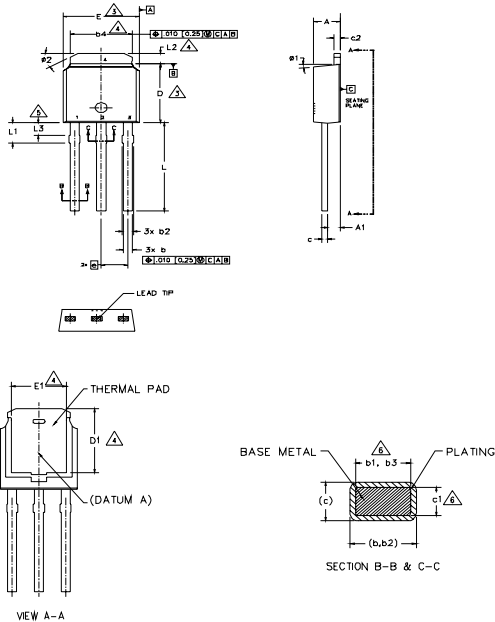
1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/automotive/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

IRLR/U3114ZPbF



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 - 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
 - 3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 - 4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
 - 5.- LEAD DIMENSION UNCONTROLLED IN L3.
 - 6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
 - 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
 - 8.- CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	1.14	1.52	.045	.060	5
ø1	0"	15"	0"	15"	
ø2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

HEXFET

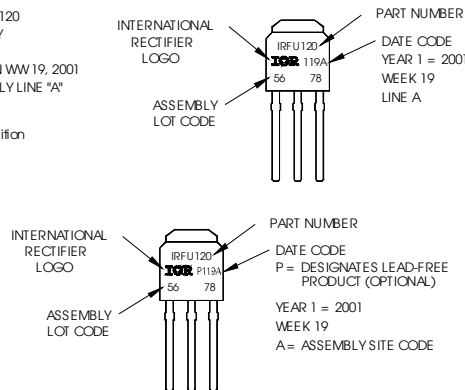
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW19, 2001 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates Lead-Free

OR

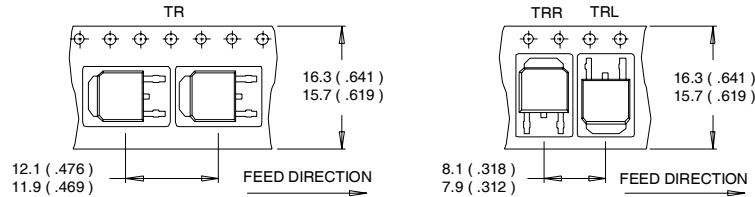


Notes:

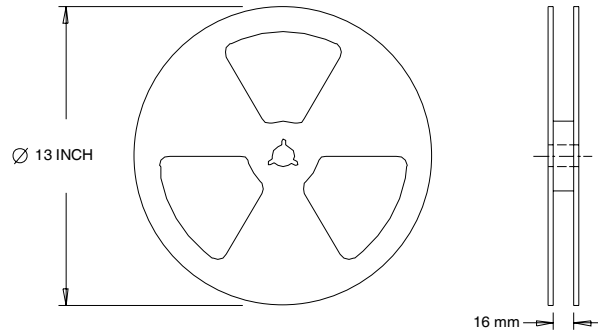
1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.15\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 42\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material).
- ⑧ R_θ is measured at T_J approximately 90°C .

Data and specifications subject to change without notice.
 This product has been designed for the Industrial market.
 Qualification Standards can be found on IR's Web site.