

IR2108(4) (S) & (PbF)

Features

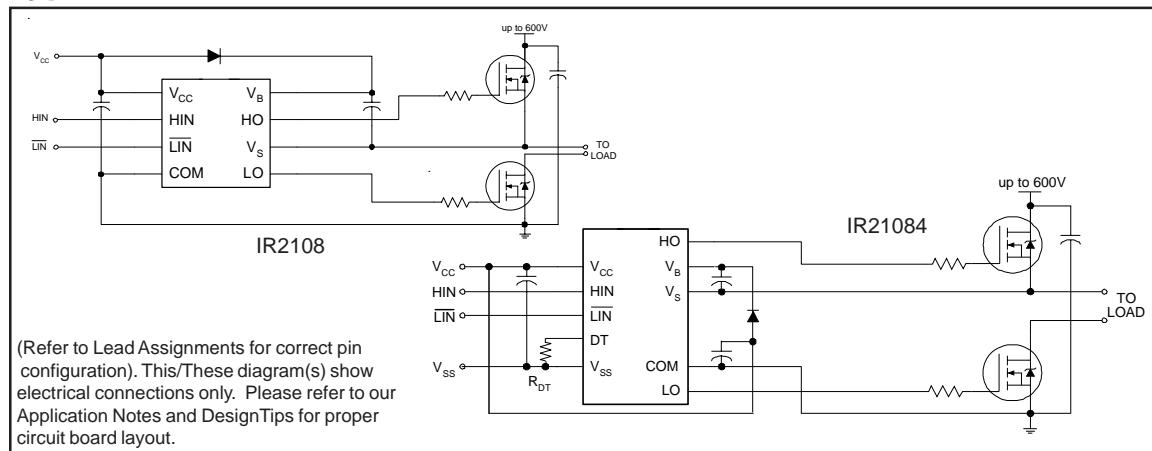
- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with HIN input
- Low side output out of phase with LIN input
- Logic and power ground +/- 5V offset.
- Internal 540ns dead-time, and programmable up to 5us with one external R_{DT} resistor (IR21084)
- Lower di/dt gate driver for better noise immunity
- Available in Lead-Free

Description

The IR2108(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune

CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating absolute voltage	-0.3	625	V
V_S	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	$V_{CC} + 0.3$	
DT	Programmable dead-time pin voltage (IR21084 only)	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage (HIN & LIN)	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
V_{SS}	Logic ground (IR21084 only)	$V_{CC} - 25$	$V_{CC} + 0.3$	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	(8 lead PDIP)	—	1.0
		(8 lead SOIC)	—	0.625
		(14 lead PDIP)	—	1.6
		(14 lead SOIC)	—	1.0
R_{thJA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125
		(8 lead SOIC)	—	200
		(14 lead PDIP)	—	75
		(14 lead SOIC)	—	120
T_J	Junction temperature	—	150	$^\circ\text{C}$
T_S	Storage temperature	-50	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	IR2108	COM	
		IR21084	V_{SS}	
DT	Programmable dead-time pin voltage (IR21084 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21084 only)	-5	5	$^\circ\text{C}$
T_A	Ambient temperature	-40	125	

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = V_{SS} unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	220	300	nsec	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	200	280		$V_S = 0V$ or 600V
MT	Delay matching $ t_{on} - t_{off} $	—	0	30		
t_r	Turn-on rise time	—	150	220		$V_S = 0V$
t_f	Turn-off fall time	—	50	80		$V_S = 0V$
DT	Deadtime: LO turn-off to HO turn-on(DTLO-HO) & HO turn-off to LO turn-on (DTHO-LO)	400	540	680		RDT= 0
MDT	Deadtime matching = $ DT_{LO-HO} - DT_{HO-LO} $	4	5	6	usec	RDT = 200K (IR21084)
		—	0	60		RDT=0
MDT	Deadtime matching = $ DT_{LO-HO} - DT_{HO-LO} $	—	0	600	nsec	RDT = 200K (IR21084)

Static Electrical Characteristics

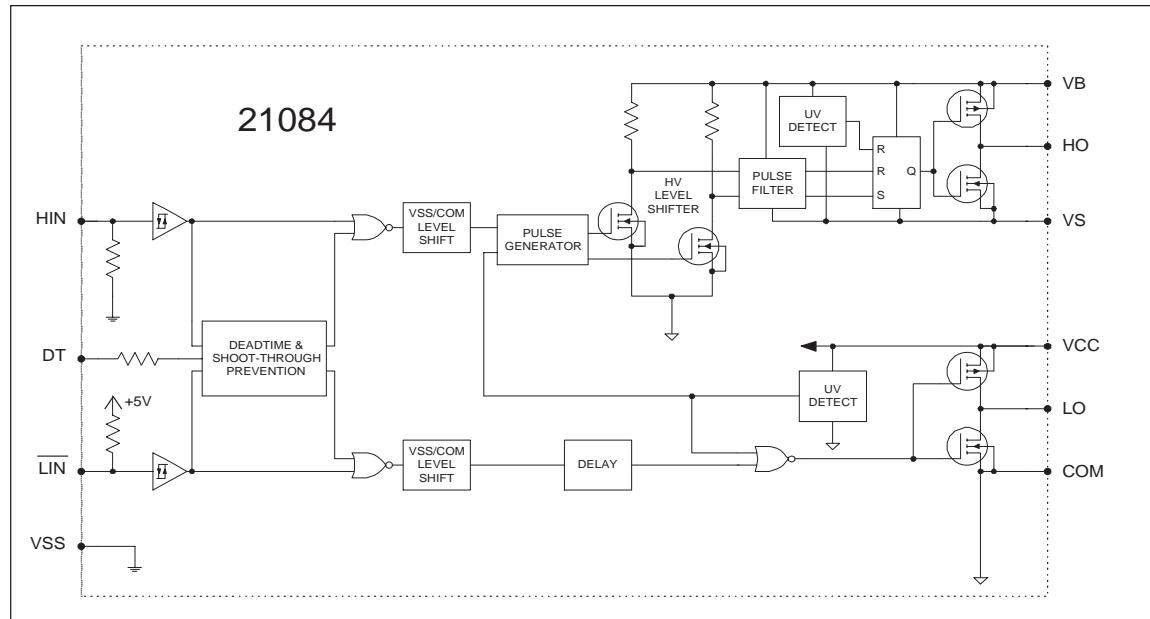
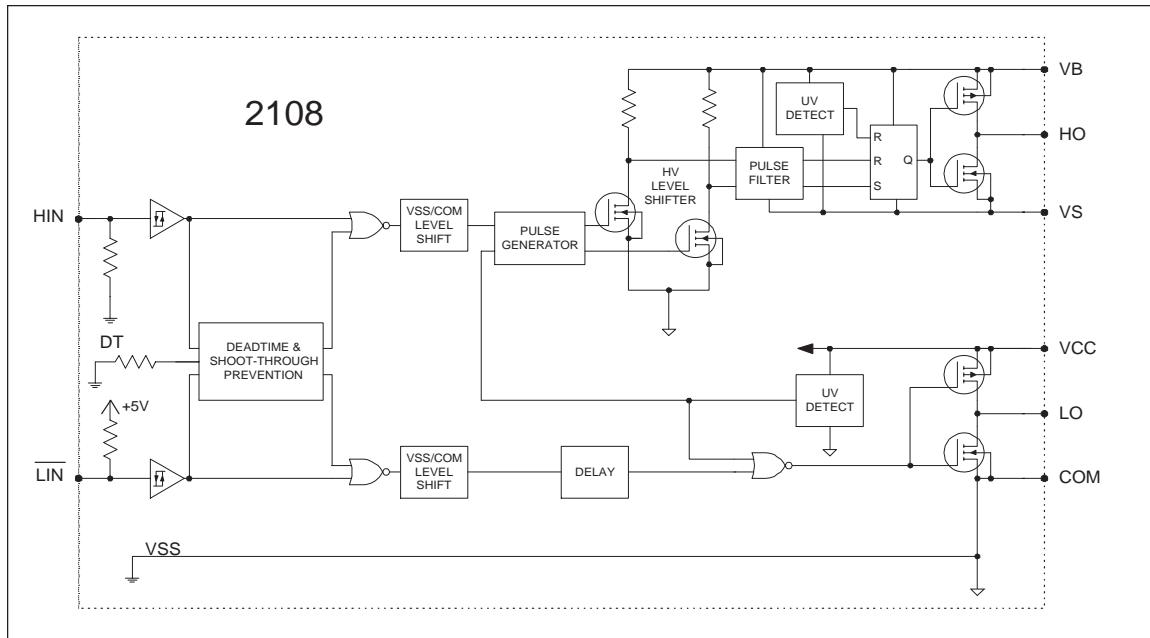
V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: HIN and LIN. The V_O , I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HIN & logic "0" for \overline{LIN}	2.9	—	—	V	$V_{CC} = 10V$ to 20V
V_{IL}	Logic "0" input voltage for HIN & logic "1" for \overline{LIN}	—	—	0.8		$V_{CC} = 10V$ to 20V
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20$ mA
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		$I_O = 20$ mA
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	20	75	130		$V_{IN} = 0V$ or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	$V_{IN} = 0V$ or 5V RDT=0
I_{IN+}	Logic "1" input bias current	—	5	20	μA	$HIN = 5V$, $\overline{LIN} = 0V$
I_{IN-}	Logic "0" input bias current	—	—	2		$HIN = 0V$, $\overline{LIN} = 5V$
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V$, $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	250	350	—		$V_O = 15V$, $PW \leq 10 \mu s$

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Functional Block Diagram



Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (referenced to COM for IR2108 and VSS for IR21084)
LIN	Logic input for low side gate driver output (LO), out of phase (referenced to COM for IR2108 and VSS for IR21084)
DT	Programmable dead-time lead, referenced to VSS. (IR21084 only)
VSS	Logic Ground (21084 only)
V _B	High side floating supply
HO	High side gate driver output
V _S	High side floating supply return
V _{CC}	Low side and logic fixed supply
LO	Low side gate driver output
COM	Low side return

Lead Assignments

 8 Lead PDIP	 8 Lead SOIC
IR2108	IR2108S

 14 Lead PDIP	 14 Lead SOIC
IR21084	IR21084S

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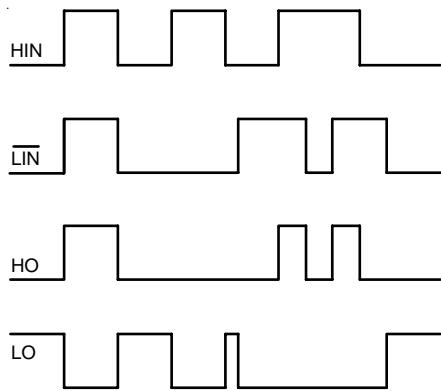


Figure 1. Input/Output Timing Diagram

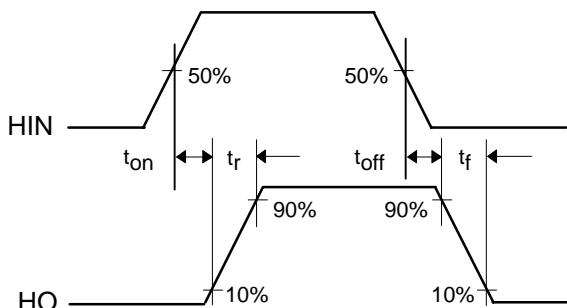
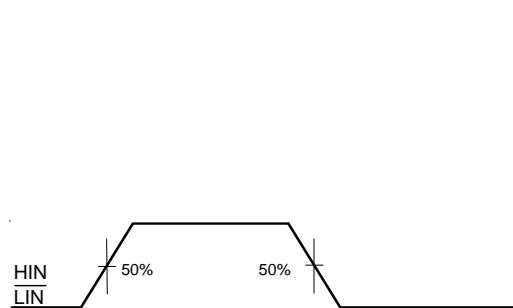
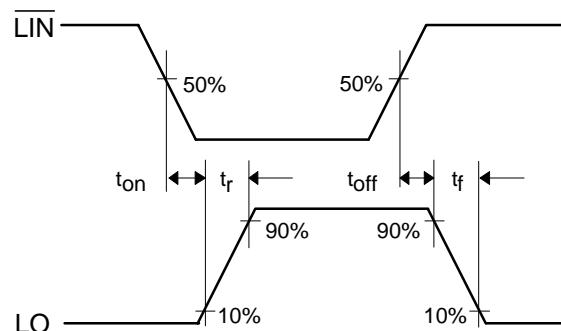


Figure 3. Deadtime Waveform Definitions

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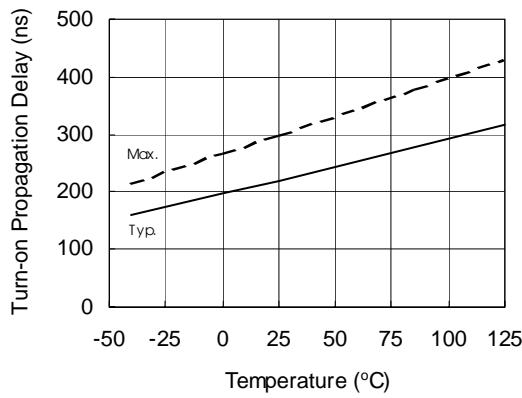


Figure 4A. Turn-on Propagation Delay vs. Temperature

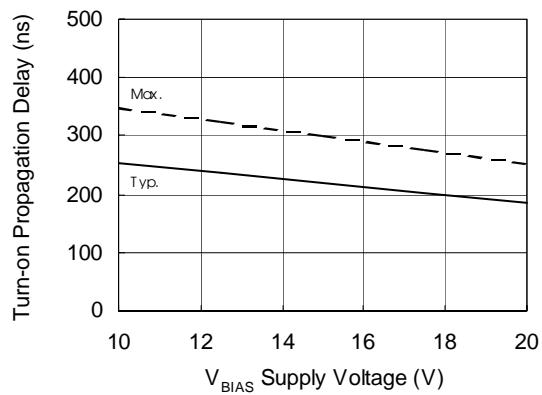


Figure 4B. Turn-on Propagation Delay vs. Supply Voltage

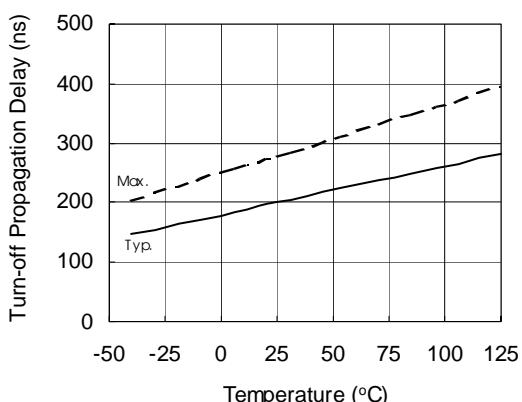


Figure 5A. Turn-off Propagation Delay vs. Temperature

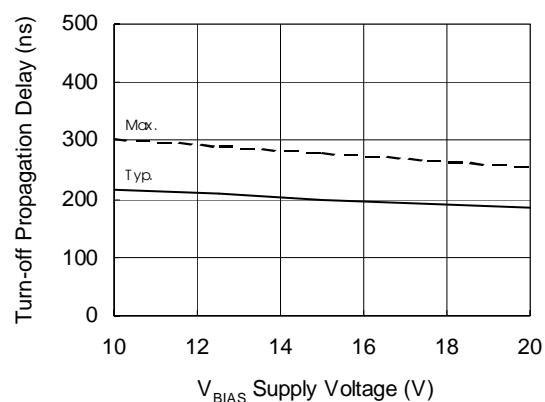


Figure 5B. Turn-off Propagation Delay vs. Supply Voltage

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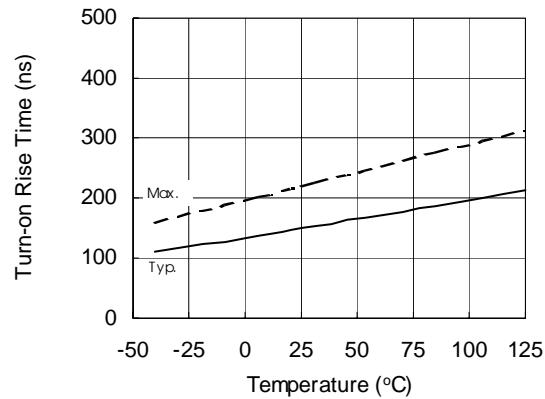


Figure 6A. Turn-on Rise Time
vs. Temperature

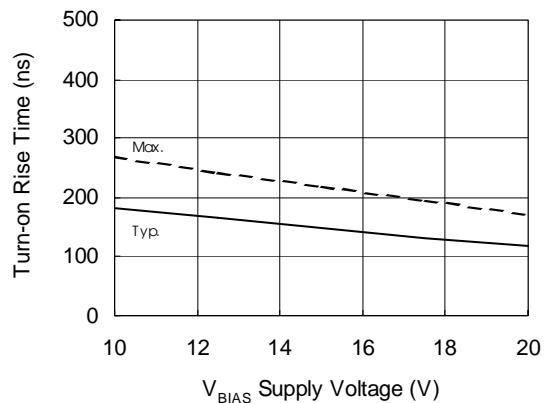


Figure 6B. Turn-on Rise Time
vs. Supply Voltage

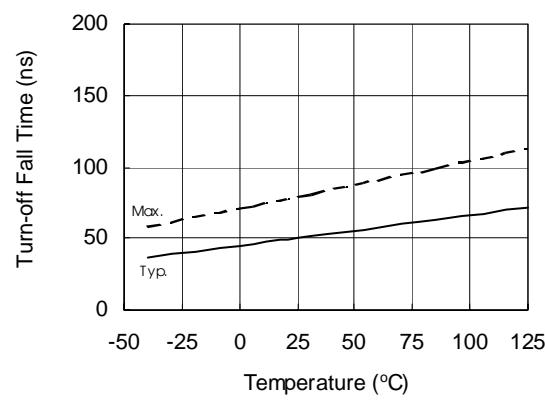


Figure 7A. Turn-off Fall Time
vs. Temperature

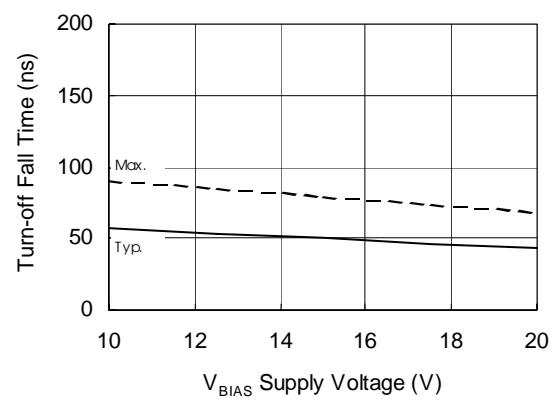


Figure 7B. Turn-off Fall Time
vs. Supply Voltage

IR2108(4) (S) & (PbF)

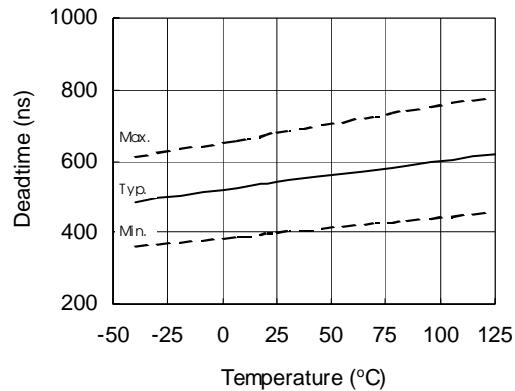


Figure 8A. Deadtime vs. Temperature

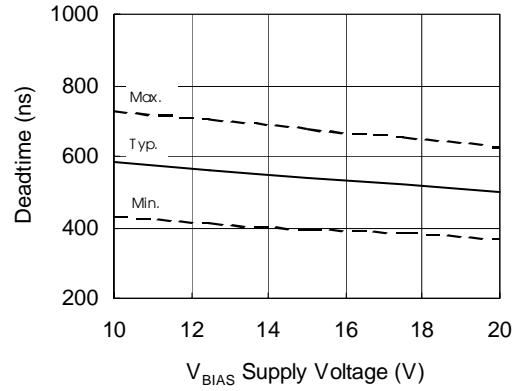


Figure 8B. Deadtime vs. Supply Voltage

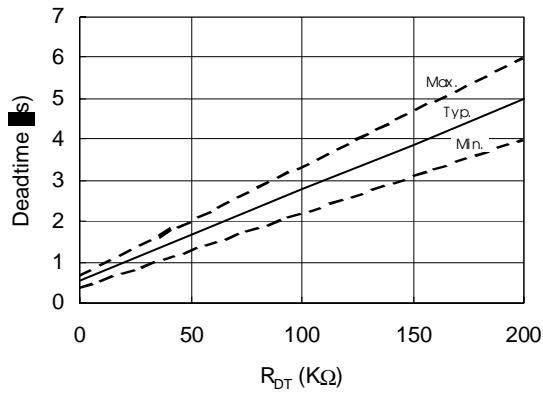


Figure 8C. Deadtime vs. R_{DT}
(IR21084 Only)

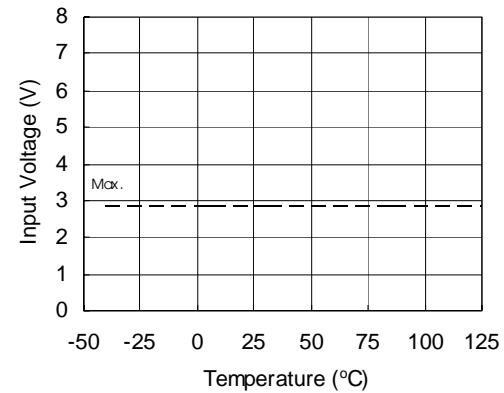


Figure 9A. Logic "1" Input Voltage
vs. Temperature

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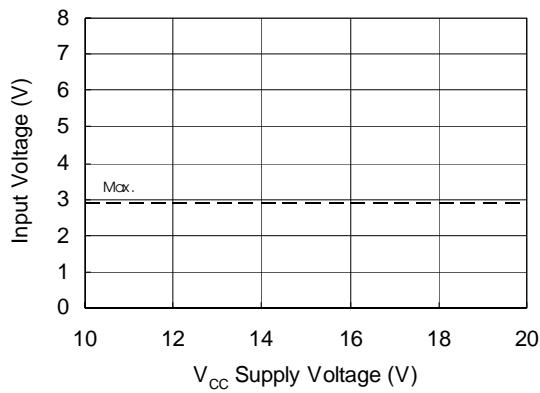


Figure 9B. Logic "1" Input Voltage vs. Supply Voltage

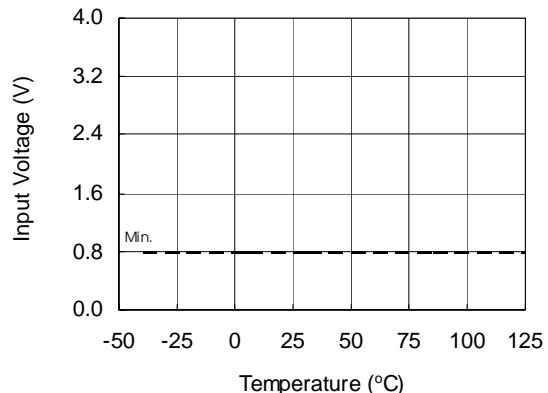


Figure 10A. Logic "0" Input Voltage vs. Temperature

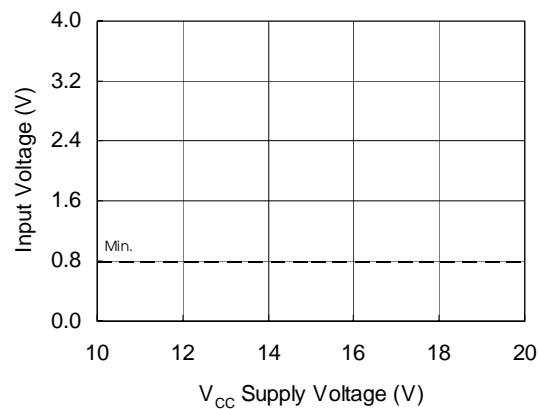


Figure 10B. Logic "0" Input Voltage vs. Supply Voltage

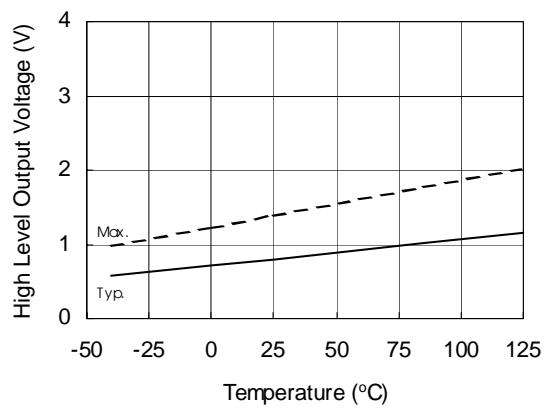


Figure 11A. High Level Output vs. Temperature

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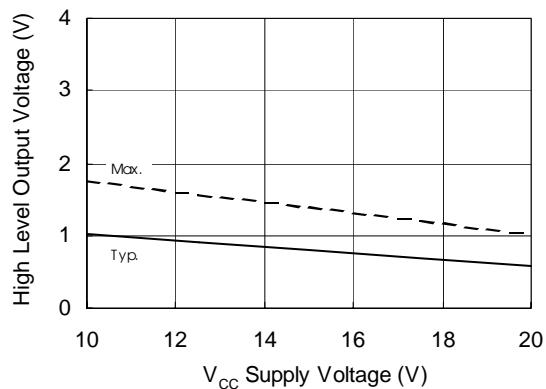


Figure 11B. High Level Output
vs. Supply Voltage

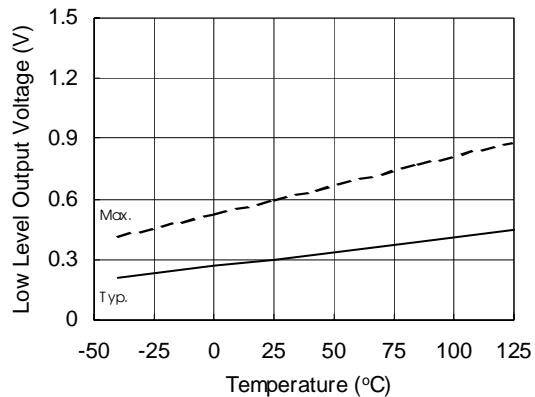


Figure 12A. Low Level Output
vs. Temperature

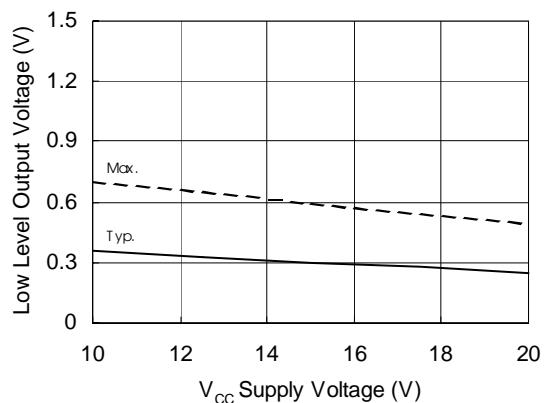


Figure 12B. Low Level Output
vs. Supply Voltage

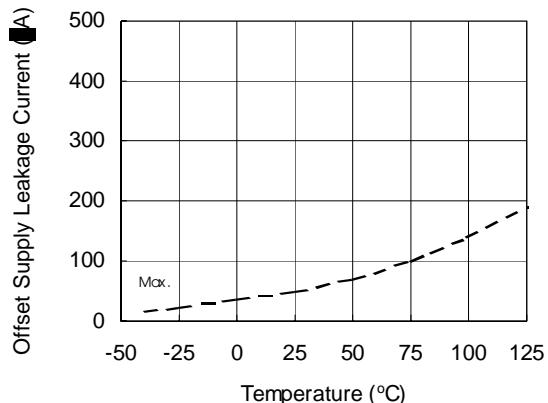


Figure 13A. Offset Supply Leakage Current
vs. Temperature

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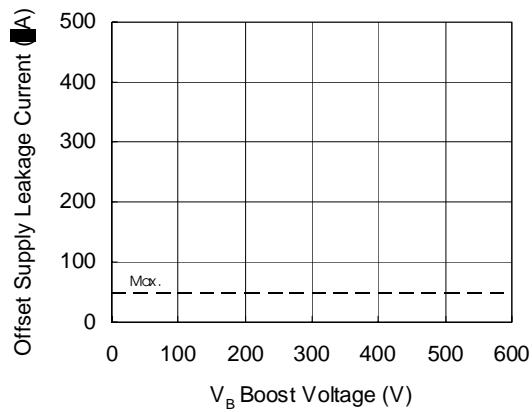


Figure 13B. Offset Supply Leakage Current
vs. Temperature

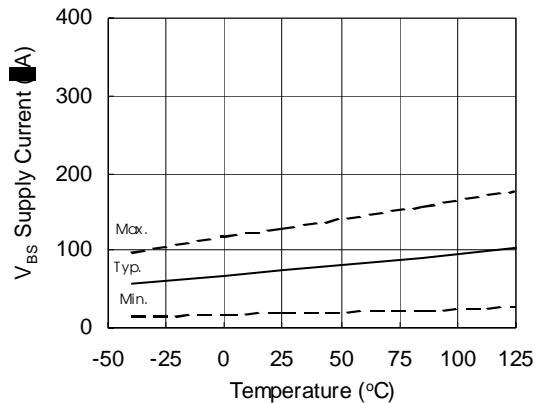


Figure 14A. V_{BS} Supply Current
vs. Temperature

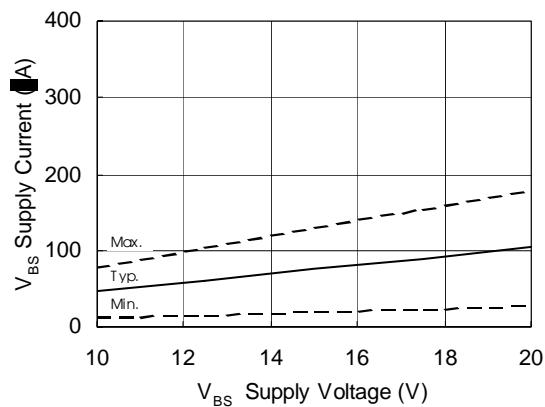


Figure 14B. V_{BS} Supply Current
vs. Supply Voltage

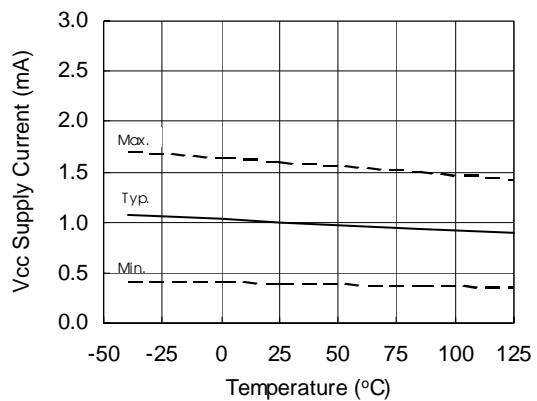


Figure 15A. V_{CC} Supply Current
vs. Temperature

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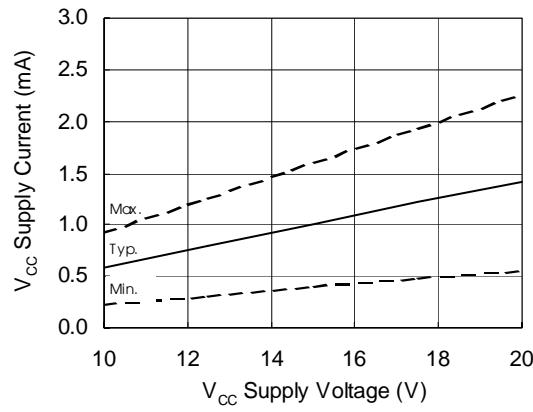


Figure 15B. V_{CC} Supply Current
vs. Supply Voltage

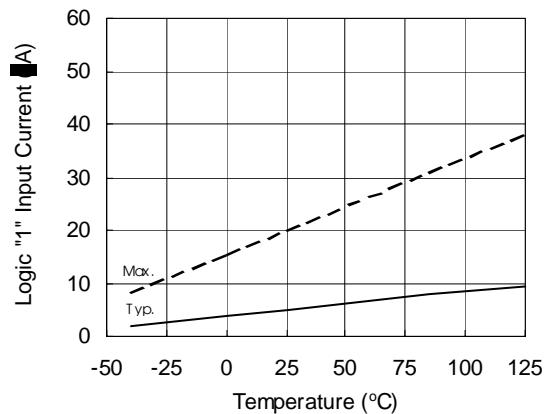


Figure 16A. Logic "1" Input Current
vs. Temperature

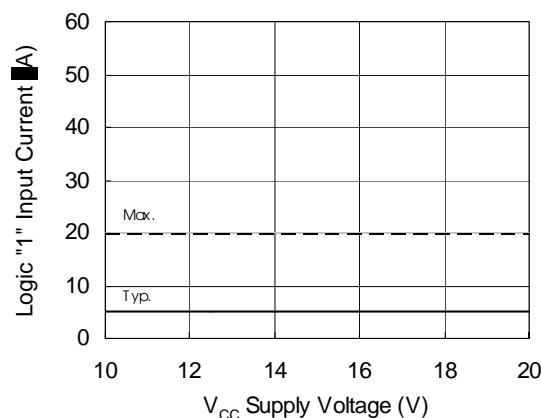


Figure 16B. Logic "1" Input Current
vs. Supply Voltage

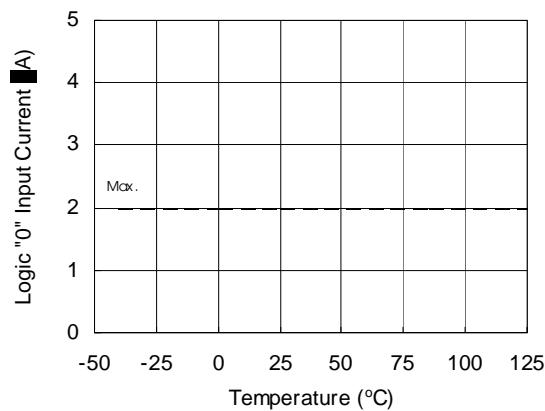


Figure 17A. Logic "0" Input Current
vs. Temperature

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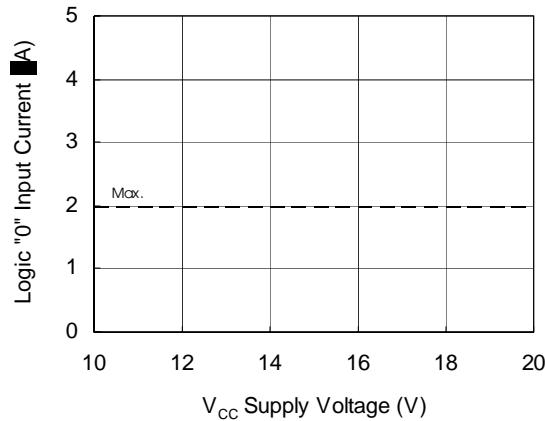


Figure 17B. Logic "0" Input Current vs. Supply Voltage

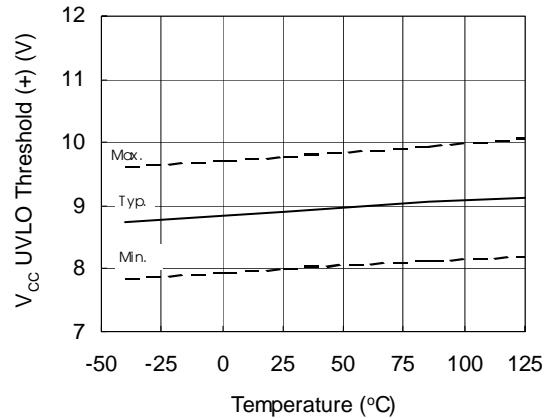


Figure 18. V_{CC} Undervoltage Threshold (+) vs. Temperature

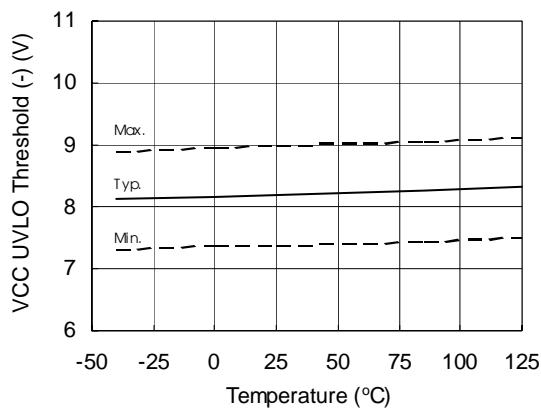


Figure 19. V_{CC} Undervoltage Threshold (-) vs. Temperature

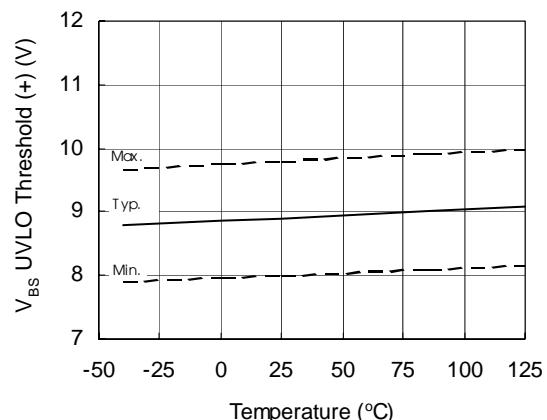


Figure 20. V_{BS} Undervoltage Threshold (+) vs. Temperature

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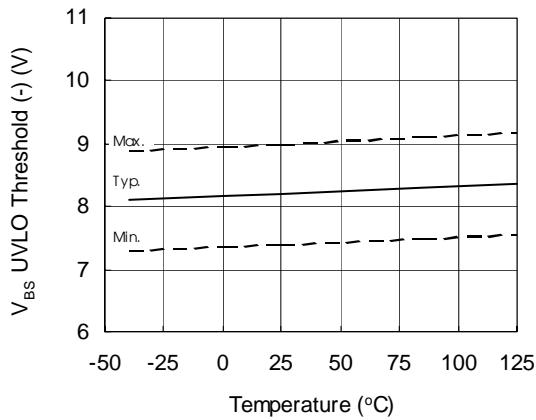


Figure 21. V_{BS} Undervoltage Threshold (-) vs. Temperature

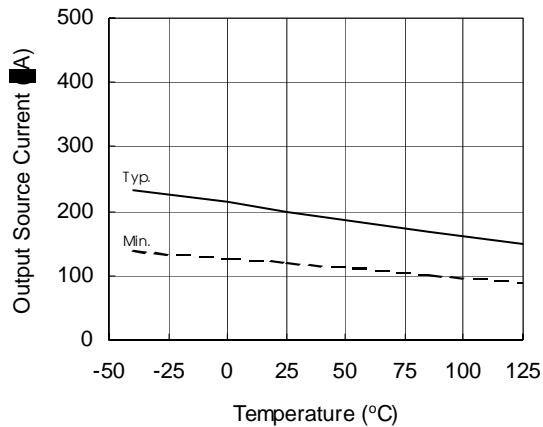


Figure 22A. Output Source Current vs. Temperature

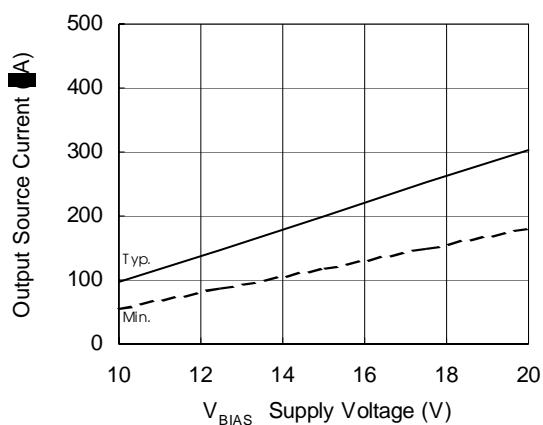


Figure 22B. Output Source Current vs. Supply Voltage

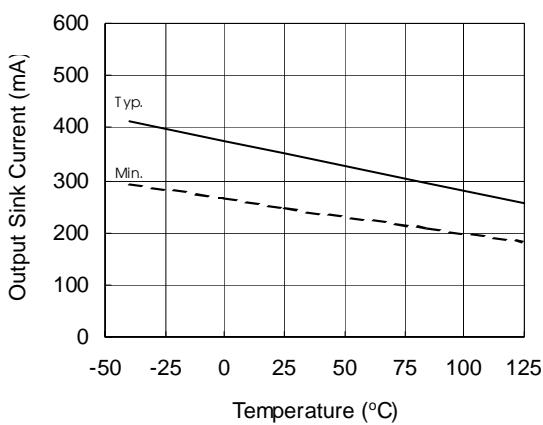


Figure 23A. Output Sink Current vs. Temperature

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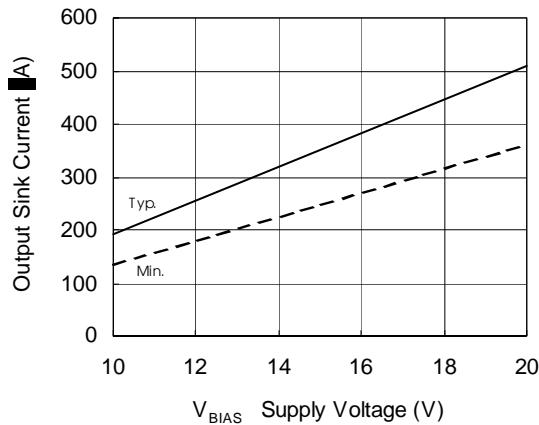


Figure 23B. Output Sink Current
vs. Supply Voltage

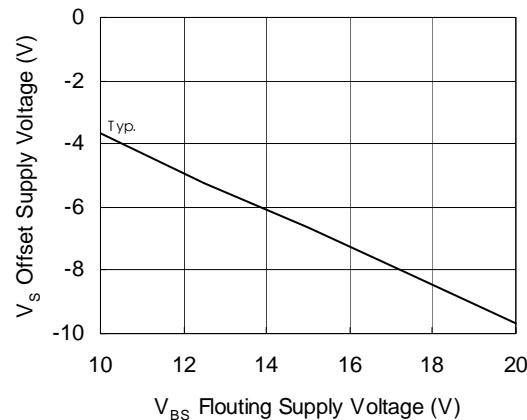


Figure 24. Maximum V_s Negative Offset
vs. Supply Voltage

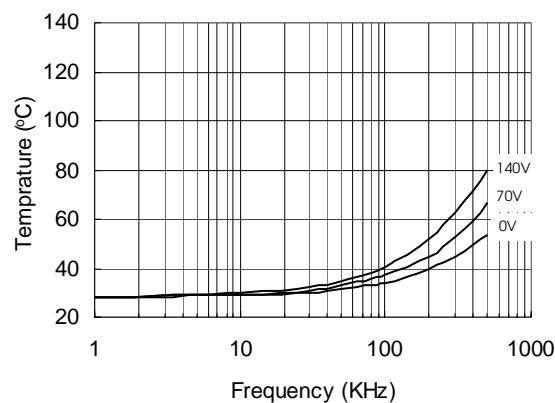


Figure 25. IR2108 vs. Frequency (IRFBC20),
R_{gate}=33Ω, V_{CC}=15V

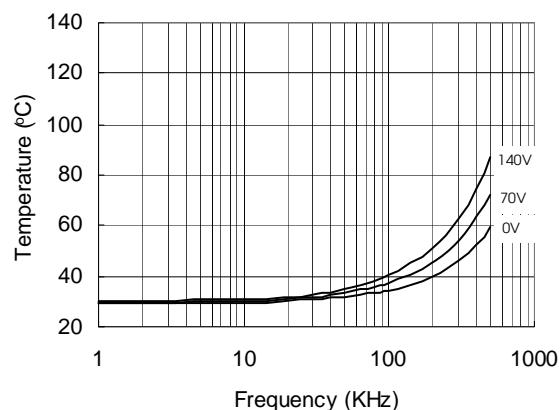


Figure 26. IR2108 vs. Frequency (IRFBC30),
R_{gate}=22Ω, V_{CC}=15V

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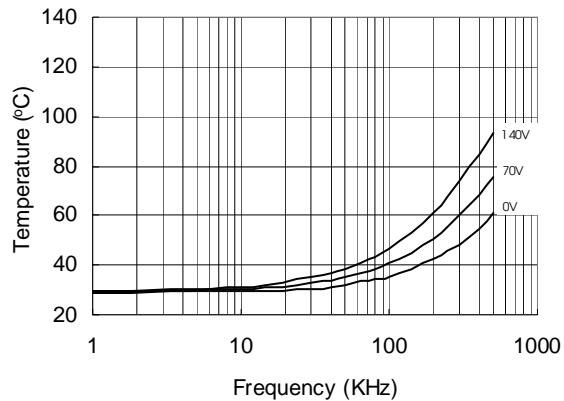


Figure 27. IR2108 vs. Frequency (IRFBC40),
 $R_{\text{gate}}=15\Omega$, $V_{\text{cc}}=15\text{V}$

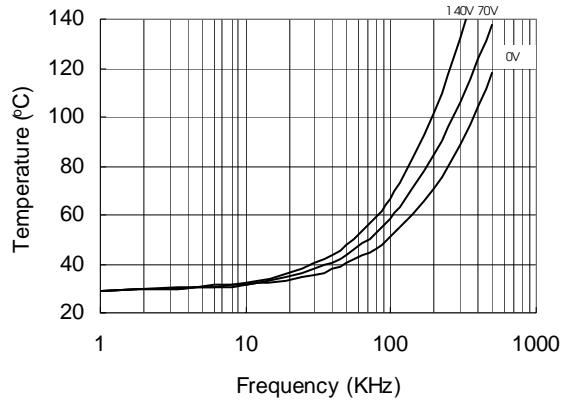


Figure 28. IR2108 vs. Frequency (IRFPE50),
 $R_{\text{gate}}=10\Omega$, $V_{\text{cc}}=15\text{V}$

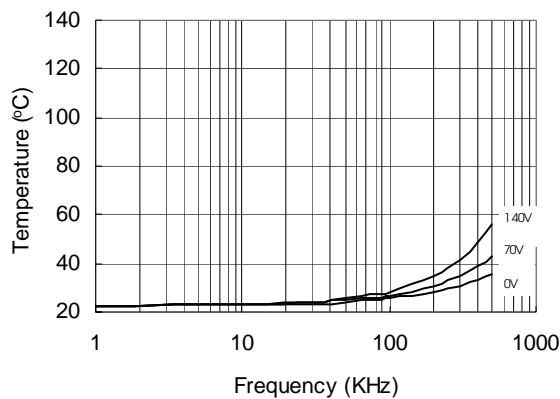


Figure 29. IR21084 vs. Frequency (IRFBC20),
 $R_{\text{gate}}=33\Omega$, $V_{\text{cc}}=15\text{V}$

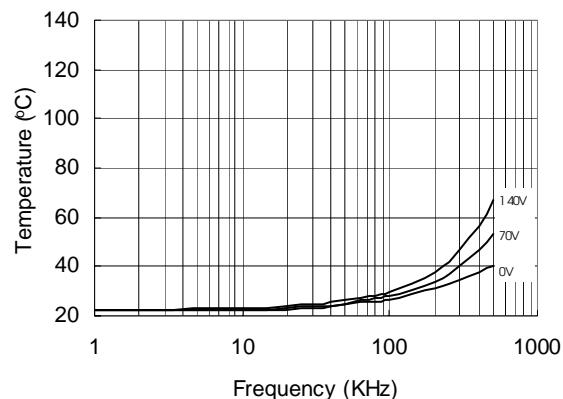


Figure 30. IR21084 vs. Frequency (IRFBC30),
 $R_{\text{gate}}=22\Omega$, $V_{\text{cc}}=15\text{V}$

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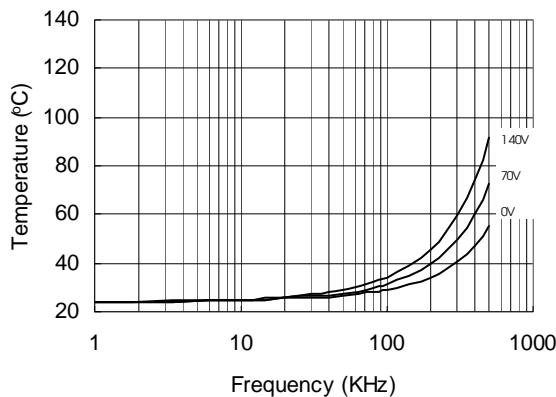


Figure 31. IR21084 vs. Frequency (IRFBC40),
 $R_{gate}=15\Omega$, $V_{CC}=15V$

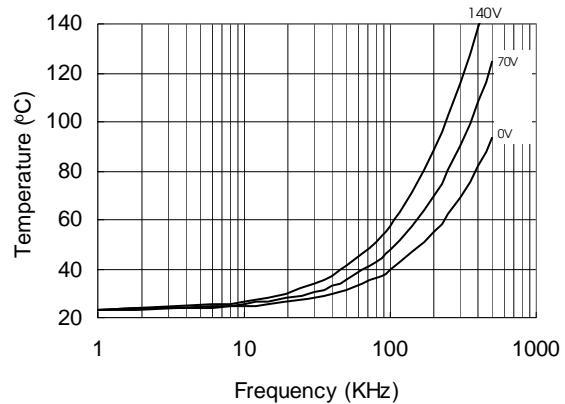


Figure 32. IR21084 vs. Frequency (IRFPE50),
 $R_{gate}=10\Omega$, $V_{CC}=15V$

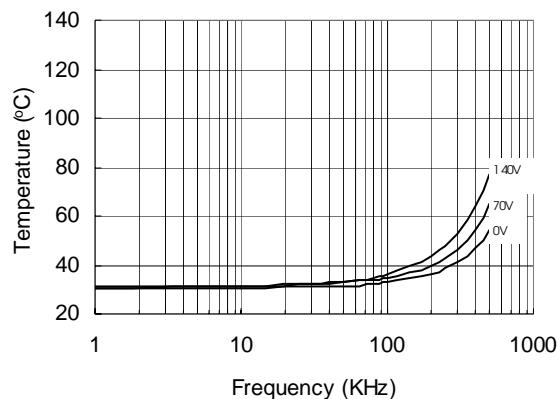


Figure 33. IR2108S vs. Frequency (IRFBC20),
 $R_{gate}=33\Omega$, $V_{CC}=15V$

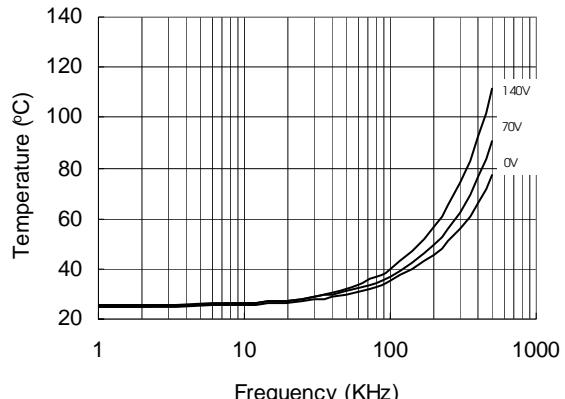
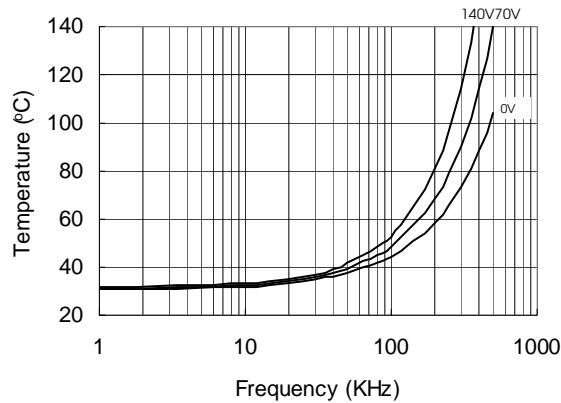
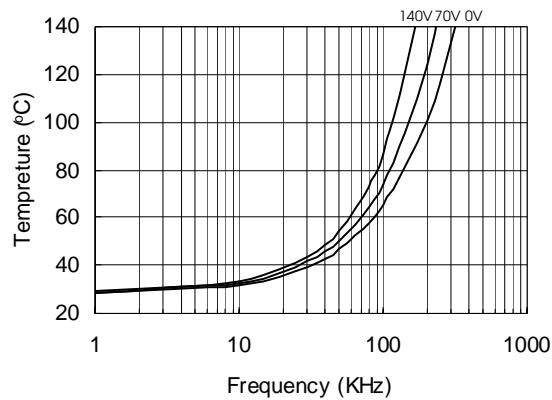


Figure 34. IR2108S vs. Frequency (IRFBC30),
 $R_{gate}=22\Omega$, $V_{CC}=15V$

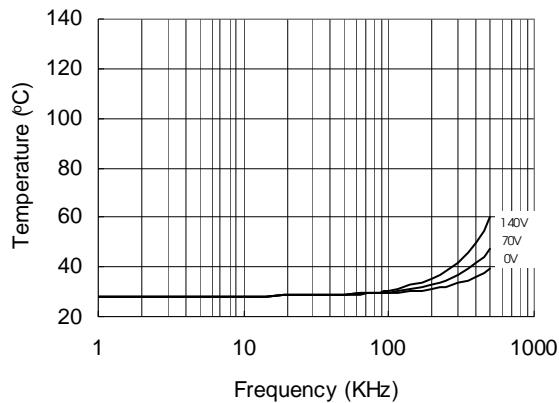
IR2108(4) (S) & (PbF)



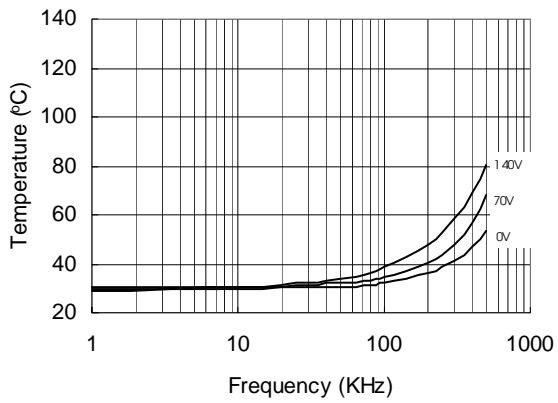
**Figure 35. IR2108S vs. Frequency (IRFBC40),
 $R_{gate}=15\Omega$, $V_{cc}=15V$**



**Figure 36. IR2108S vs. Frequency
 (IRFPE50), $R_{gate}=10\Omega$, $V_{cc}=15V$**



**Figure 37. IR21084S vs. Frequency (IRFBC20),
 $R_{gate}=33\Omega$, $V_{cc}=15V$**



**Figure 38. IR21084S vs. Frequency (IRFBC30),
 $R_{gate}=22\Omega$, $V_{cc}=15V$**

IR2108(4) (S) & (PbF)

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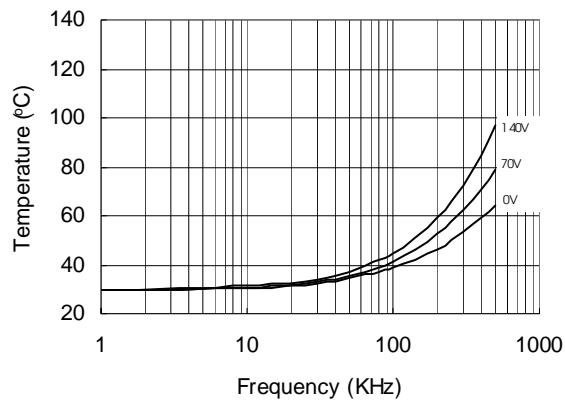


Figure 39. IR21084S vs. Frequency (IRFBC40),
 $R_{gate}=15\Omega$, $V_{cc}=15V$

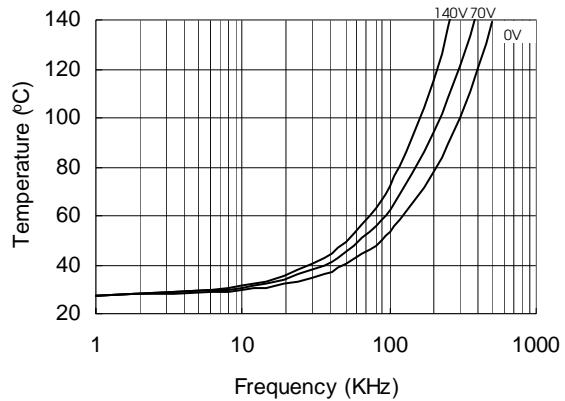
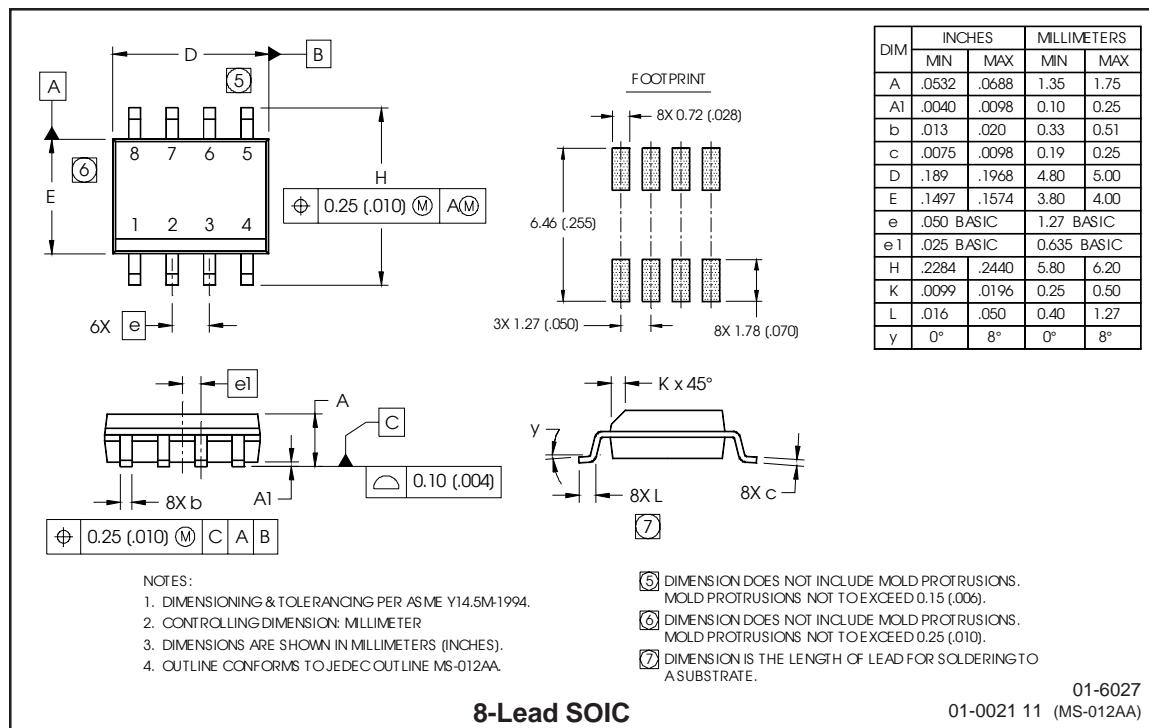
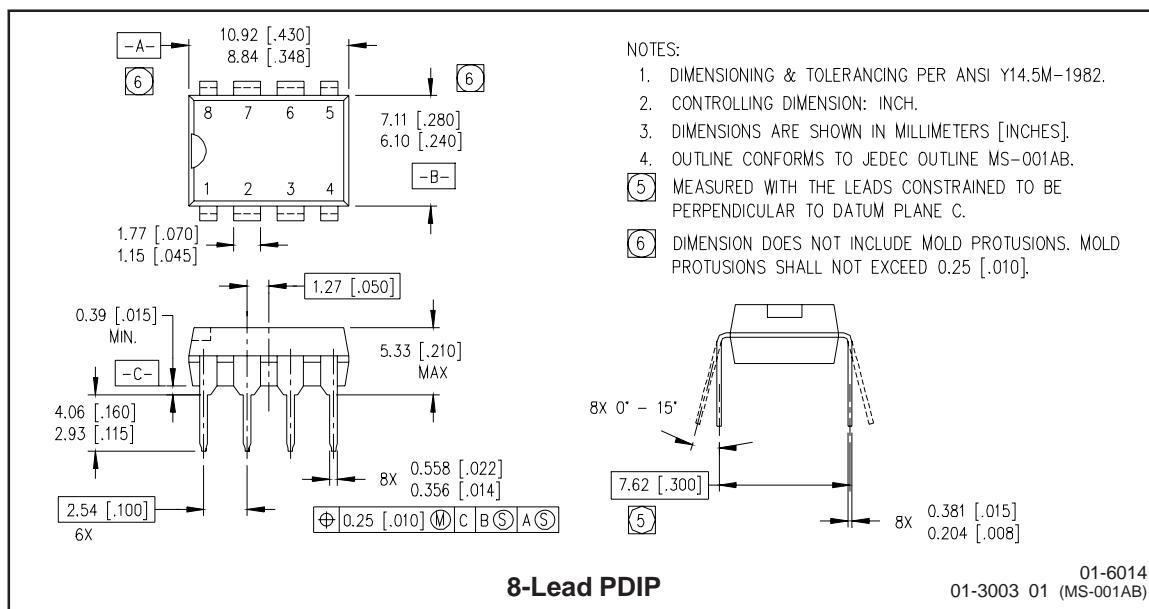


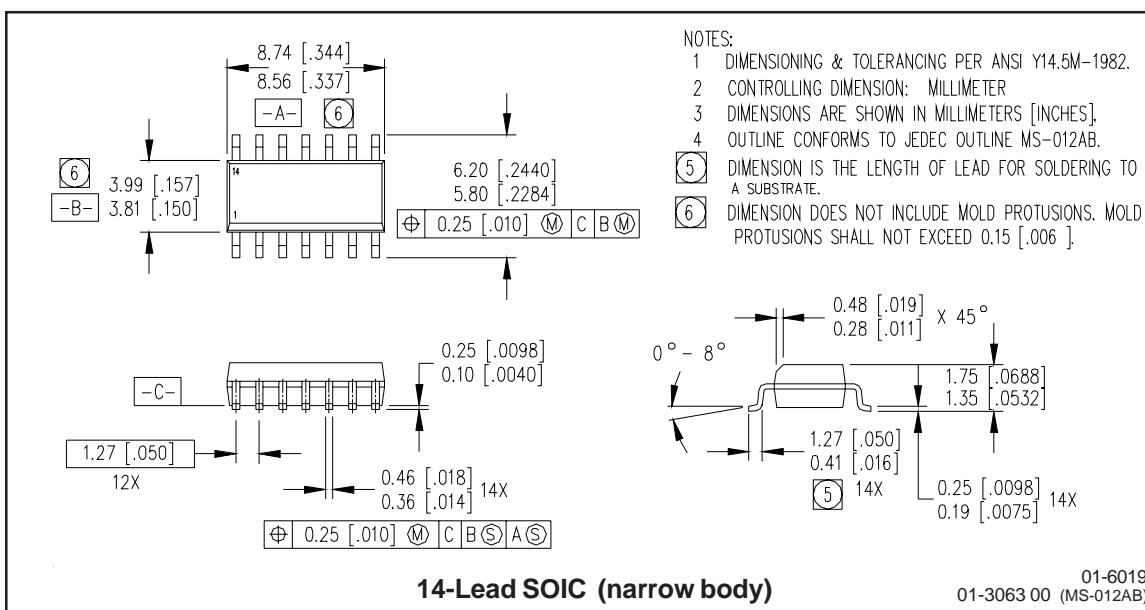
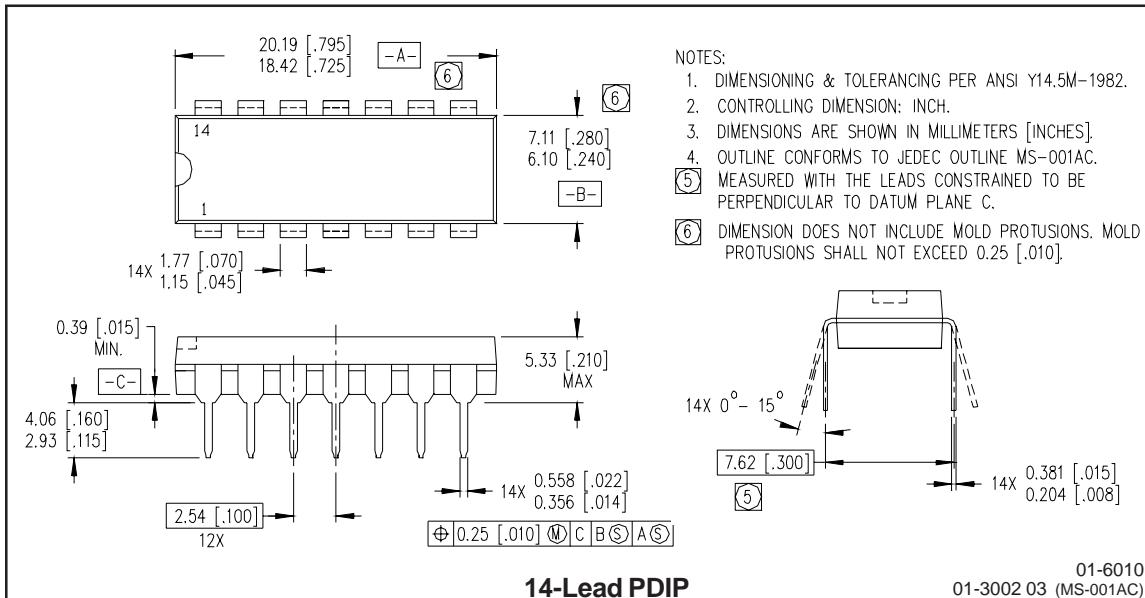
Figure 40. IR21084S vs. Frequency (IRFPE50),
 $R_{gate}=10\Omega$, $V_{cc}=15V$

Case outlines



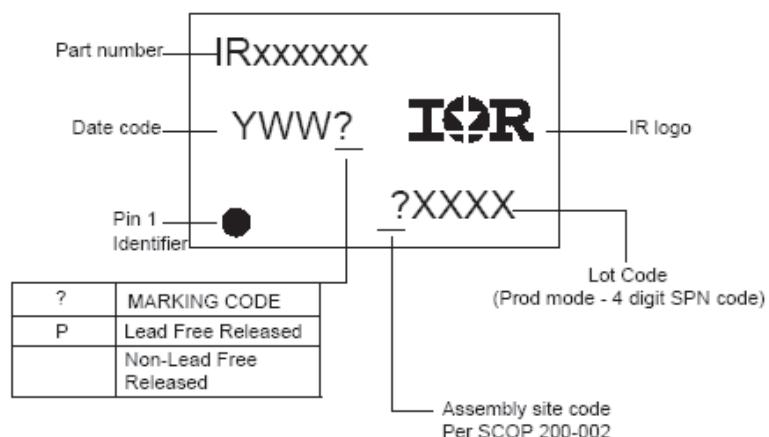
IR2108(4) (S) & (PbF)

International
IR Rectifier



IR2108(4) (S) & (PbF)

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR2108 order IR2108
 8-Lead SOIC IR2108S order IR2108S
 14-Lead PDIP IR21084 order IR21084
 14-Lead SOIC IR21084S order IR21084S

Lead-Free Part

8-Lead PDIP IR2108 order IR2108PbF
 8-Lead SOIC IR2108S order IR2108SPbF
 14-Lead PDIP IR21084 order IR21084PbF
 14-Lead SOIC IR21084S order IR21084SPbF

International
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This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Website.

Data and specifications subject to change without notice.

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
 TAC Fax: (310) 252-7903

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