

## IR2111(S) & (PbF)

### HALF-BRIDGE DRIVER

#### Features

- Floating channel designed for bootstrap operation  
 Fully operational to +600V  
 Tolerant to negative transient voltage  
 dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels
- Internally set deadtime
- High side output in phase with input
- Also available LEAD-FREE

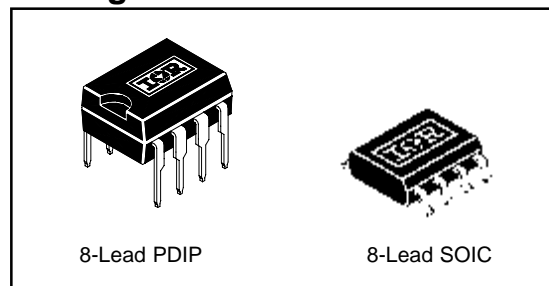
#### Description

The IR2111(S) is a high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels designed for half-bridge applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Internal deadtime is provided to avoid shoot-through in the output half-bridge. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

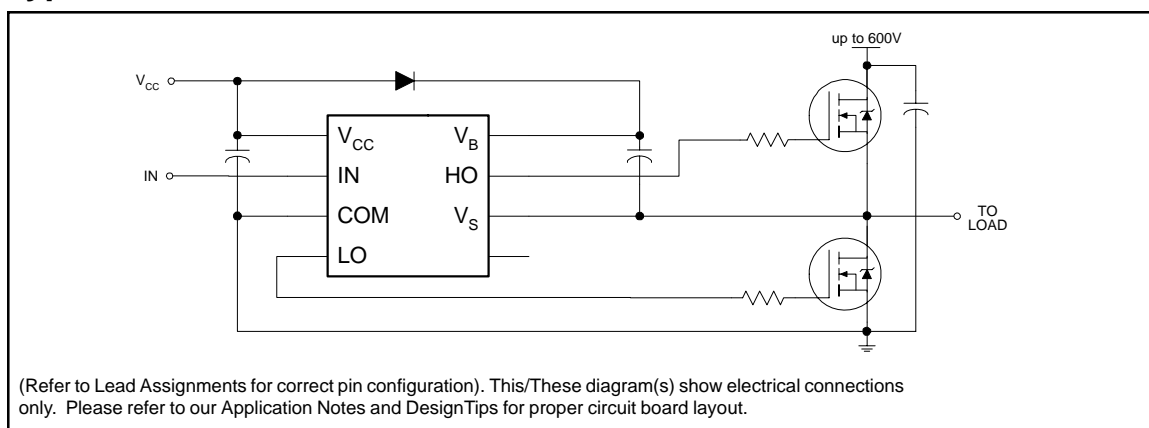
#### Product Summary

$V_{\text{OFFSET}}$	600V max.
$I_{\text{O}+/-}$	200 mA / 420 mA
$V_{\text{OUT}}$	10 - 20V
$t_{\text{on/off}}$ (typ.)	750 & 150 ns
Deadtime (typ.)	650 ns

#### Packages



#### Typical Connection



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in figures 7 through 10.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High side floating supply voltage	-0.3	625	V	
V <sub>S</sub>	High side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>CC</sub>	Low side and logic fixed supply voltage	-0.3	25		
V <sub>LO</sub>	Low side output voltage	-0.3	V <sub>CC</sub> + 0.3		
V <sub>IN</sub>	Logic input voltage	-0.3	V <sub>CC</sub> + 0.3		
dV <sub>S</sub> /dt	Allowable offset supply voltage transient (figure 2)	—	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	(8 Lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High side floating supply absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High side floating supply offset voltage	Note 1	600	
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low side and logic fixed supply voltage	10	20	
V <sub>LO</sub>	Low side output voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input voltage	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

Note 1: Logic operational for V<sub>S</sub> of -5 to +600V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in figure 3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	550	750	950	ns	$V_S = 0V$
$t_{off}$	Turn-off propagation delay	—	150	180		$V_S = 600V$
$t_r$	Turn-on rise time	—	80	130		
$t_f$	Turn-off fall time	—	40	65		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on	480	650	820		
MT	Delay matching, HS & LS turn-on/off	—	30	—		

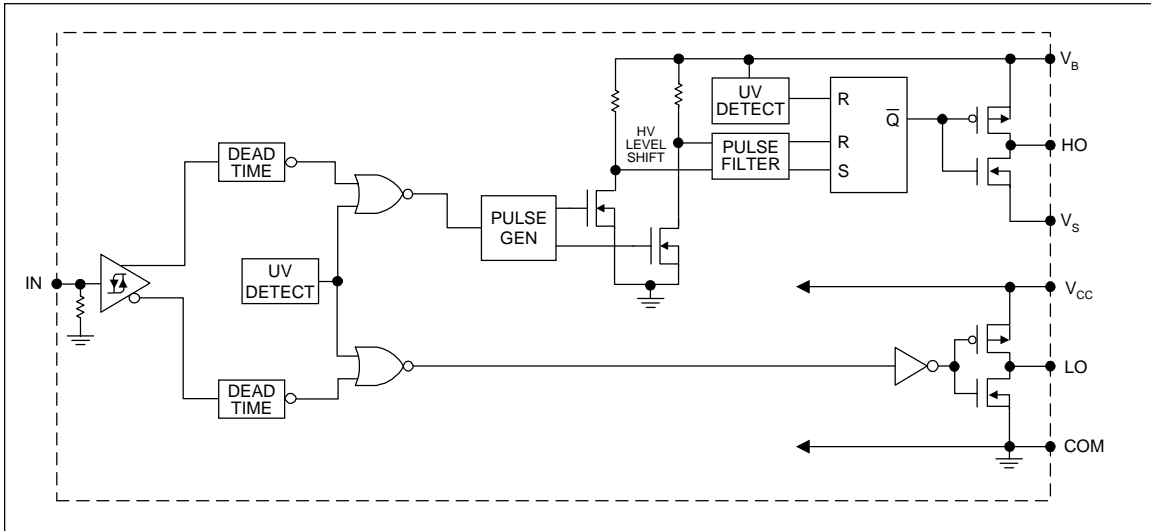
## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage for HO & logic "0" for LO	6.4	—	—	V	$V_{CC} = 10V$
		9.5	—	—		$V_{CC} = 15V$
		12.6	—	—		$V_{CC} = 20V$
$V_{IL}$	Logic "0" input voltage for HO & logic "1" for LO	—	—	3.8		$V_{CC} = 10V$
		—	—	6.0		$V_{CC} = 15V$
		—	—	8.3		$V_{CC} = 20V$
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
$V_{OL}$	Low level output voltage, $V_O$	—	—	100		$I_O = 0A$
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	50	100		$V_{IN} = 0V$ or $V_{CC}$
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	70	180		$V_{IN} = 0V$ or $V_{CC}$
$I_{IN+}$	Logic "1" input bias current	—	30	50		$V_{IN} = V_{CC}$
$I_{IN-}$	Logic "0" input bias current	—	—	1.0		$V_{IN} = 0V$
$V_{BSUV+}$	$V_{BS}$ supply undervoltage positive going threshold	7.6	8.6	9.6	V	
$V_{BSUV-}$	$V_{BS}$ supply undervoltage negative going threshold	7.2	8.2	9.2		
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold	7.6	8.6	9.6		
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.2	8.2	9.2		
$I_{O+}$	Output high short circuit pulsed current	200	250	—	mA	$V_O = 0V$ , $V_{IN} = V_{CC}$ $PW \leq 10 \mu s$
$I_{O-}$	Output low short circuit pulsed current	420	500	—		$V_O = 15V$ , $V_{IN} = 0V$ $PW \leq 10 \mu s$

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## Functional Block Diagram



## Lead Definitions

Symbol	Description
IN	Logic input for high side and low side gate driver outputs (HO & LO), in phase with HO
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return
V <sub>CC</sub>	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

## Lead Assignments

<p>8 Lead DIP</p>	<p>8 Lead SOIC</p>
<b>IR2111</b>	<b>IR2111S</b>
<b>Part Number</b>	

# IR2111(S) & (PbF)

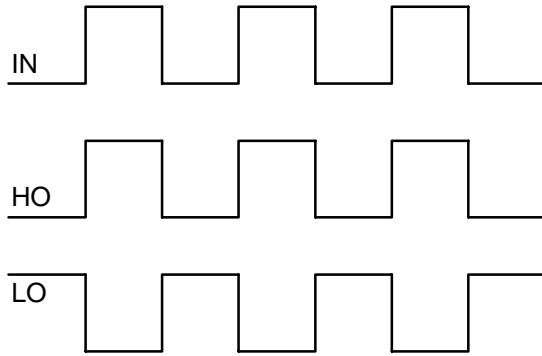


Figure 1. Input/Output Timing Diagram

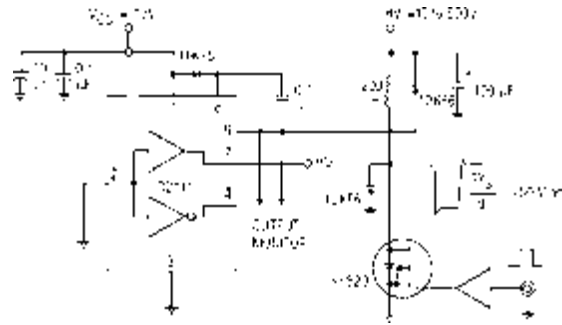


Figure 2. Floating Supply Voltage Transient Test Circuit

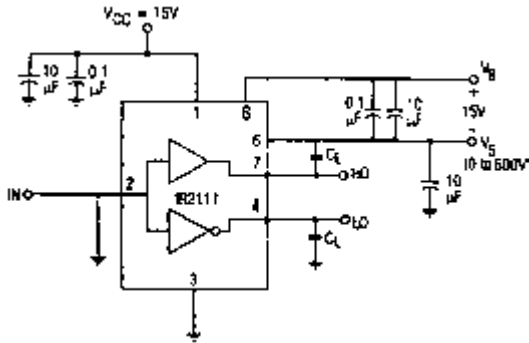


Figure 3. Switching Time Test Circuit

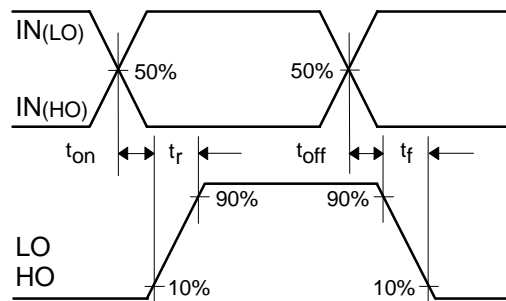


Figure 4. Switching Time Waveform Definition

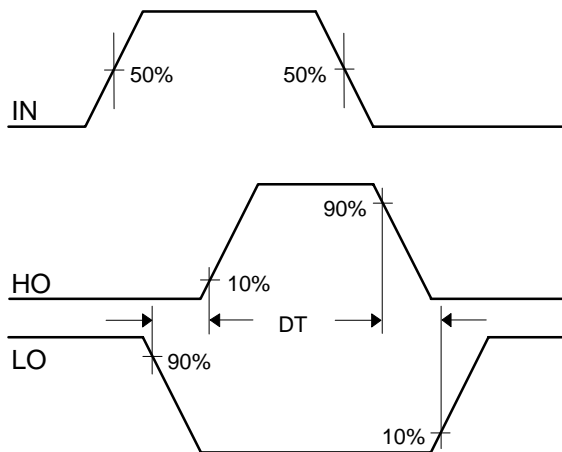


Figure 5. Deadtime Waveform Definitions

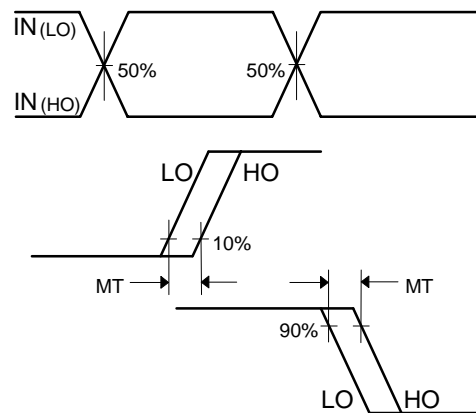


Figure 6. Delay Matching Waveform Definitions

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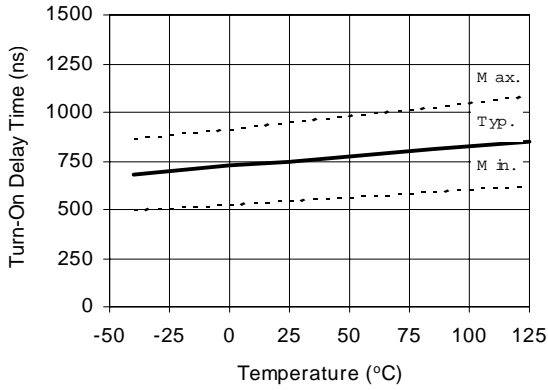


Figure 11A Turn-On Time vs Temperature

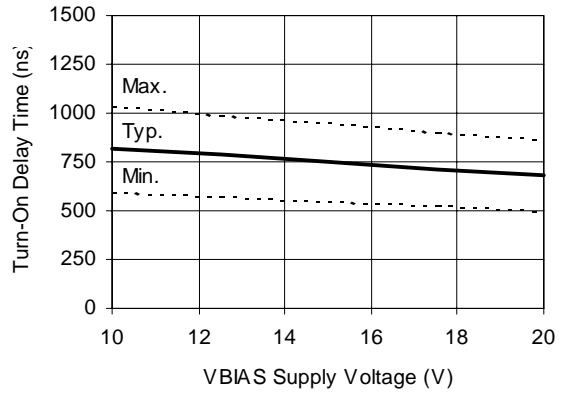


Figure 11B Turn-On Time vs Voltage

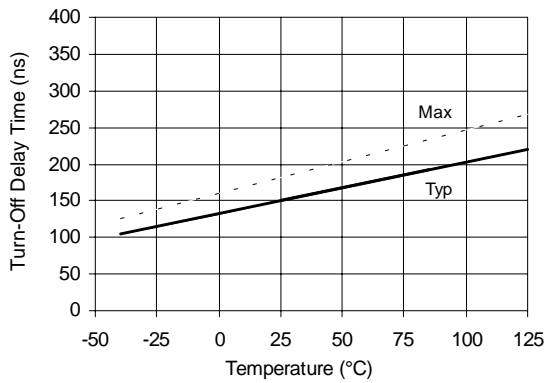


Figure 12A Turn-Off Time vs Temperature

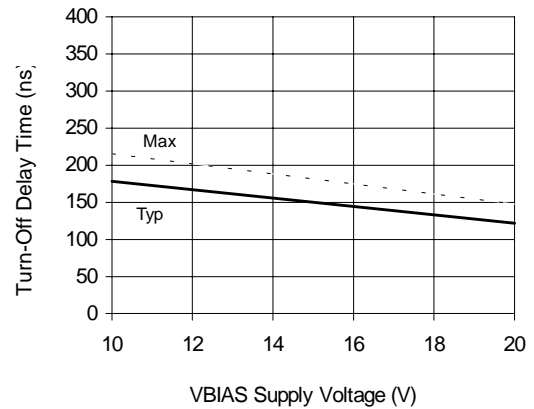


Figure 12B Turn-Off Time vs Voltage

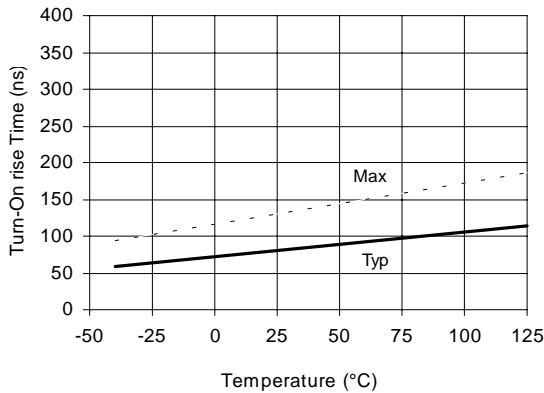


Figure 13A Turn-On Rise Time vs Temperature

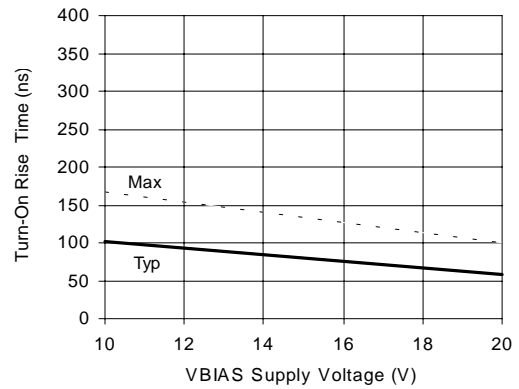


Figure 13B Turn-On Rise Time vs Voltage

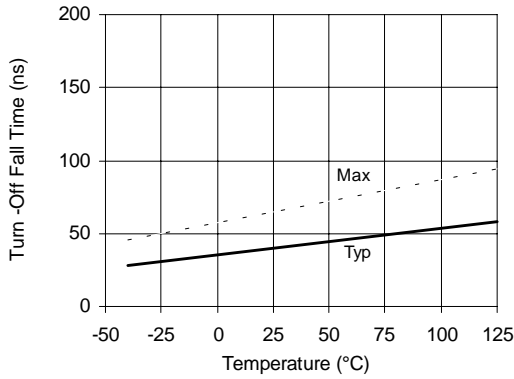


Figure 14A Turn-Off Fall Time vs Temperature

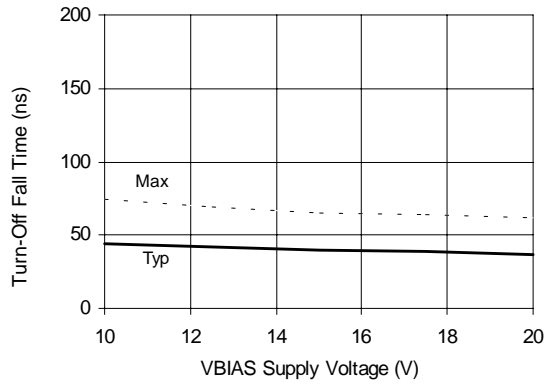


Figure 14B Turn-Off Fall Time vs Voltage

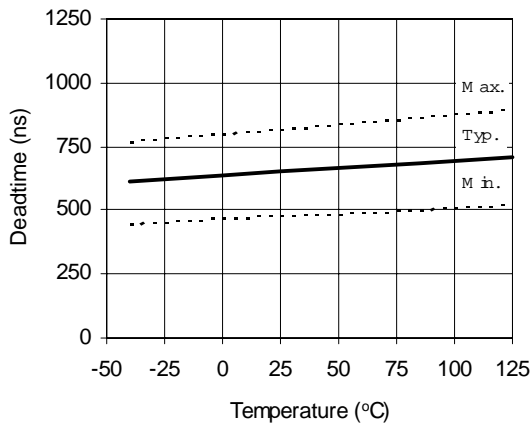


Figure 15A Dead Time vs Temperature

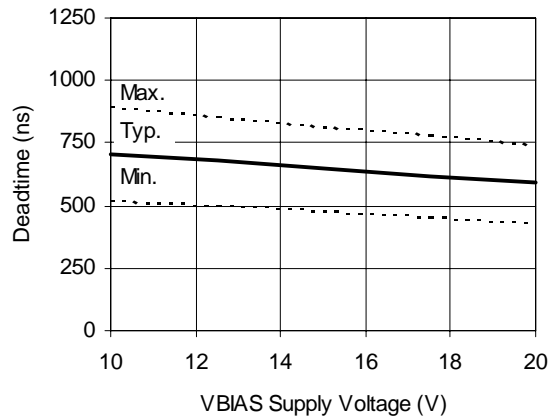


Figure 15B Dead Time vs Voltage

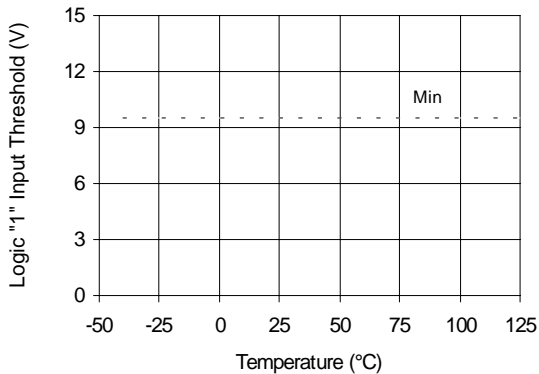


Figure 16A Logic "1" Input voltage for HO & Logic "0" for LO vs Temperature

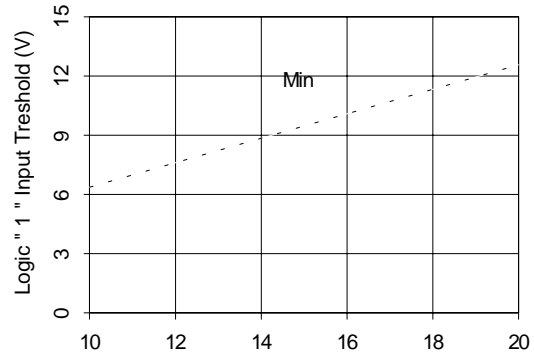
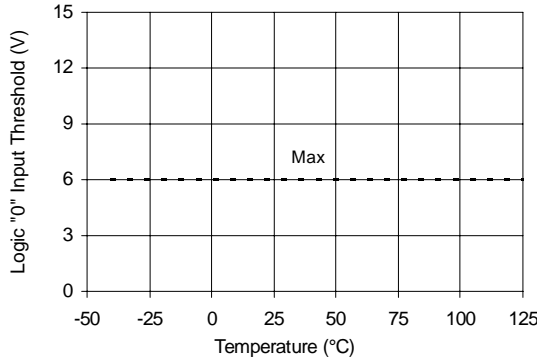
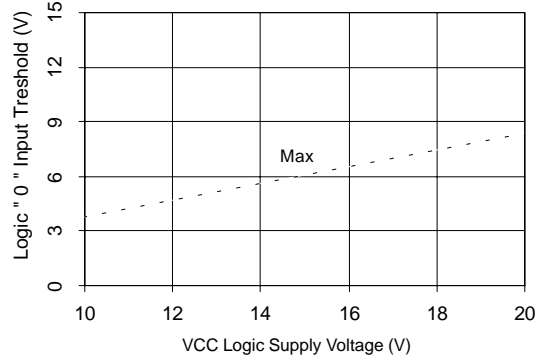


Figure 16B Logic "1" Input voltage for HO & Logic "0" for LO vs Voltage

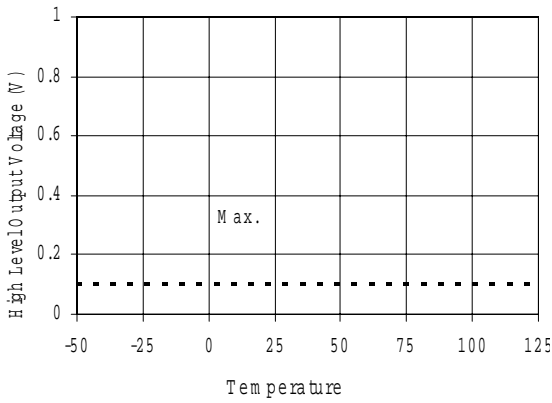
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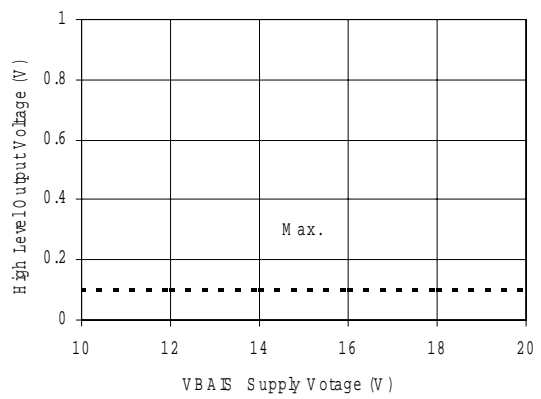
**Figure 17A Logic "0" Input voltage for HO & Logic "1" for LO vs Temperature**



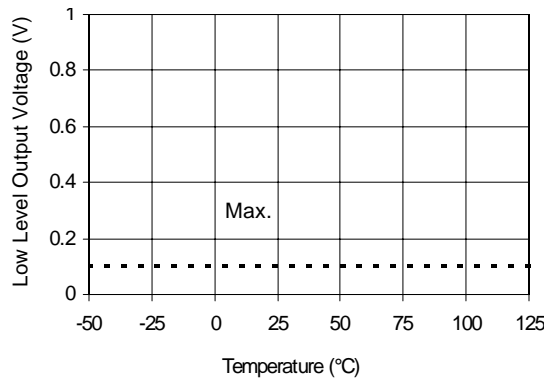
**Figure 17B Logic "0" Input voltage for HO & Logic "1" for LO vs Voltage**



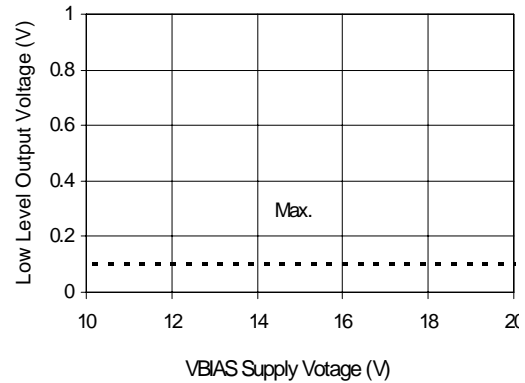
**Figure 18A. High Level Output vs. Temperature**



**Figure 18B. High Level Output vs. Voltage**



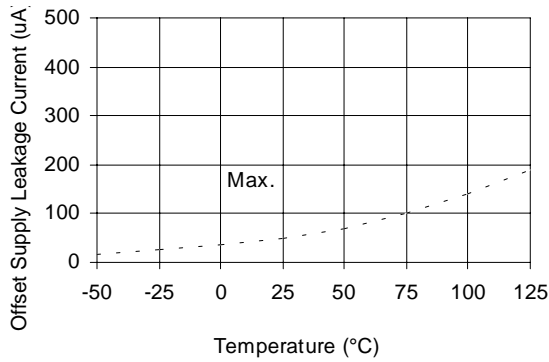
**Figure 19A. Low Level Output vs. Temperature**



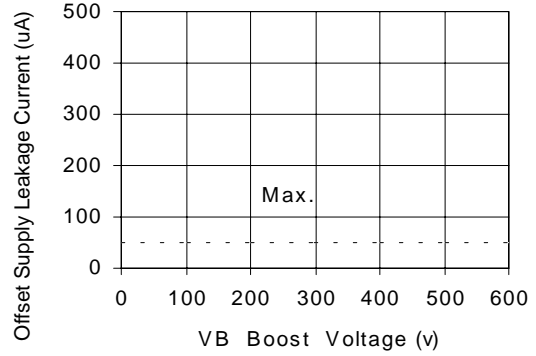
**Figure 19B. Low Level Output vs. Voltage**



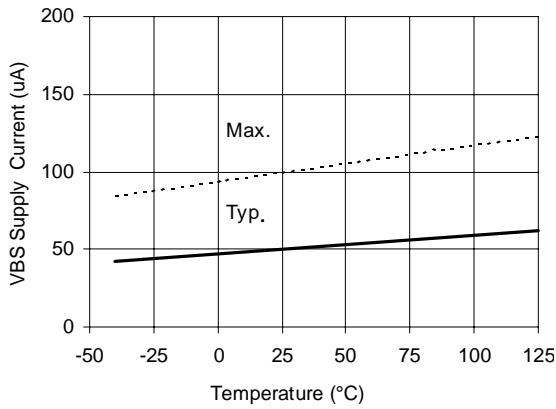
# IR2111(S) & (PbF)



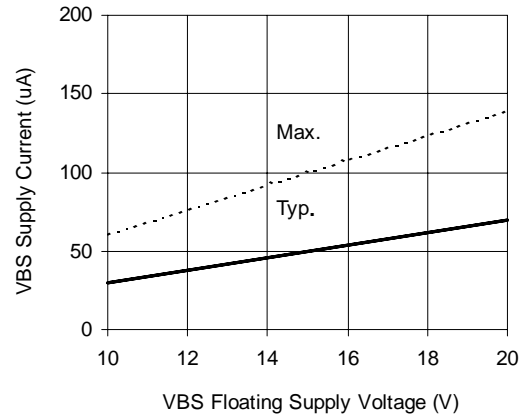
**Figure 20A Offset Supply Current vs Temperature**



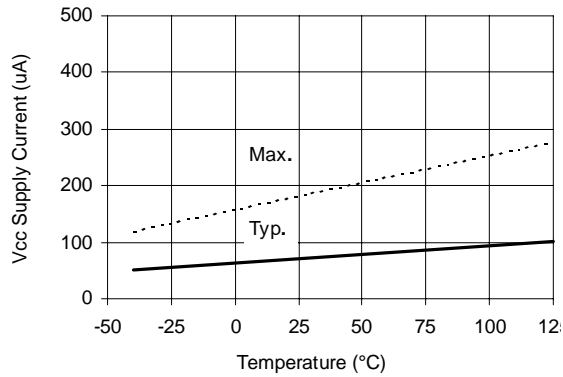
**Figure 20B Offset Supply Current vs Voltage**



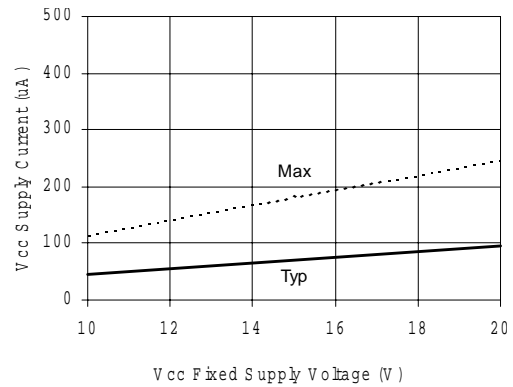
**Figure 21A VBS Supply Current vs Temperature**



**Figure 21B VBS Supply Current vs Voltage**



**Figure 22A VCC Supply Current vs Temperature**



**Figure 22B VCC Supply Current vs Voltage**

# IR2111(S)&(PbF)

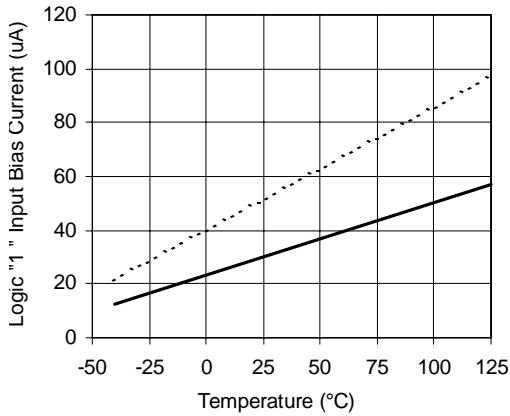


Figure 23A Logic "1" Input Current vs Temperature

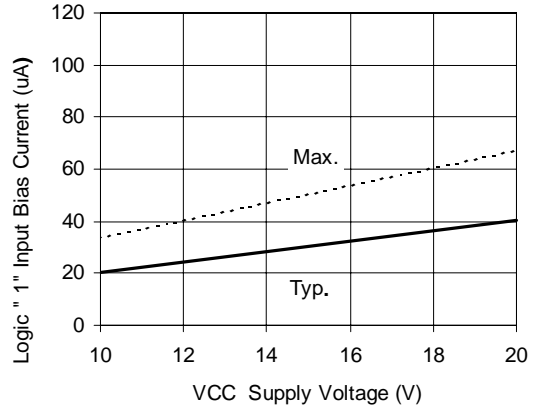


Figure 23B Logic "1" Input Current vs Vcc Voltage

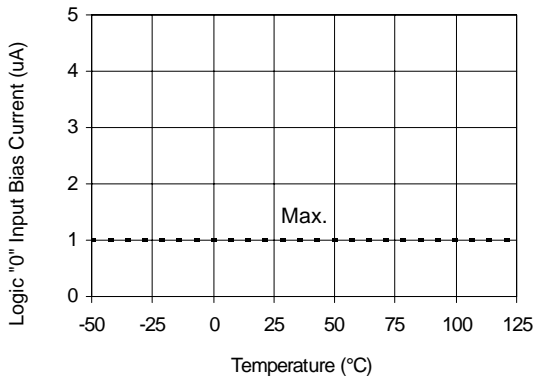


Figure 24A. Logic "0" Input Current vs. Temperature

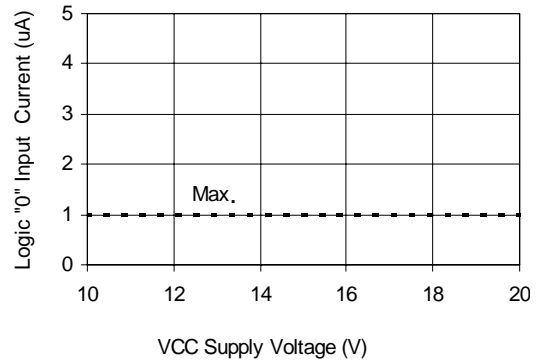


Figure 24B. Logic "0" Input Current vs. Vcc Voltage

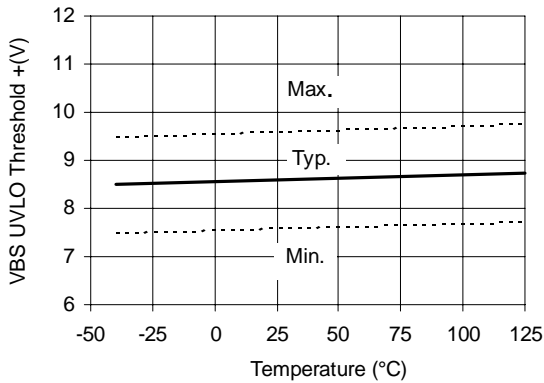


Figure 25 VBS Undervoltage Threshold (+) vsTemperature

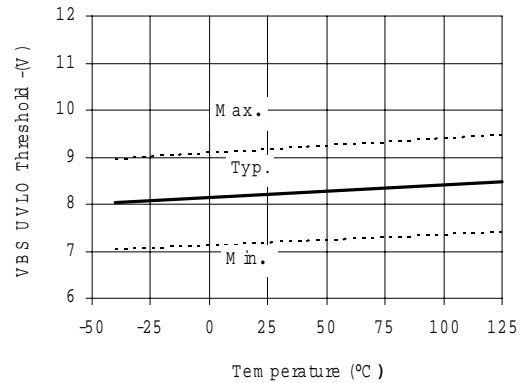


Figure 26 VBS Undervoltage Threshold (-) vsTemperature

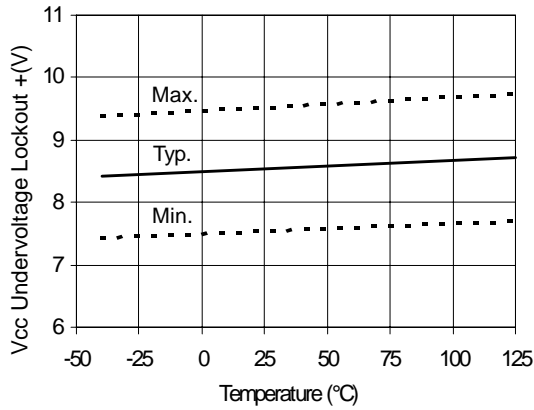


Figure 27 Vcc Undervoltage (-) vs Temperature

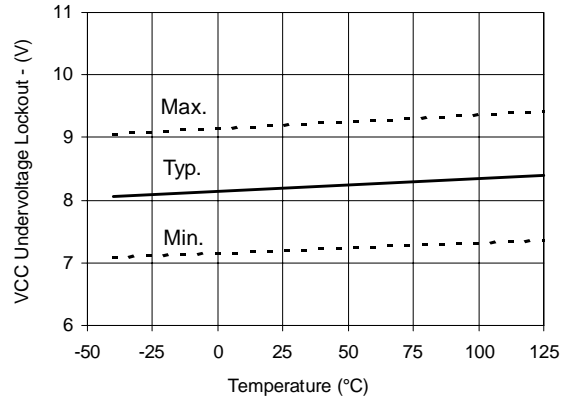


Figure 28 Vcc Undervoltage (-) vs Temperature

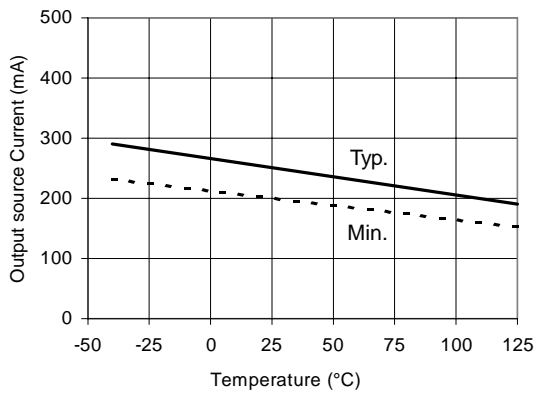


Figure 29A Output Source Current vs Temperature

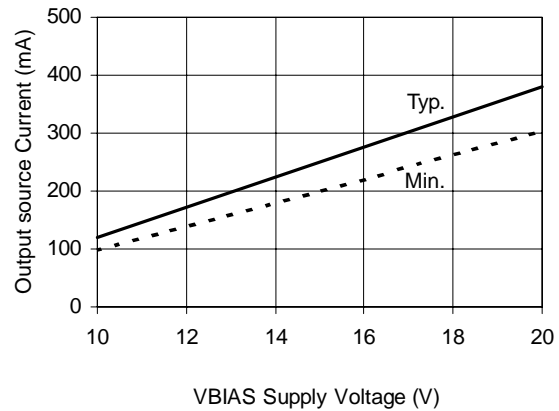


Figure 29B Output Source Current vs Voltage

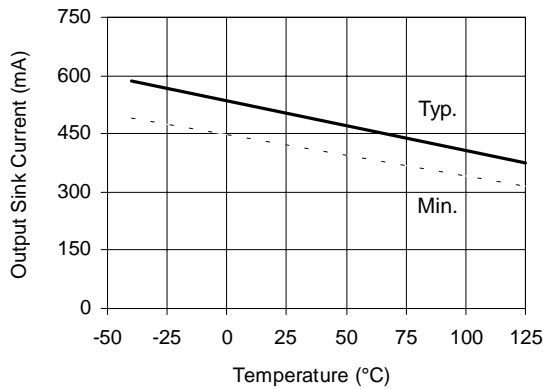


Figure 30A Output Sink Current vs Temperature

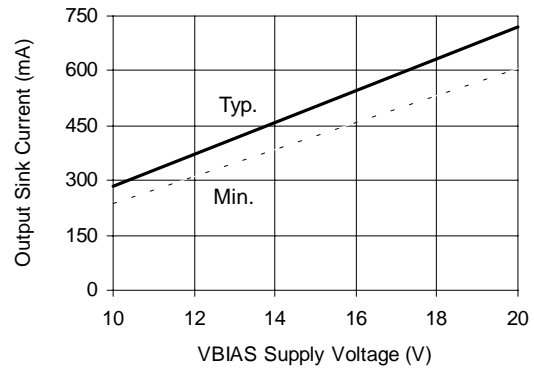


Figure 30B Output Sink Current vs Voltage

# IR2111(S)&(PbF)

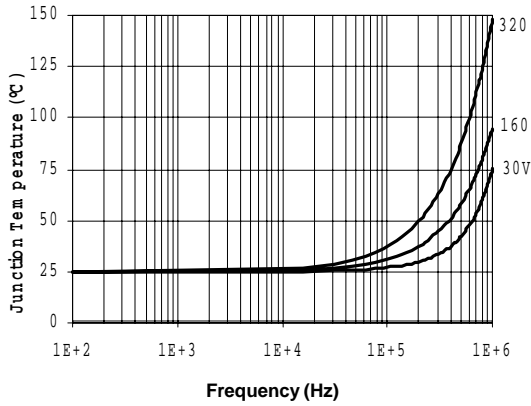


Figure 31. IR2111 T<sub>J</sub> vs. Frequency (IRFBC20)  
R<sub>GATE</sub> = 33Ω, V<sub>CC</sub> = 15V

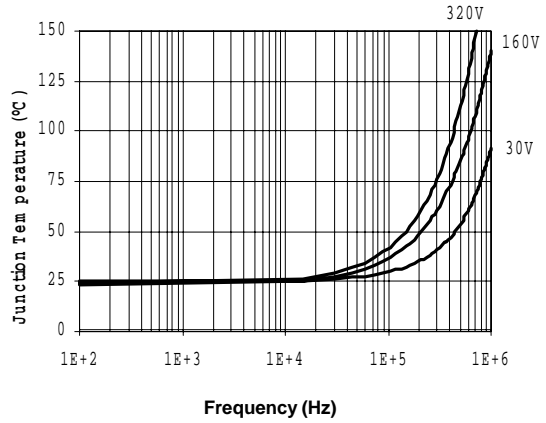


Figure 32. IR2111 T<sub>J</sub> vs. Frequency (IRFBC30)  
R<sub>GATE</sub> = 22Ω, V<sub>CC</sub> = 15V

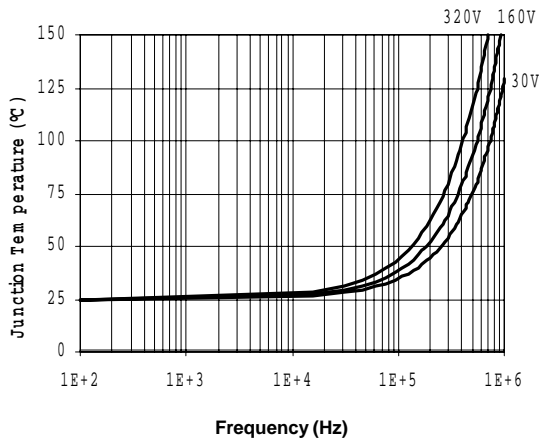


Figure 33. IR2111 T<sub>J</sub> vs. Frequency (IRFBC40)  
R<sub>GATE</sub> = 15Ω, V<sub>CC</sub> = 15V

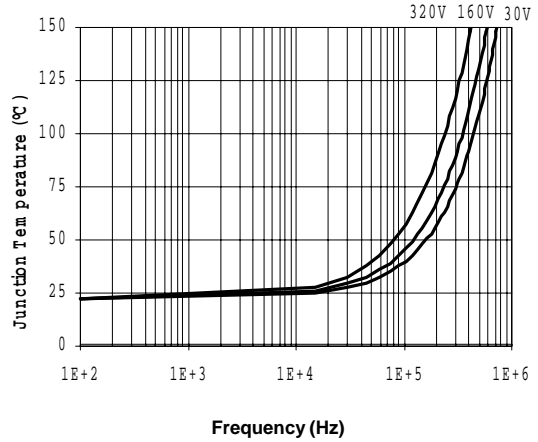
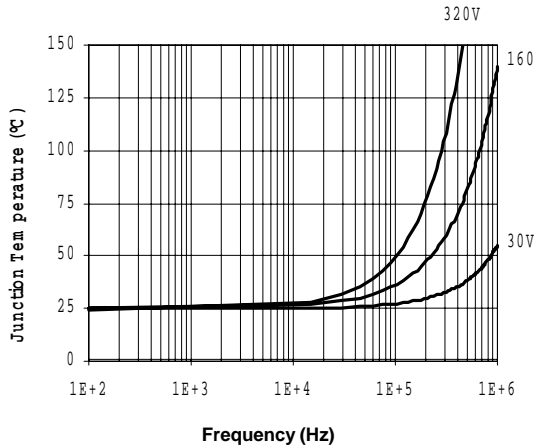
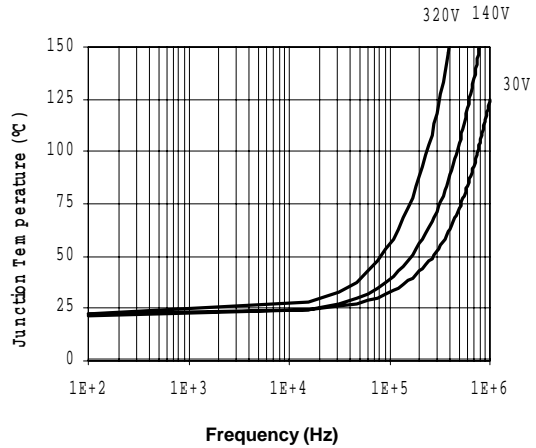


Figure 34. IR2111 T<sub>J</sub> vs. Frequency (IRFPC50)  
R<sub>GATE</sub> = 10Ω, V<sub>CC</sub> = 15V

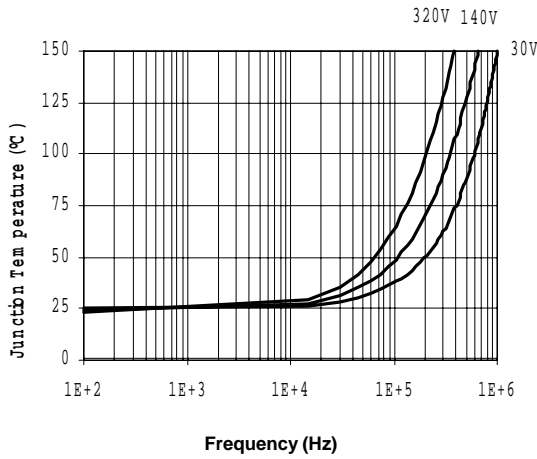
# IR2111(S) & (PbF)



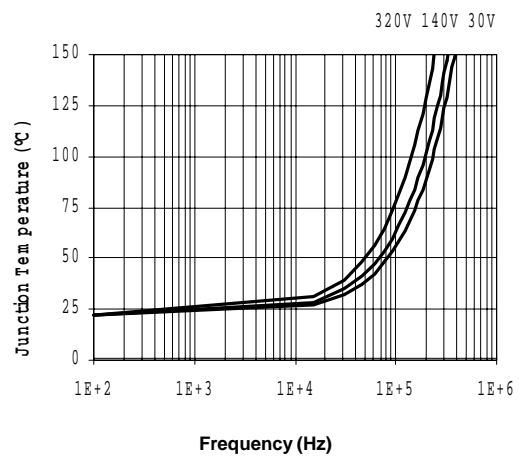
**Figure 35. IR2111S T<sub>J</sub> vs. Frequency (IRFBC20)**  
R<sub>GATE</sub> = 33Ω, V<sub>CC</sub> = 15V



**Figure 36. IR2111S T<sub>J</sub> vs. Frequency (IRFBC30)**  
R<sub>GATE</sub> = 22Ω, V<sub>CC</sub> = 15V



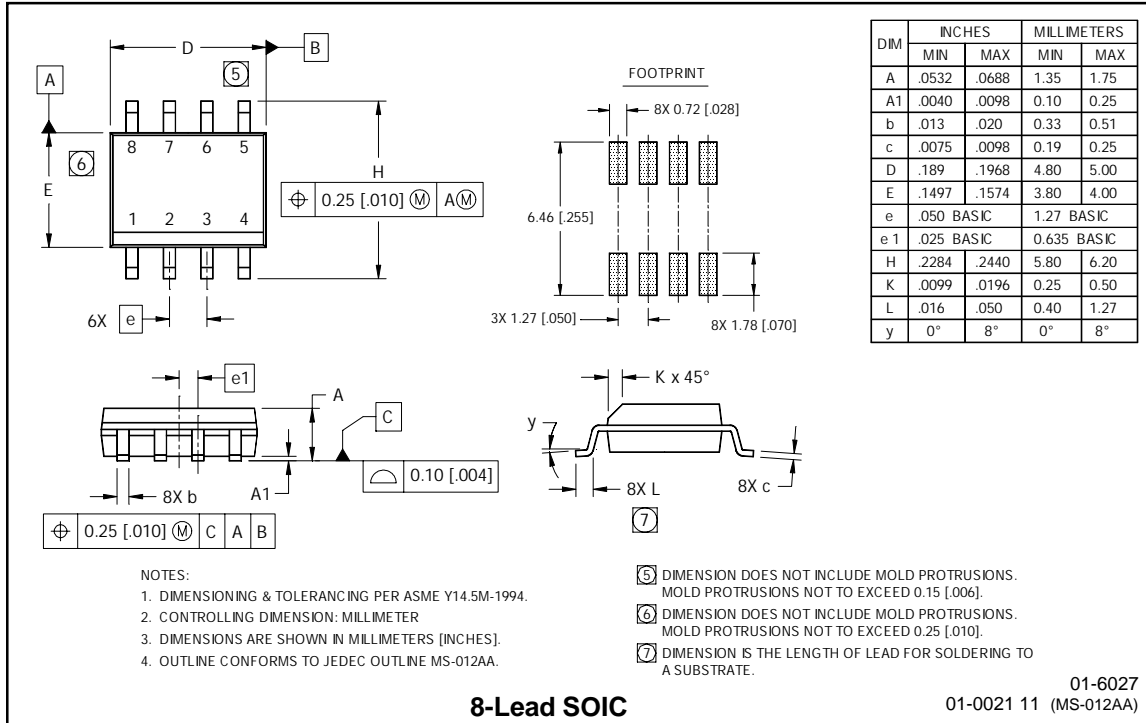
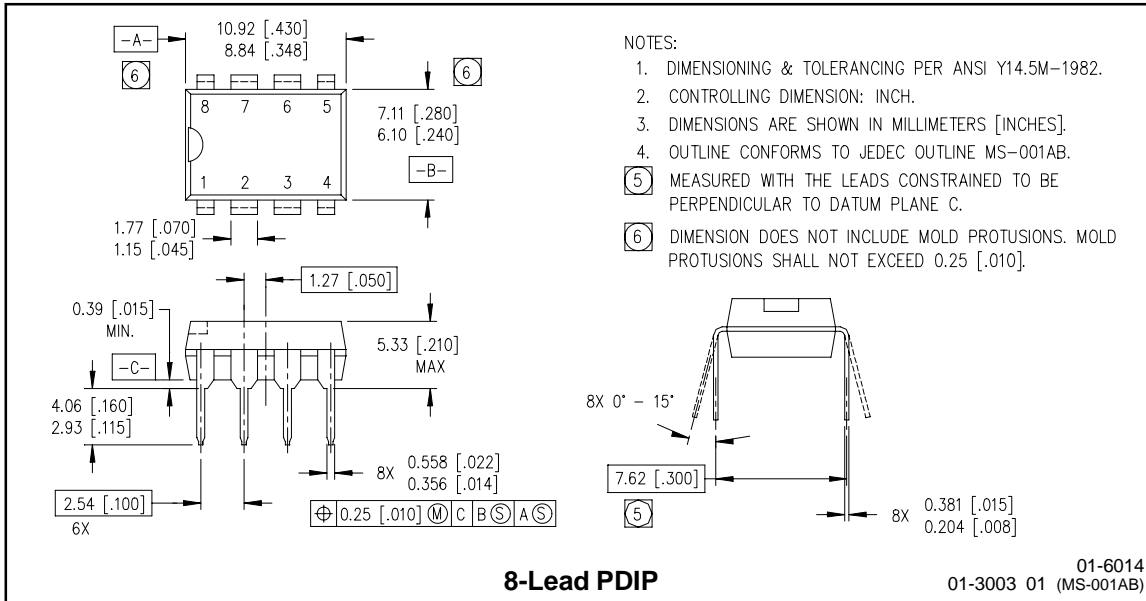
**Figure 37. IR2111S T<sub>J</sub> vs. Frequency (IRFBC40)**  
R<sub>GATE</sub> = 15Ω, V<sub>CC</sub> = 15V



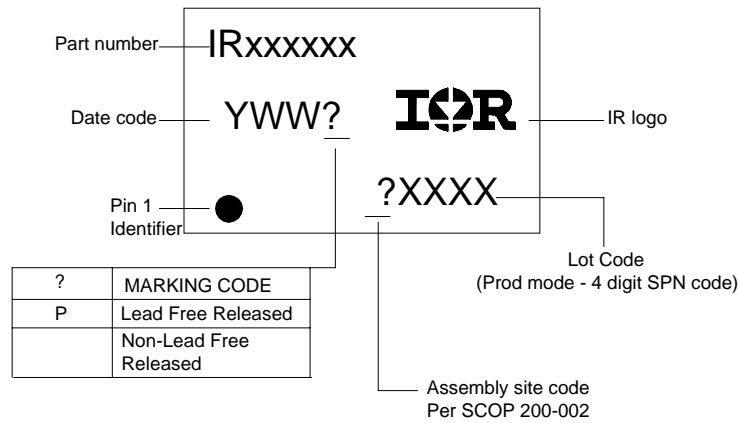
**Figure 38. IR2111S T<sub>J</sub> vs. Frequency (IRFPC50)**  
R<sub>GATE</sub> = 10Ω, V<sub>CC</sub> = 15V

# IR2111(S) & (PbF)

## Case outlines



## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

### Basic Part (Non-Lead Free)

8-Lead PDIP IR2111 order IR2111  
 8-Lead SOIC IR2111S order IR2111S

### Leadfree Part

8-Lead PDIP IR2111 order IR2111PbF  
 8-Lead SOIC IR2111S order IR2111SPbF