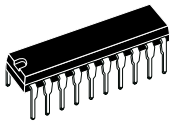
L6234

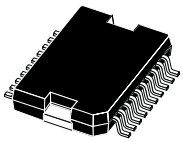
Three phase motor driver

Features

- Supply voltage from 7 to 52 V
- 5 A peak current
- R_{DSon} 0.3 Ω typ. value at 25 °C
- Cross conduction protection
- TTL compatible driver
- Operating frequency up to 150 kHz
- Thermal shutdown
- Intrinsic fast free wheeling diodes
- Input and enable function for each half bridge
- 10 V external reference available



POWER DIP (16+2+2)



PowerSO20

Description

The L6234 is a triple half bridge to drive a brushless DC motor.

It is realized in BCDmultipower technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip.

By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performance.

The output DMOS transistors can sustain a very high current due to the fact that the DMOS structure is not affected by the second breakdown effect, the RMS maximum current is practically limited by the dissipation capability of the package.

All the logic inputs are TTL, CMOS and µP compatible. Each channel is controlled by two separate logic input.

L6234 is available in 20 pin PowerDIP package (16+2+2) and in PowerSO20.

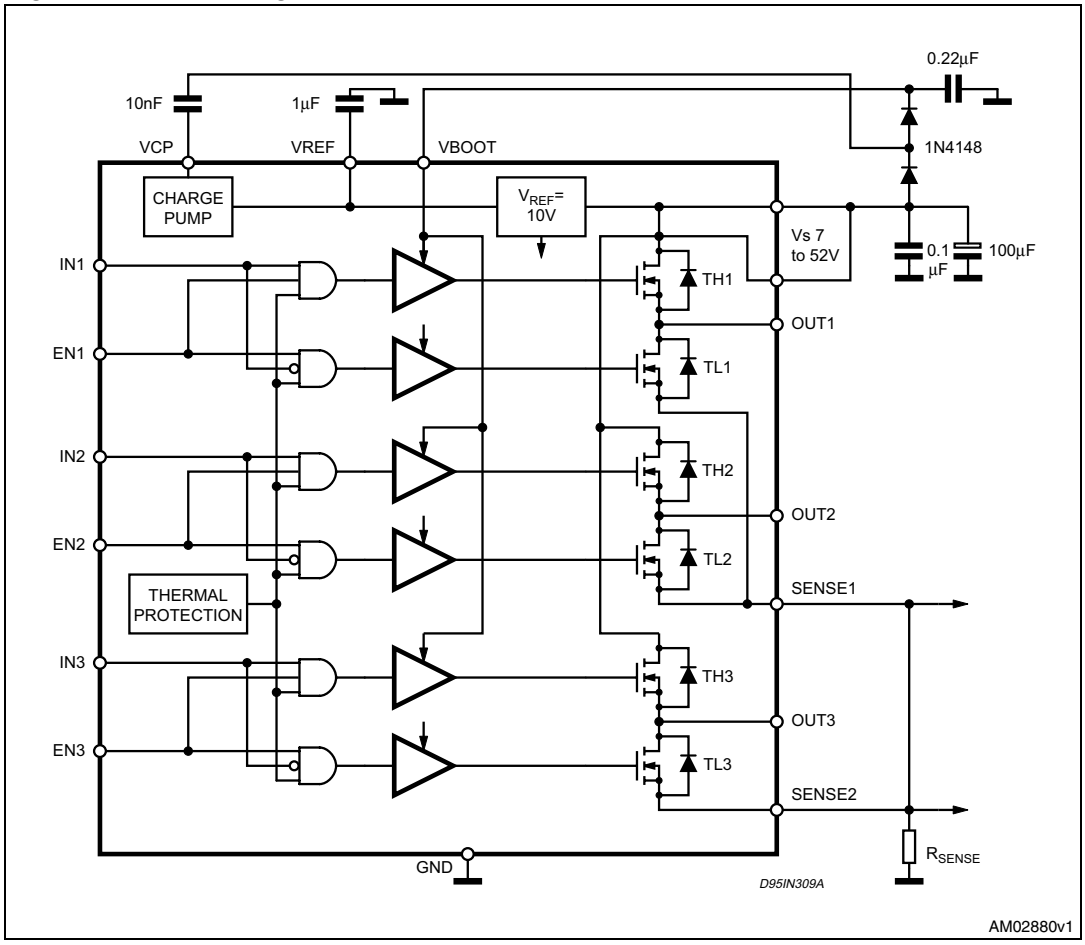
Table 1. Device summary

Order code	Package	Packing
L6234	PowerDIP20	Tube
L6234PD	PowerSO20	Tube
L6234PD013TR	PowerSO20	Tape and reel

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin connections

Figure 2. Pin connections

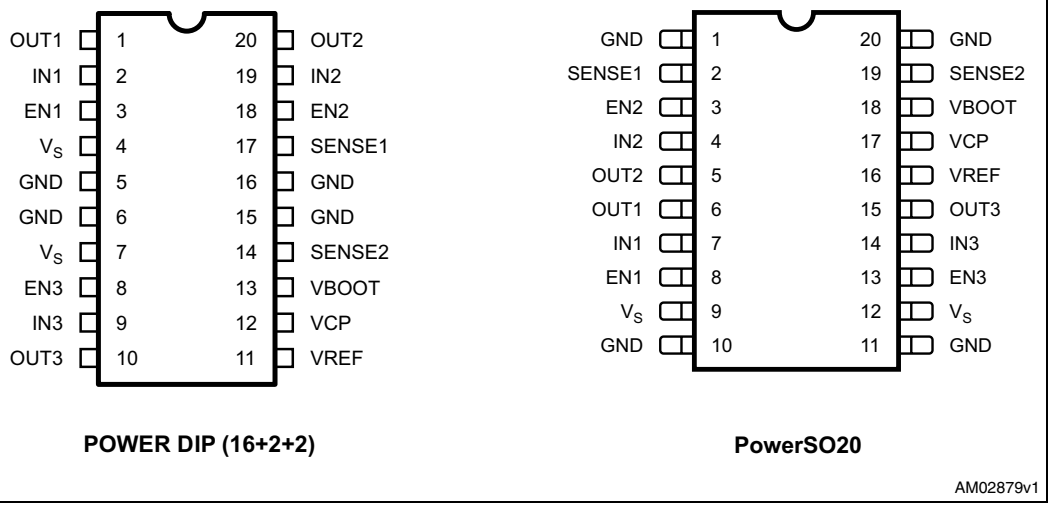


Table 2. Pin functions

PowerDIP	PowerSO20	Name	Function
1 20 10	6 5 15	OUT 1 OUT 2 OUT 3	Output of the channels 1/2/3.
2 19 9	7 4 14	IN 1 IN 2 IN 3	Logic input of channels 1/2/3. A logic HIGH level (when the corresponding EN pin is HIGH) switches ON the upper DMOS Power Transistor, while a logic LOW switches ON the corresponding low side DMOS Power.
3 18 8	8 3 13	EN 1 EN 2 EN 3	Enable of the channels 1/2/3. A logic LOW level on this pin switches off both power DMOS of the related channel.
4,7	9, 12	Vs	Power supply voltage.
14	19	SENSE2	A sense resistor connected to this pin provides feedback for motor current control for the bridge 3.
17	2	SENSE1	A sense resistor connected to this pin provides feedback for motor current control for the bridges 1 and 2.
11	16	VREF	Internal voltage reference. A capacitor connected from this pin to GND increases the stability of the Power DMOS drive circuit.
12	17	VCP	Bootstrap oscillator. Oscillator output for the external charge pump.
13	18	VBOOT	Overvoltage input to drive the upper DMOS
5,6 15,16	1,10 11,20	GND	Common ground terminal. In PowerDIP and SO packages these pins are used to dissipate the heat forward the PCB.

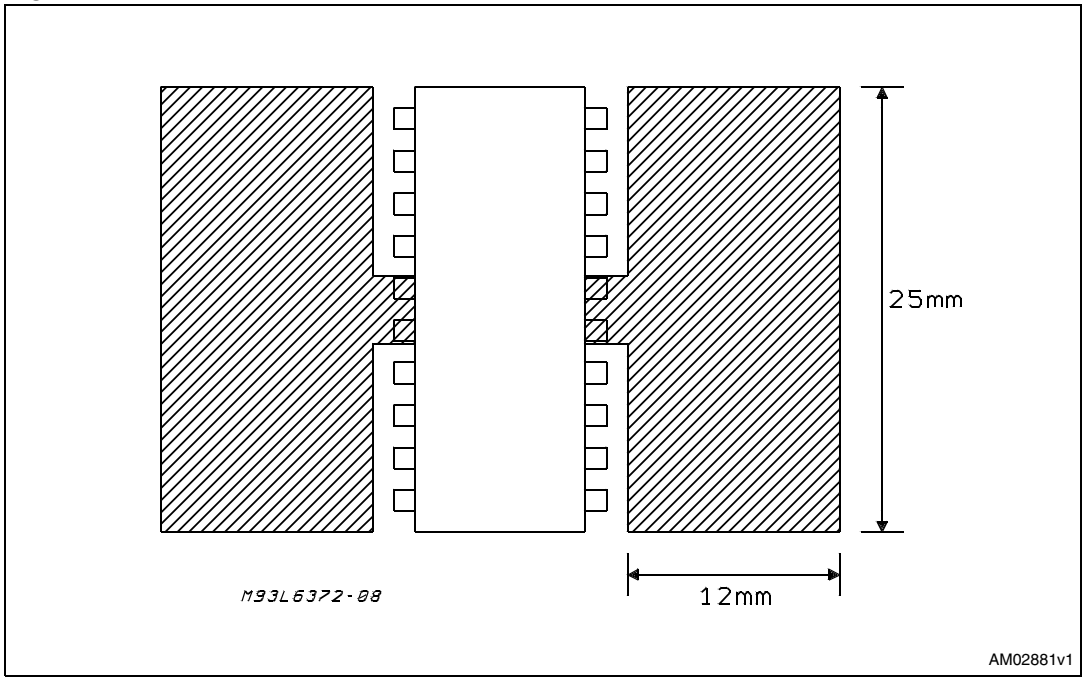
3 Thermal data

Table 3. Thermal data

Symbol	Parameter	DIP16+2+2	PowerSO20	Unit
$R_{th\ j\text{-}pin}$	Thermal resistance, junction to pin	12 (1)	–	°C/W
$R_{th\ j\text{-}amb1}$	Thermal resistance, junction to ambient	40 (2)	–	°C/W
$R_{th\ j\text{-}amb2}$	Thermal resistance, junction characteristics) to ambient	50 (3)	–	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	–	1.5	°C/W

1. The thermal resistance is referred to the thermal path from the dissipating region on the top surface of the silicon chip, to the points along the four central pins of the package, at a distance of 1.5 mm away from the stand-offs.
2. If a dissipating surface, thick at least 35 mm, and with a surface similar or bigger than the one shown in *Figure 3*, is created making use of the printed circuit. Such heatsinking surface is considered on the bottom side of an horizontal PCB (worst case).
3. If the power dissipating pins (the four central ones), as well as the others, have a minimum thermal connection with the external world (very thin strips only) so that the dissipation takes place through still air and through the PCB itself. It is the same situation of note 2, without any heatsinking surface created on purpose on the board.

Figure 3. Printed Heatsink



4 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Power supply voltage	52	V
V_{IN}, V_{EN}	Input enable voltage	– 0.3 to 7	V
I_{peak}	Pulsed output current (1)	5	A
V_{SENSE}	Sensing voltage (DC voltage)	-1 to 4	V
V_{boot}	Bootstrap peak voltage	62	V
V_{OD}	Differential output voltage (between any of the 3 OUT pins)	60	V
f_C	Commutation frequency	150	kHz
V_{REF}	Reference voltage	12	V
P_{tot}	Total power dissipation L6234PD, T_A = 70°C	2.3	W
P_{tot}	Total power dissipation L6234, T_A = 70°C	1.6 (2)	W
T_{stg}, T_j	Storage and junction temperature range	-40 to 150	°C

1. Pulse width limited only by junction temperature and the transient thermal impedance
2. Mounted on board with minimized copper area

4.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_S	Supply voltage	7 to 42	V
V_{OD}	Peak to peak differential voltage (between any of the 3 out pins)	52	V
I_{out}	DC output current powerSO20 (T_A = 25°C)	4	A
	DC output current powerDIP (T_A = 25°C) with infinite heatsink	2.8	A
V_{SENSE}	Sensing voltage (pulsed t_w < 300 nsec)	-4 to 4	V
	Sensing voltage (DC)	-1 to 1	V
T_j	Junction temperature range	-40 to 125	°C

5 Electrical characteristics

V_S = 42 V; T_j = 25 °C unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage		7		52	V
V_{ref}	Reference voltage			10		V
I_S	Quiescent supply current			6.5		mA
T_S	Thermal shutdown		150			°C
T_D	Dead time protection			300		ns
Output dmos transistor						
I_{DSS}	Leakage current				1	mA
R_{DSon}	ON resistance			0.3		Ω
Source drain diode						
V_{SD}	Forward ON voltage	I_{SD} = 4A; EN = LOW		1.2		V
T_{RR}	Reverse recovery time	I_F = 4A		900		ns
T_{pr}	Forward recovery time			200		ns
Logic levels						
V_{INL}, V_{ENL}	Input LOW voltage		-0.3		0.8	V
V_{INH}, V_{ENH}	Input HIGH voltage		2		7	V
I_{INL}, I_{ENL}	Input LOW current	V_{IN},V_{EN} = L			-10	µA
I_{INH}, I_{ENH}	Input HIGH current	V_{IN},V_{EN} = H		30		µA

6 Circuit description

L6234 is a triple half bridge designed to drive brushless DC motors. Each half bridge has 2 power DMOS transistors with R_{DSon} = 0.3 Ω.

The 3 half bridges can be controlled independently by means of the 3 inputs IN1, IN2, IN3 and the 3 inputs EN1, EN2, and EN3. An external connection to the 3 common low side DMOS sources is provided to connect a sensing resistor for constant current chopping application.

The driving stage and the logic stage are designed to work from 7 V to 52 V.

7 Typical characteristics

Figure 4. Quiescent current vs. supply voltage

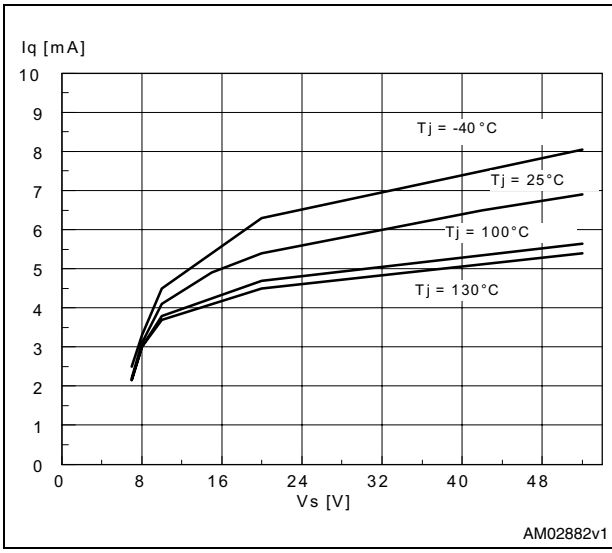


Figure 5. Normalized quiescent current vs. switching frequency

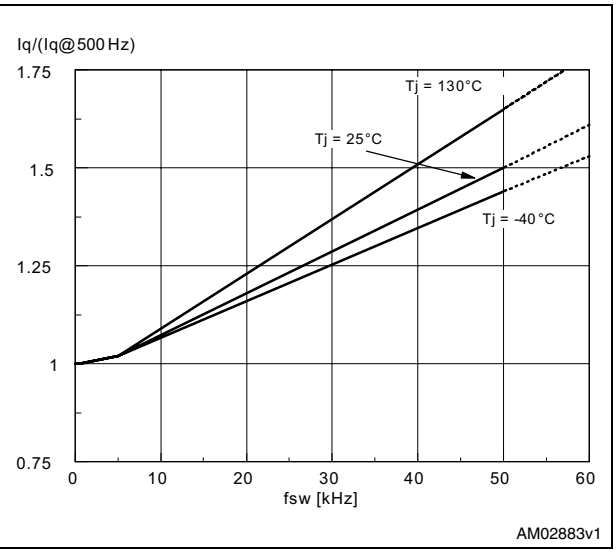


Figure 6. Typical R_{DSon} vs. supply voltage

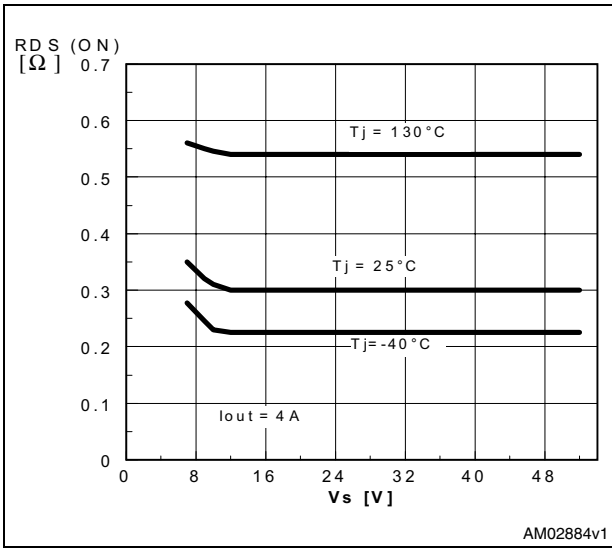


Figure 7. Source drain forward on voltage vs. junction temperature

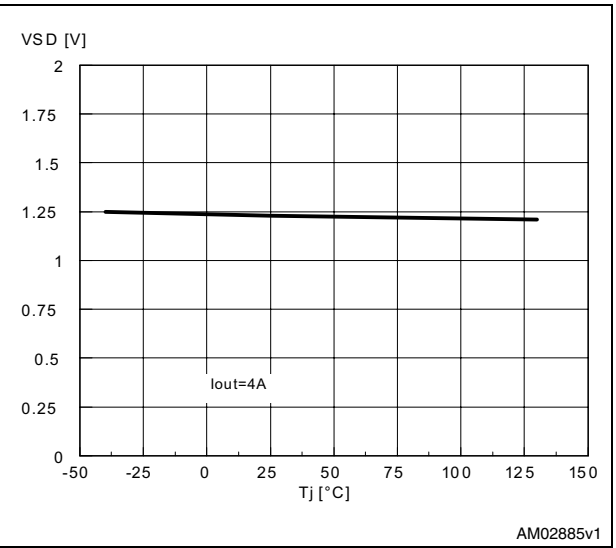


Figure 8. Typical diode forward ON characteristics

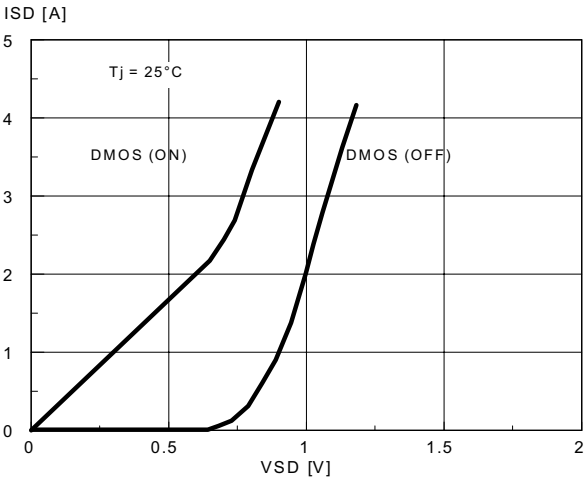


Figure 9. Reference voltage vs. supply voltage

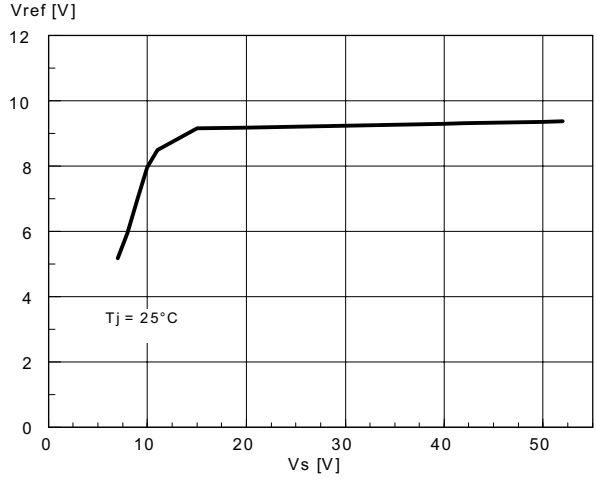


Figure 10. Reference voltage vs. junction temperature

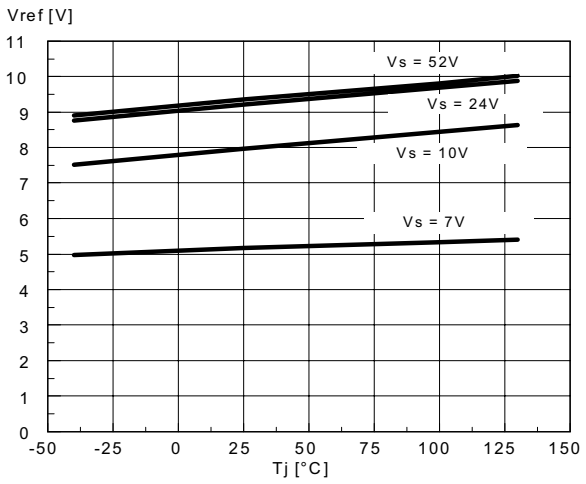


Figure 11. PowerSO-20 transient thermal resistance

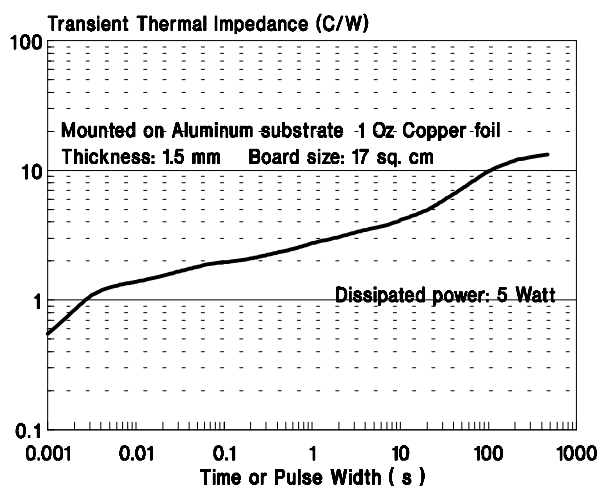


Figure 12. PowerSO-20 thermal resistance (mounted on Aluminium substrate)

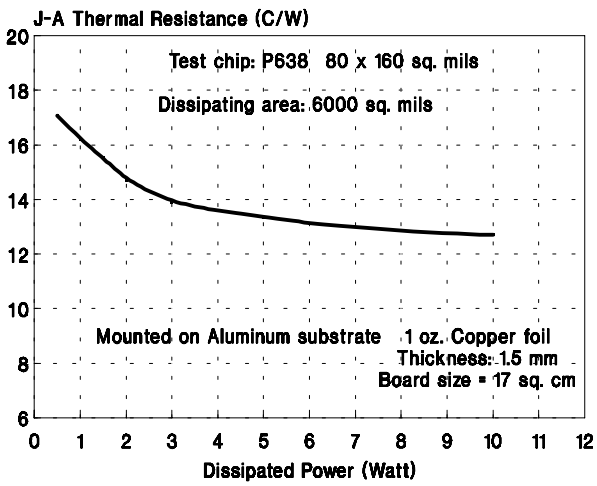


Figure 13. PowerSO-20 thermal resistance (mounted on FR4 monolayer substrate)

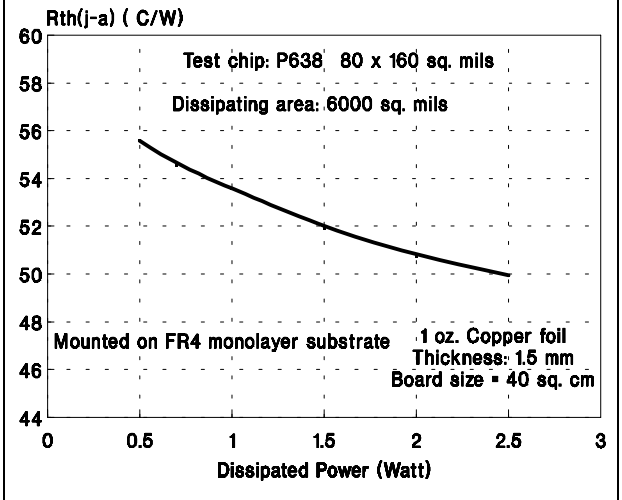


Figure 14. PowerSO-20: with external heatsink

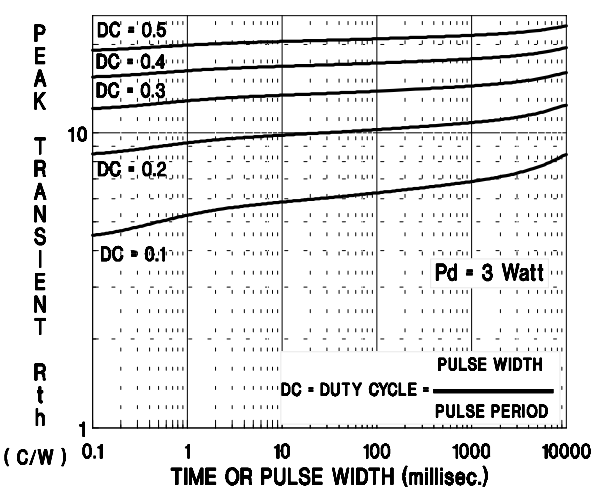
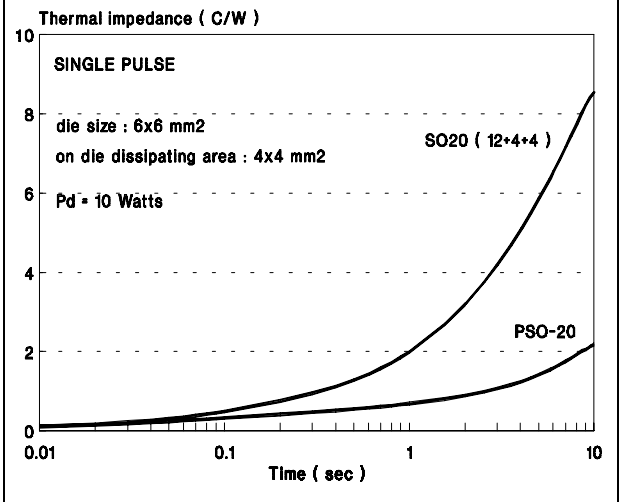


Figure 15. Thermal impedance of PowerSO-20 and standard SO20



8 Mechanical data

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Table 7. PowerSO20 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			3.6
a1	0.1		0.3
a2			3.3
a3	0		0.1
b	0.4		0.53
c	0.23		0.32
D (1)	15.8		16
D1	9.4		9.8
E	13.9		14.5
e		1.27	
e3		11.43	
E1 (1)	10.9		11.1
E2			2.9
E3	5.8		6.2
G	0		0.1
H	15.5		15.9
h			1.1
L	0.8		1.1
N	8° (typ.)		
S	8° (max.)		
T		10	

Figure 16. PowerSO20 mechanical drawing

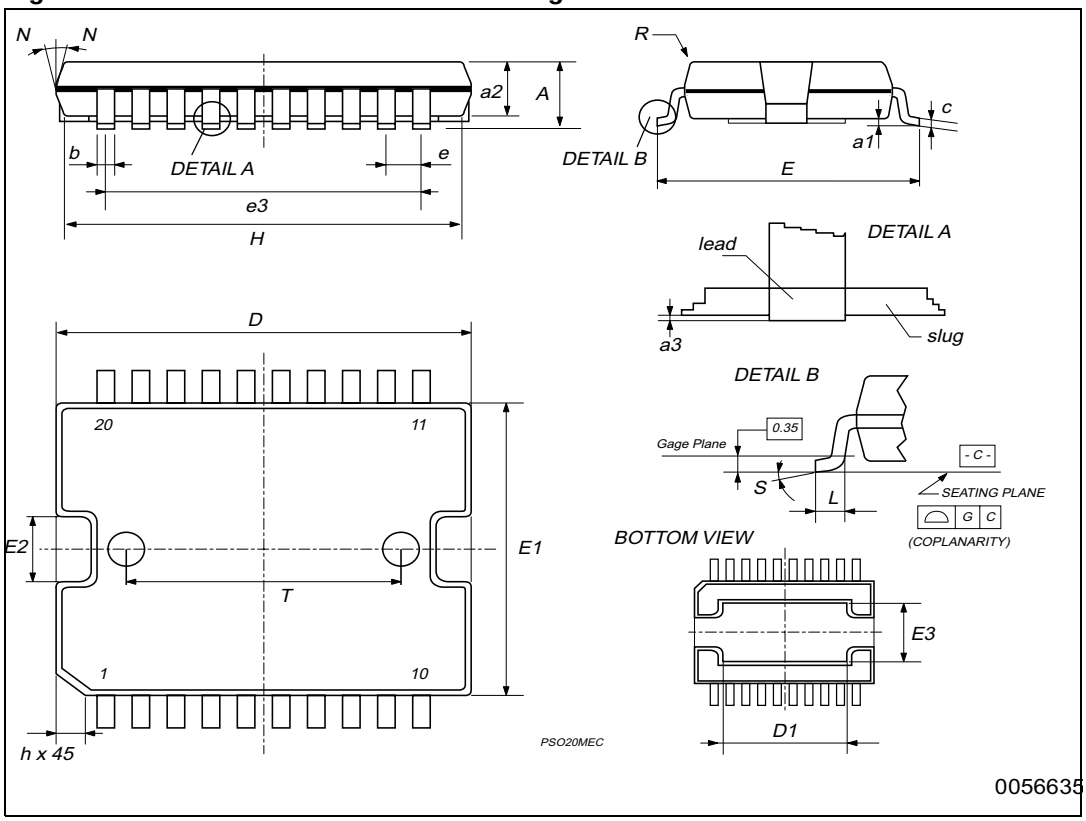
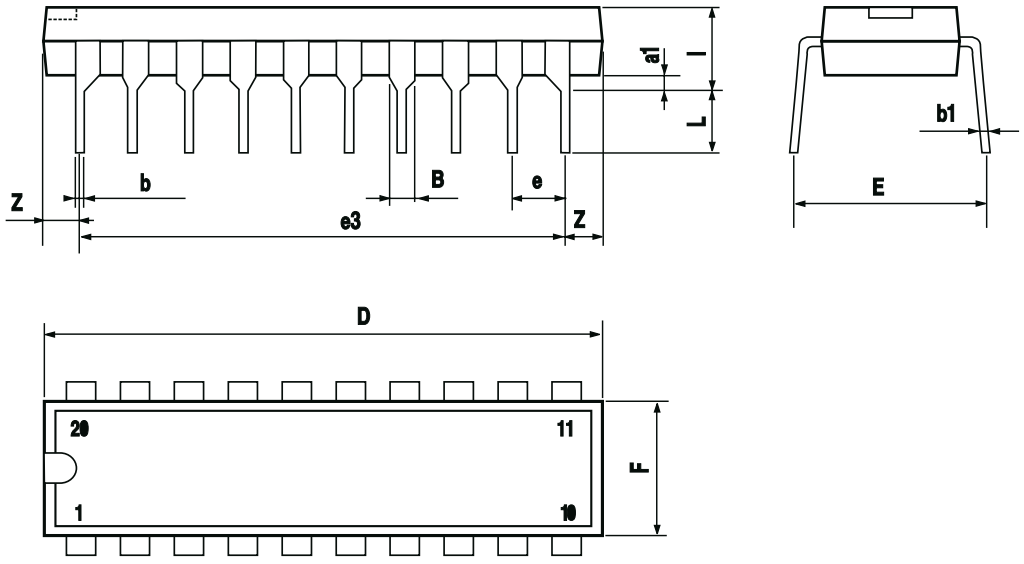


Table 8. PowerDIP20 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
a1	0.51		
B	0.85		1.40
b		0.50	
b1	0.38		0.50
D			24.80
E		8.80	
e		2.54	
e3		22.86	
F			7.10
I			5.10
L		3.30	
Z			1.27

Figure 17. PowerDIP20 mechanical drawing



9 Revision history

Table 9. Document revision history

Date	Revision	Changes
01-Aug-2003	9	
15-Nov-2011	10	Updated Features in coverpage and *Table 4*

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