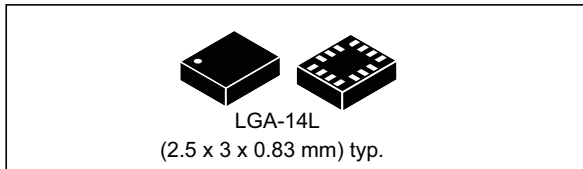


## iNEMO inertial module: always-on 3D accelerometer and 3D gyroscope

Datasheet - production data



### Features

- Power consumption: 0.9 mA in combo normal mode and 1.25 mA in combo high-performance mode up to 1.6 kHz.
- “Always-on” experience with low power consumption for both accelerometer and gyroscope
- Smart FIFO up to 8 kbyte based on features set
- Compliant with Android K and L
- Hard, soft ironing for external magnetic sensor corrections
- $\pm 2/\pm 4/\pm 8/\pm 16$  g full scale
- $\pm 125/\pm 245/\pm 500/\pm 1000/\pm 2000$  dps full scale
- Analog supply voltage: 1.71 V to 3.6 V
- Independent IOs supply (1.62 V)
- Compact footprint, 2.5 mm x 3 mm x 0.83 mm
- SPI/I<sup>2</sup>C serial interface with main processor data synchronization feature
- Embedded temperature sensor
- ECOPACK<sup>®</sup>, RoHS and “Green” compliant

### Applications

- Pedometer, step detector and step counter
- Significant motion and tilt functions
- Indoor navigation
- Tap and double-tap detection
- IoT and connected devices
- Intelligent power saving for handheld devices
- Vibration monitoring and compensation
- Free-fall detection
- 6D orientation detection

### Description

The LSM6DS3 is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope performing at 1.25 mA (up to 1.6 kHz ODR) in high-performance mode and enabling always-on low-power features for an optimal motion experience for the consumer.

The LSM6DS3 supports main OS requirements, offering real, virtual and batch sensors with 8 kbyte for dynamic data batching.

ST’s family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LSM6DS3 has a full-scale acceleration range of  $\pm 2/\pm 4/\pm 8/\pm 16$  g and an angular rate range of  $\pm 125/\pm 245/\pm 500/\pm 1000/\pm 2000$  dps.

High robustness to mechanical shock makes the LSM6DS3 the preferred choice of system designers for the creation and manufacturing of reliable products.

The LSM6DS3 is available in a plastic land grid array (LGA) package.

Table 1. Device summary

| Part number | Temperature range [°C] | Package                        | Packing     |
|-------------|------------------------|--------------------------------|-------------|
| LSM6DS3     | -40 to +85             | LGA-14L<br>(2.5 x 3 x 0.83 mm) | Tray        |
| LSM6DS3TR   | -40 to +85             |                                | Tape & Reel |

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# 1 Overview

The LSM6DS3 is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope.

The integrated power-efficient modes are able to reduce the power consumption down to 1.25 mA in high-performance mode, combining always-on low-power features with superior sensing precision for an optimal motion experience for the consumer thanks to ultra-low noise performance for both the gyroscope and accelerometer.

The LSM6DS3 delivers best-in-class motion sensing that can detect orientation and gestures in order to empower application developers and consumers with features and capabilities that are more sophisticated than simply orienting their devices to portrait and landscape mode.

The event-detection interrupts enable efficient and reliable motion tracking and contextual awareness, implementing hardware recognition of free-fall events, 6D orientation, tap and double-tap sensing, activity or inactivity, and wakeup events.

The LSM6DS3 supports main OS requirements, offering real, virtual and batch mode sensors. In addition, the LSM6DS3 can efficiently run the sensor-related features specified in Android, saving power and enabling faster reaction time. In particular, the LSM6DS3 has been designed to implement hardware features such as significant motion, tilt, pedometer functions, timestamping and to support the data acquisition of an external magnetometer with ironing correction (hard, soft).

The LSM6DS3 offers hardware flexibility to connect the pins with different mode connections to external sensors to expand functionalities such as adding a sensor hub, etc.

Up to 8 kbyte of FIFO with dynamic allocation of significant data (i.e. external sensors, timestamp, etc.) allows overall power saving of the system.

Like the entire portfolio of MEMS sensor modules, the LSM6DS3 leverages on the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LSM6DS3 is available in a small plastic land grid array (LGA) package of 2.5 x 3.0 x 0.83 mm to address ultra-compact solutions.

## 2 Embedded low-power features

The LSM6DS3 has been designed to be fully compliant with Android, featuring the following on-chip functions:

- 8 kbyte data buffering
  - 100% efficiency with flexible configurations and partitioning
  - possibility to store timestamp
- Event-detection interrupts (fully configurable):
  - free-fall
  - wakeup
  - 6D orientation
  - tap and double-tap sensing
  - activity / inactivity recognition
- Specific IP blocks with negligible power consumption and high-performance:
  - pedometer functions: step detector and step counters
  - tilt (Android compliant, refer to [Section 2.1: Tilt detection](#) for additional info)
  - significant motion (Android compliant)
- Sensor hub
  - up to 6 total sensors: 2 internal (accelerometer and gyroscope) and 4 external sensors
- Data rate synchronization with external trigger for reduced sensor access and enhanced fusion

### 2.1 Tilt detection

The tilt function helps to detect activity change and has been implemented in hardware using only the accelerometer to achieve both the targets of ultra-low power consumption and robustness during the short duration of dynamic accelerations.

It is based on a trigger of an event each time the device's tilt changes by an angle greater than 35 degrees from the start position.

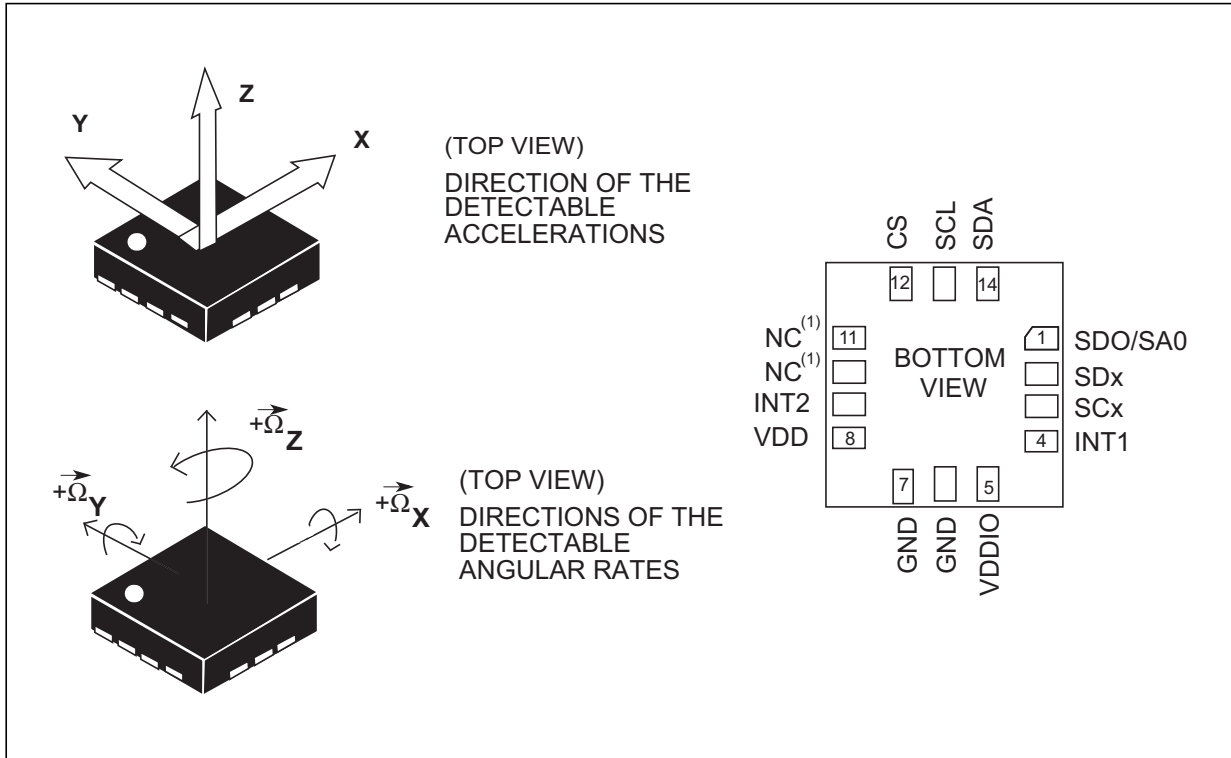
The tilt function can be used with different scenarios, for example:

- a) Trigger when phone is in a front pants pocket and the user goes from sitting to standing or standing to sitting;
- b) Doesn't trigger when phone is in a front pants pocket and the user is walking, running or going upstairs.



### 3 Pin description

Figure 1. Pin connections



1. Leave pin electrically unconnected and soldered to PCB.

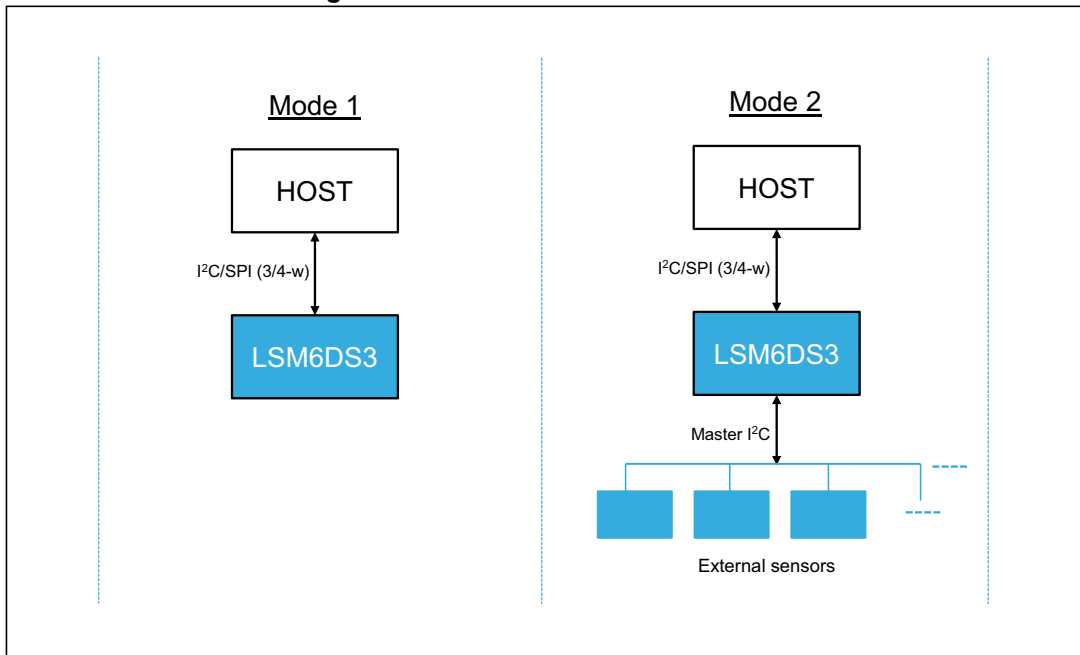
### 3.1 Pin connections

The LSM6DS3<sup>(a)</sup> offers the flexibility to connect the pins in order to have two different mode connections and functionalities. In detail:

- **Mode 1:** I<sup>2</sup>C slave interface or SPI (3- and 4-wire) serial interface is available;
- **Mode 2:** I<sup>2</sup>C slave interface or SPI (3- and 4-wire) serial interface and I<sup>2</sup>C interface master for external sensor connections are available;

In the following table each mode is described for the pin connection and function.

**Figure 2. LSM6DS3 connection modes**



a. The LSM6DS3H is recommended for optimal OIS/EIS performance.

**Table 2. Pin description**

| Pin# | Name                 | Mode 1 function  | Mode 2 function  |
|------|----------------------|--|--|
| 1    | SDO/SA0              | SPI 4-wire interface serial data output (SDO)<br>I <sup>2</sup> C least significant bit of the device address (SA0)                                    | SPI 4-wire interface serial data output (SDO)<br>I <sup>2</sup> C least significant bit of the device address (SA0)                                    |
| 2    | SDx                  | Connect to VDDIO or GND  | I <sup>2</sup> C serial data master (MSDA)   |
| 3    | SCx                  | Connect to VDDIO or GND  | I <sup>2</sup> C serial clock master (MSCL)  |
| 4    | INT1                 | Programmable interrupt 1   |  |
| 5    | VDDIO <sup>(1)</sup> | Power supply for I/O pins  |  |
| 6    | GND                  | 0 V supply   |  |
| 7    | GND                  | 0 V supply   |  |
| 8    | VDD <sup>(2)</sup>   | Power supply   |  |
| 9    | INT2                 | Programmable interrupt 2 (INT2)/ Data enable (DEN)   | Programmable interrupt 2 (INT2)/ Data enable (DEN)/<br>I <sup>2</sup> C master external synchronization signal (MDRDY)                                 |
| 10   | NC <sup>(3)</sup>    | Leave unconnected  |  |
| 11   | NC <sup>(3)</sup>    | Leave unconnected  |  |
| 12   | CS                   | I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled) | I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled) |
| 13   | SCL                  | I <sup>2</sup> C serial clock (SCL)<br>SPI serial port clock (SPC)   | I <sup>2</sup> C serial clock (SCL)<br>SPI serial port clock (SPC)   |
| 14   | SDA                  | I <sup>2</sup> C serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO)   | I <sup>2</sup> C serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO)   |

1. Recommended 100 nF filter capacitor.
2. Recommended 100 nF capacitor.
3. Leave pin electrically unconnected and soldered to PCB.

## 4 Module specifications

### 4.1 Mechanical characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

**Table 3. Mechanical characteristics**

| Symbol   | Parameter  | Test conditions                       | Min. | Typ. <sup>(1)</sup> | Max. | Unit     |
|----------|--|---------------------------------------|------|---------------------|------|----------|
| LA_FS    | Linear acceleration measurement range                                      |                                       |      | ±2                  |      | g        |
|          |  |                                       |      | ±4                  |      |          |
|          |  |                                       |      | ±8                  |      |          |
|          |  |                                       |      | ±16                 |      |          |
| G_FS     | Angular rate measurement range   |                                       |      | ±125                |      | dps      |
|          |  |                                       |      | ±245                |      |          |
|          |  |                                       |      | ±500                |      |          |
|          |  |                                       |      | ±1000               |      |          |
|          |  |                                       |      | ±2000               |      |          |
| LA_So    | Linear acceleration sensitivity  | FS = ±2                               |      | 0.061               |      | mg/LSB   |
|          |  | FS = ±4                               |      | 0.122               |      |          |
|          |  | FS = ±8                               |      | 0.244               |      |          |
|          |  | FS = ±16                              |      | 0.488               |      |          |
| G_So     | Angular rate sensitivity   | FS = ±125                             |      | 4.375               |      | mdps/LSB |
|          |  | FS = ±245                             |      | 8.75                |      |          |
|          |  | FS = ±500                             |      | 17.50               |      |          |
|          |  | FS = ±1000                            |      | 35                  |      |          |
|          |  | FS = ±2000                            |      | 70                  |      |          |
| LA_SoDr  | Linear acceleration sensitivity change vs. temperature <sup>(2)</sup>      | from -40° to +85°<br>delta from T=25° |      | ±1                  |      | %        |
| G_SoDr   | Angular rate sensitivity change vs. temperature <sup>(2)</sup>             | from -40° to +85°<br>delta from T=25° |      | ±1.5                |      | %        |
| LA_TyOff | Linear acceleration typical zero-g level offset accuracy <sup>(3)</sup>    |                                       |      | ±40                 |      | mg       |
| G_TyOff  | Angular rate typical zero-rate level <sup>(3)</sup>                        |                                       |      | ±10                 |      | dps      |
| LA_OffDr | Linear acceleration zero-g level change vs. temperature <sup>(2)</sup>     |                                       |      | ±0.5                |      | mg/°C    |
| G_OffDr  | Angular rate typical zero-rate level change vs. temperature <sup>(2)</sup> |                                       |      | ±0.05               |      | dps/°C   |

**Table 3. Mechanical characteristics (continued)**

| Symbol | Parameter  | Test conditions | Min. | Typ. <sup>(1)</sup> | Max. | Unit     |
|--------|--|-----------------|------|---------------------|------|----------|
| Rn     | Rate noise density in high-performance mode <sup>(4)</sup>         |                 |      | 7                   |      | mdps/√Hz |
| RnRMS  | Gyroscope RMS noise in low-power mode <sup>(5)</sup>               |                 |      | 140                 |      | mdps     |
| An     | Acceleration noise density in high-performance mode <sup>(6)</sup> | FS= ±2 g        |      | 90                  |      | μg/√Hz   |
|        |  | FS= ±4 g        |      | 90                  |      | μg/√Hz   |
|        |  | FS= ±8 g        |      | 110                 |      | μg/√Hz   |
|        |  | FS= ±16 g       |      | 180                 |      | μg/√Hz   |
| RMS    | Acceleration RMS noise in normal/low-power mode <sup>(7)</sup>     | FS= ±2 g        |      | 1.7                 |      | mg(RMS)  |
|        |  | FS= ±4 g        |      | 2.0                 |      | mg(RMS)  |
|        |  | FS= ±8 g        |      | 2.7                 |      | mg(RMS)  |
|        |  | FS= ±16 g       |      | 4.4                 |      | mg(RMS)  |
| LA_ODR | Linear acceleration output data rate                               |                 |      | 12.5                |      | Hz       |
|        |  |                 |      | 26                  |      |          |
|        |  |                 |      | 52                  |      |          |
|        |  |                 |      | 104                 |      |          |
|        |  |                 |      | 208                 |      |          |
|        |  |                 |      | 416                 |      |          |
|        |  |                 |      | 833                 |      |          |
|        |  |                 |      | 1666                |      |          |
| G_ODR  | Angular rate output data rate                                      |                 |      | 12.5                |      |          |
|        |  |                 |      | 26                  |      |          |
|        |  |                 |      | 52                  |      |          |
|        |  |                 |      | 104                 |      |          |
|        |  |                 |      | 208                 |      |          |
|        |  |                 |      | 416                 |      |          |
|        |  |                 |      | 833                 |      |          |
|        |  |                 |      | 1666                |      |          |
| Vst    | Linear acceleration self-test output change <sup>(8)(9)</sup>      | FS = 2 g        | 90   |                     | 1700 | mg       |
|        | Angular rate self-test output change <sup>(10)(11)</sup>           | FS = 2000 dps   | 150  |                     | 700  | dps      |
| Top    | Operating temperature range  |                 | -40  |                     | +85  | °C       |

1. Typical specifications are not guaranteed.
2. Measurements are performed in a uniform temperature setup.
3. Values after soldering.
4. RND (rate noise density) mode is independent of the ODR and FS setting.
5. Gyro noise RMS is independent of the ODR and FS setting.
6. Noise density in HP mode is the same for all ODRs.



7. Noise RMS in Normal/LP mode is the same for all the ODR RMS related to  $BW = ODR / 2$  (for ODR /9, typ value can be calculated by  $Typ * 0.6$ )
8. The sign of the linear acceleration self-test output change is defined by the STx\_XL bits in [CTRL5\\_C \(14h\)](#), [Table 60](#) for all axes.
9. The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of:  $OUTPUT[LSb] \text{ (self-test enabled)} - OUTPUT[LSb] \text{ (self-test disabled)}$ . 1LSb = 0.061 mg at  $\pm 2 g$  full scale.
10. The sign of the angular rate self-test output change is defined by the STx\_G bits in [CTRL5\\_C \(14h\)](#), [Table 59](#) for all axes.
11. The angular rate self-test output change is defined with the device in stationary condition as the absolute value of:  $OUTPUT[LSb] \text{ (self-test enabled)} - OUTPUT[LSb] \text{ (self-test disabled)}$ . 1LSb = 70 mdps at  $\pm 2000$  dps full scale.

## 4.2 Electrical characteristics

@ V<sub>dd</sub> = 1.8 V, T = 25 °C unless otherwise noted.

**Table 4. Electrical characteristics**

| Symbol               | Parameter  | Test conditions                       | Min.                     | Typ. <sup>(1)</sup> | Max.                     | Unit |
|----------------------|--|---------------------------------------|--------------------------|---------------------|--------------------------|------|
| V <sub>dd</sub>      | Supply voltage   |                                       | 1.71                     | 1.8                 | 3.6                      | V    |
| V <sub>dd_IO</sub>   | Power supply for I/O                                       |                                       | 1.62                     |                     | V <sub>dd</sub> + 0.1    | V    |
| I <sub>ddHP</sub>    | Gyroscope and accelerometer in high-performance mode       | up to ODR = 1.6 kHz                   |                          | 1.25                |                          | mA   |
| I <sub>ddNM</sub>    | Gyroscope and accelerometer in normal mode                 | ODR = 208 Hz                          |                          | 0.9                 |                          | mA   |
| I <sub>ddLP</sub>    | Gyroscope and accelerometer in low-power mode              | ODR = 12.5 Hz                         |                          | 0.42                |                          | mA   |
| LA_I <sub>ddHP</sub> | Accelerometer current consumption in high-performance mode | up to ODR = 1.6 kHz                   |                          | 240                 |                          | μA   |
| LA_I <sub>ddNM</sub> | Accelerometer current consumption in normal mode           | ODR = 104 Hz                          |                          | 70                  |                          | μA   |
| LA_I <sub>ddLM</sub> | Accelerometer current consumption in low-power mode        | ODR = 12.5 Hz                         |                          | 24                  |                          | μA   |
| I <sub>ddPD</sub>    | Gyroscope and accelerometer in power down                  |                                       |                          | 6                   |                          | μA   |
| V <sub>IH</sub>      | Digital high-level input voltage                           |                                       | 0.8 * V <sub>DD_IO</sub> |                     |                          | V    |
| V <sub>IL</sub>      | Digital low-level input voltage                            |                                       |                          |                     | 0.2 * V <sub>DD_IO</sub> | V    |
| V <sub>OH</sub>      | High-level output voltage                                  | I <sub>OH</sub> = 4 mA <sup>(2)</sup> | V <sub>DD_IO</sub> - 0.2 |                     |                          | V    |
| V <sub>OL</sub>      | Low-level output voltage                                   | I <sub>OL</sub> = 4 mA <sup>(2)</sup> |                          |                     | 0.2                      | V    |
| Top                  | Operating temperature range                                |                                       | -40                      |                     | +85                      | °C   |

1. Typical specifications are not guaranteed.
2. 4 mA is the maximum driving capability, i.e. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V<sub>OH</sub> and V<sub>OL</sub>.

For details related to the LSM6DS3 operating modes, refer to [5.2: Gyroscope power modes](#) and [5.3: Accelerometer power modes](#).

## 4.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

**Table 5. Temperature sensor characteristics**

| Symbol    | Parameter                                     | Test condition | Min. | Typ. <sup>(1)</sup> | Max. | Unit   |
|-----------|---|----------------|------|---------------------|------|--------|
| TODR      | Temperature refresh rate                      |                |      | 52                  |      | Hz     |
| Toff      | Temperature offset <sup>(2)</sup>             |                | -15  |                     | +15  | °C     |
| TSen      | Temperature sensitivity                       |                |      | 16                  |      | LSB/°C |
| TST       | Temperature stabilization time <sup>(3)</sup> |                |      |                     | 500  | µs     |
| T_ADC_res | Temperature ADC resolution                    |                |      | 12                  |      | bit    |
| Top       | Operating temperature range                   |                | -40  |                     | +85  | °C     |

1. Typical specifications are not guaranteed.
2. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
3. Time from power ON bit to valid data based on characterization data.



## 4.4 Communication interface characteristics

### 4.4.1 SPI - serial peripheral interface

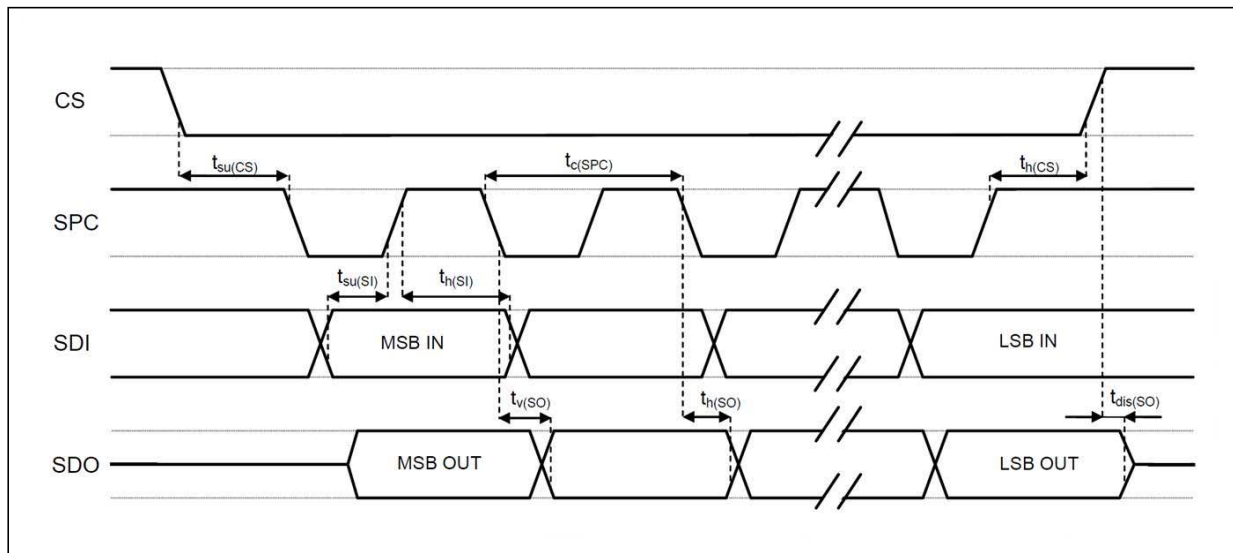
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

| Symbol        | Parameter               | Value <sup>(1)</sup> |     | Unit |
|---------------|-------------------------|----------------------|-----|------|
|               |                         | Min                  | Max |      |
| $t_{c(SPC)}$  | SPI clock cycle         | 100                  |     | ns   |
| $f_{c(SPC)}$  | SPI clock frequency     |                      | 10  | MHz  |
| $t_{su(CS)}$  | CS setup time           | 5                    |     | ns   |
| $t_{h(CS)}$   | CS hold time            | 20                   |     |      |
| $t_{su(SI)}$  | SDI input setup time    | 5                    |     |      |
| $t_{h(SI)}$   | SDI input hold time     | 15                   |     |      |
| $t_{v(SO)}$   | SDO valid output time   |                      | 50  |      |
| $t_{h(SO)}$   | SDO output hold time    | 5                    |     |      |
| $t_{dis(SO)}$ | SDO output disable time |                      | 50  |      |

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 3. SPI slave timing diagram



Note: Measurement points are done at  $0.2 \cdot V_{dd\_IO}$  and  $0.8 \cdot V_{dd\_IO}$ , for both input and output ports.

### 4.4.2 I<sup>2</sup>C - inter-IC control interface

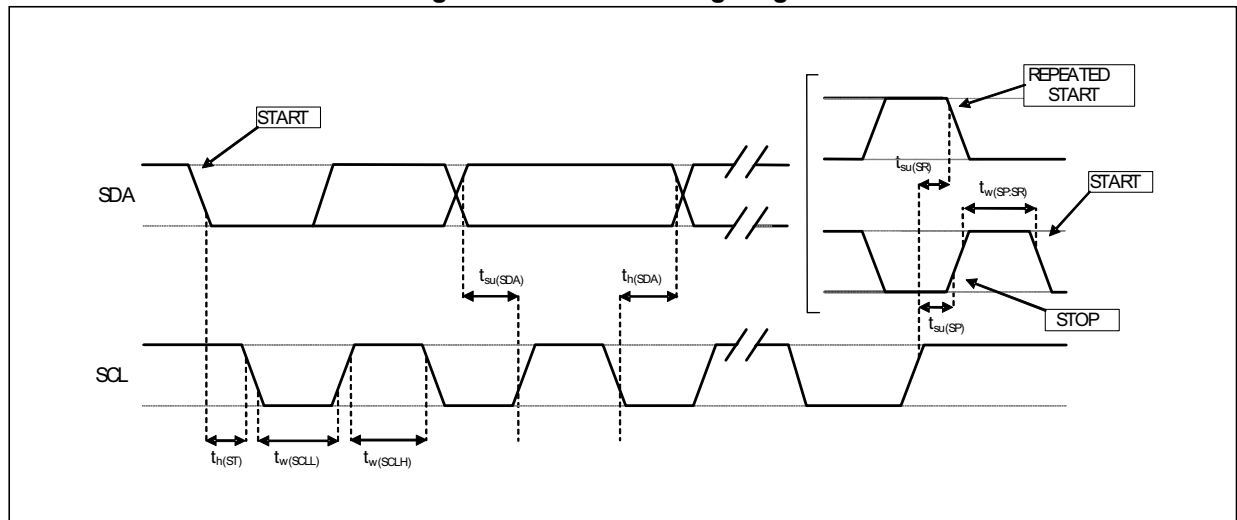
Subject to general operating conditions for Vdd and Top.

Table 7. I<sup>2</sup>C slave timing values

| Symbol                | Parameter                                      | I <sup>2</sup> C Standard mode <sup>(1)</sup> |      | I <sup>2</sup> C Fast mode <sup>(1)</sup> |     | Unit |
|-----------------------|--|---|------|---|-----|------|
|                       |  | Min   | Max  | Min                                       | Max |      |
| f <sub>(SCL)</sub>    | SCL clock frequency                            | 0   | 100  | 0   | 400 | kHz  |
| t <sub>w(SCLL)</sub>  | SCL clock low time                             | 4.7   |      | 1.3                                       |     | μs   |
| t <sub>w(SCLH)</sub>  | SCL clock high time                            | 4.0   |      | 0.6                                       |     |      |
| t <sub>su(SDA)</sub>  | SDA setup time                                 | 250   |      | 100                                       |     | ns   |
| t <sub>h(SDA)</sub>   | SDA data hold time                             | 0   | 3.45 | 0   | 0.9 | μs   |
| t <sub>h(ST)</sub>    | START condition hold time                      | 4   |      | 0.6                                       |     | μs   |
| t <sub>su(SR)</sub>   | Repeated START condition setup time            | 4.7   |      | 0.6                                       |     |      |
| t <sub>su(SP)</sub>   | STOP condition setup time                      | 4   |      | 0.6                                       |     |      |
| t <sub>w(SP:SR)</sub> | Bus free time between STOP and START condition | 4.7   |      | 1.3                                       |     |      |

1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.

Figure 4. I<sup>2</sup>C slave timing diagram



Note: Measurement points are done at 0.2·Vdd<sub>IO</sub> and 0.8·Vdd<sub>IO</sub>, for both ports.

## 4.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 8. Absolute maximum ratings**

| Symbol           | Ratings   | Maximum value      | Unit |
|------------------|---|--------------------|------|
| Vdd              | Supply voltage  | -0.3 to 4.8        | V    |
| T <sub>STG</sub> | Storage temperature range   | -40 to +125        | °C   |
| Sg               | Acceleration g for 0.2 ms   | 10,000             | g    |
| ESD              | Electrostatic discharge protection (HBM)  | 2                  | kV   |
| V <sub>in</sub>  | Input voltage on any control pin<br>(including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0) | 0.3 to Vdd_IO +0.3 | V    |

*Note:* Supply voltage on any pin should never exceed 4.8 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 4.6 Terminology

### 4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 g acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so,  $\pm 1$  g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

An angular rate gyroscope is device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

### 4.6.2 Zero-g and zero-rate level

Linear acceleration zero-g level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 g on both the X-axis and Y-axis, whereas the Z-axis will measure 1 g. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called zero-g offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-g level change vs. temperature" in [Table 3](#). The zero-g level tolerance (TyOff) describes the standard deviation of the range of zero-g levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

## 5 Functionality

### 5.1 Operating modes

The LSM6DS3 has three operating modes available:

- only accelerometer active and gyroscope in power-down
- only gyroscope active and accelerometer in power-down
- both accelerometer and gyroscope sensors active with independent ODR

The accelerometer is activated from power down by writing ODR\_XL[3:0] in [CTRL1\\_XL \(10h\)](#) while the gyroscope is activated from power-down by writing ODR\_G[3:0] in [CTRL2\\_G \(11h\)](#). For combo mode the ODRs are totally independent.

### 5.2 Gyroscope power modes

In the LSM6DS3, the gyroscope can be configured in four different operating modes: power-down, low-power, normal mode and high-performance mode. The operating mode selected depends on the value of the G\_HM\_MODE bit in [CTRL7\\_G \(16h\)](#). If G\_HM\_MODE is set to '0', high-performance mode is valid for all ODRs (from 12.5 Hz up to 1.6 kHz).

To enable the low-power and normal mode, the G\_HM\_MODE bit has to be set to '1'. Low-power mode is available for lower ODR (12.5, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

### 5.3 Accelerometer power modes

In the LSM6DS3, the accelerometer can be configured in four different operating modes: power-down, low-power, normal mode and high-performance mode. The operating mode selected depends on the value of the XL\_HM\_MODE bit in [CTRL6\\_C \(15h\)](#). If XL\_HM\_MODE is set to '0', high-performance mode is valid for all ODRs (from 12.5 Hz up to 6.66 kHz).

To enable the low-power and normal mode, the XL\_HM\_MODE bit has to be set to '1'. Low-power mode is available for lower ODRs (12.5, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

## 5.4 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

LSM6DS3 embeds 8 kbytes data FIFO to store the following data:

- gyroscope
- accelerometer
- external sensors
- step counter and timestamp
- temperature

Writing data in the FIFO can be configured to be triggered by the:

- accelerometer/gyroscope data-ready signal; in which case the ODR must be lower than or equal to both the accelerometer and gyroscope ODRs;
- sensor hub data-ready signal;
- step detection signal.

In addition, each data can be stored at a decimated data rate compared to FIFO ODR and it is configurable by the user, setting the registers *FIFO\_CTRL3 (08h)* and *FIFO\_CTRL4 (09h)*. The available decimation factors are 2, 3, 4, 8, 16, 32.

Programmable FIFO threshold can be set in *FIFO\_CTRL1 (06h)* and *FIFO\_CTRL2 (07h)* using the FTH [11:0] bits.

To monitor the FIFO status, dedicated registers (*FIFO\_STATUS1 (3Ah)*, *FIFO\_STATUS2 (3Bh)*, *FIFO\_STATUS3 (3Ch)*, *FIFO\_STATUS4 (3Dh)*) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO threshold status and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pads of these status events, the configuration can be set in *INT1\_CTRL (0Dh)* and *INT2\_CTRL (0Eh)*.

FIFO buffer can be configured according to five different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous mode

Each mode is selected by the FIFO\_MODE\_[2:0] in *FIFO\_CTRL5 (0Ah)* register. To guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

### 5.4.1 Bypass mode

In Bypass mode (*FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0] = 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

### 5.4.2 FIFO mode

In FIFO mode (*FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0] = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, Bypass mode should be selected by writing *FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0]) to '000'. After this reset command, it is possible to restart FIFO mode by writing *FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0]) to '001'.

FIFO buffer memorizes up to 4096 samples of 16 bits each but the depth of the FIFO can be resized by setting the FTH [11:0] bits in *FIFO\_CTRL1 (06h)* and *FIFO\_CTRL2 (07h)*. If the STOP\_ON\_FTH bit in *CTRL4\_C (13h)* is set to '1', FIFO depth is limited up to FTH [11:0] bits in *FIFO\_CTRL1 (06h)* and *FIFO\_CTRL2 (07h)*.

### 5.4.3 Continuous mode

Continuous mode (*FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag *FIFO\_STATUS2 (3Bh)*(FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO\_CTRL1 (06h)* and *FIFO\_CTRL2 (07h)*(FTH [11:0]).

It is possible to route *FIFO\_STATUS2 (3Bh)* (FTH) to the INT1 pin by writing in register *INT1\_CTRL (0Dh)* (INT1\_FTH) = '1' or to the INT2 pin by writing in register *INT2\_CTRL (0Eh)* (INT2\_FTH) = '1'.

A full-flag interrupt can be enabled, *INT1\_CTRL (0Dh)* (INT\_FULL\_FLAG) = '1', in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the OVER\_RUN flag in *FIFO\_STATUS2 (3Bh)* is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in *FIFO\_STATUS1 (3Ah)* and *FIFO\_STATUS2 (3Bh)* (DIFF\_FIFO[11:0]).

### 5.4.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (*FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0] = 011), FIFO behavior changes according to the trigger event detected in one of the following interrupt registers *FUNC\_SRC (53h)*, *TAP\_SRC (1Ch)*, *WAKE\_UP\_SRC (1Bh)* and *D6D\_SRC (1Dh)*.

When the selected trigger bit is equal to '1', FIFO operates in FIFO mode.

When the selected trigger bit is equal to '0', FIFO operates in Continuous mode.

### 5.4.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO\_CTRL5 (0Ah)* (*FIFO\_MODE\_[2:0] = '100'*), data measurement storage inside FIFO operates in Continuous mode when selected triggers in one of the following interrupt registers *FUNC\_SRC (53h)*, *TAP\_SRC (1Ch)*, *WAKE\_UP\_SRC (1Bh)* and *D6D\_SRC (1Dh)* are equal to '1', otherwise FIFO content is reset (Bypass mode).

### 5.4.6 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers (*FIFO\_DATA\_OUT\_L (3Eh)* and *FIFO\_DATA\_OUT\_H (3Fh)*) and each FIFO sample is composed of 16 bits.

All FIFO status registers (*FIFO\_STATUS1 (3Ah)*, *FIFO\_STATUS2 (3Bh)*, *FIFO\_STATUS3 (3Ch)*, *FIFO\_STATUS4 (3Dh)*) can be read at the start of a reading operation, minimizing the intervention of the application processor.

Saving data in the FIFO buffer is organized in four FIFO data sets consisting of 6 bytes each:

The 1<sup>st</sup> FIFO data set is reserved for gyroscope data;

The 2<sup>nd</sup> FIFO data set is reserved for accelerometer data;

The 3<sup>rd</sup> FIFO data set is reserved for the external sensor data stored in the registers from *SENSORHUB1\_REG (2Eh)* to *SENSORHUB6\_REG (33h)*;

The 4<sup>th</sup> FIFO data set can be alternately associated to the external sensor data stored in the registers from *SENSORHUB7\_REG (34h)* to *SENSORHUB12\_REG(39h)*, to the step counter and timestamp info, or to the temperature sensor data.

### 5.4.7 Filter block diagrams

Figure 5. Accelerometer chain

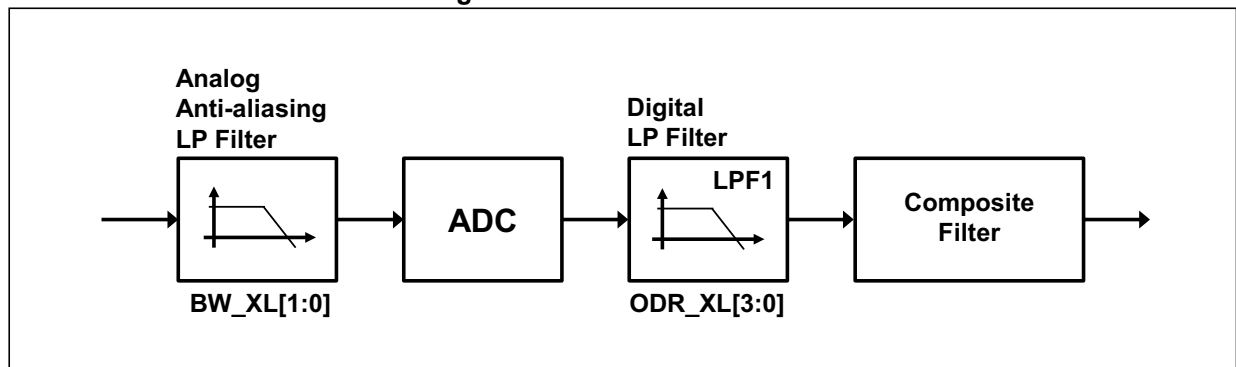




Figure 6. Accelerometer composite filter

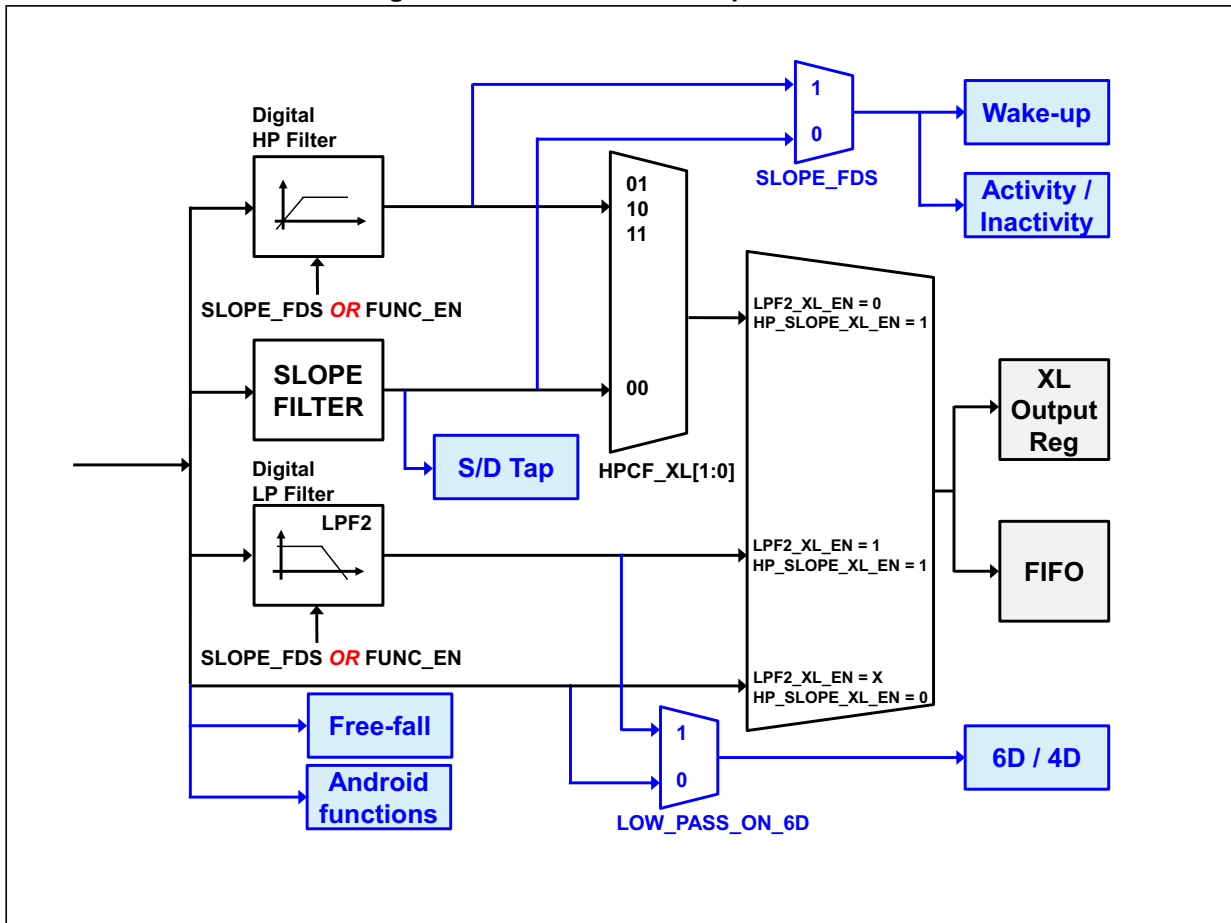
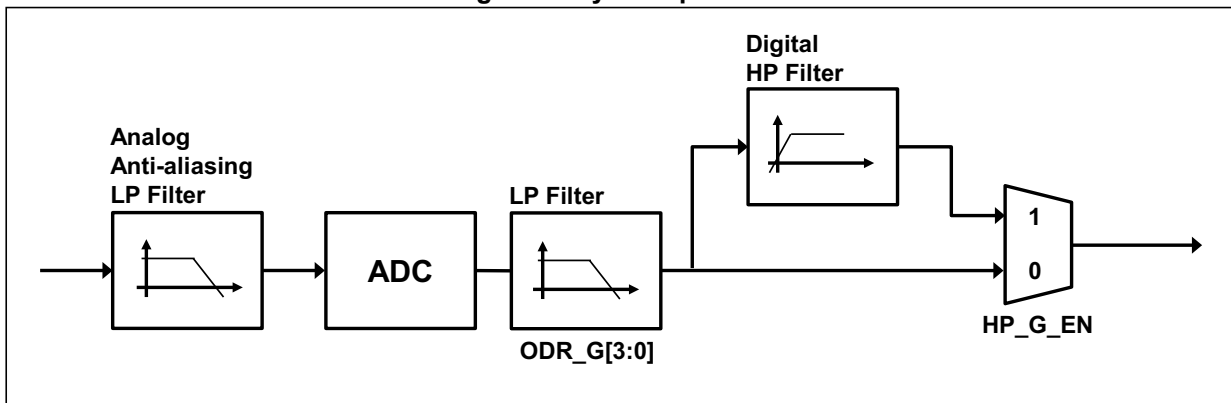


Figure 7. Gyroscope chain



## 6 Digital interfaces

The registers embedded inside the LSM6DS3 may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I<sup>2</sup>C interface, the CS line must be tied high (i.e connected to Vdd\_IO).

**Table 9. Serial interface pin description**

| Pin name    | Pin description   |
|-------------|---|
| CS          | SPI enable<br>I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled;<br>0: SPI communication mode / I <sup>2</sup> C disabled) |
| SCL/SPC     | I <sup>2</sup> C Serial Clock (SCL)<br>SPI Serial Port Clock (SPC)  |
| SDA/SDI/SDO | I <sup>2</sup> C Serial Data (SDA)<br>SPI Serial Data Input (SDI)<br>3-wire Interface Serial Data Output (SDO)  |
| SDO/SA0     | SPI Serial Data Output (SDO)<br>I <sup>2</sup> C less significant bit of the device address   |

### 6.1 I<sup>2</sup>C serial interface

The LSM6DS3 I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write the data to the registers, whose content can also be read back.

The relevant I<sup>2</sup>C terminology is provided in the table below.

**Table 10. I<sup>2</sup>C terminology**

| Term        | Description  |
|-------------|--|
| Transmitter | The device which sends data to the bus   |
| Receiver    | The device which receives data from the bus  |
| Master      | The device which initiates a transfer, generates clock signals and terminates a transfer |
| Slave       | The device addressed by the master   |

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the Serial DATA line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd\_IO through external pull-up resistors. When the bus is free, both the lines are high.

The I<sup>2</sup>C interface is implemented with fast mode (400 kHz) I<sup>2</sup>C standards as well as with the standard mode.

In order to disable the I<sup>2</sup>C block, (I2C\_disable) = 1 must be written in [CTRL4\\_C \(13h\)](#).

### 6.1.1 I<sup>2</sup>C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave Address (SAD) associated to the LSM6DS3 is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is '1' (address 1101011b); else if the SDO/SA0 pin is connected to ground, the LSb value is '0' (address 1101010b). This solution permits to connect and address two different inertial modules to the same I<sup>2</sup>C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I<sup>2</sup>C embedded inside the LSM6DS3 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The increment of the address is configured by the *CTRL3\_C (12h)* (IF\_INC).

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 11* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

**Table 11. SAD+Read/Write patterns**

| Command | SAD[6:1] | SAD[0] = SA0 | R/W | SAD+R/W        |
|---------|----------|--------------|-----|----------------|
| Read    | 110101   | 0            | 1   | 11010101 (D5h) |
| Write   | 110101   | 0            | 0   | 11010100 (D4h) |
| Read    | 110101   | 1            | 1   | 11010111 (D7h) |
| Write   | 110101   | 1            | 0   | 11010110 (D6h) |

**Table 12. Transfer when master is writing one byte to slave**

|        |    |         |     |     |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |    |

**Table 13. Transfer when master is writing multiple bytes to slave**

|        |    |         |     |     |     |      |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |      | SAK |    |

**Table 14. Transfer when master is receiving (reading) one byte of data from slave**

|        |    |         |     |     |     |    |         |     |      |      |    |
|--------|----|---------|-----|-----|-----|----|---------|-----|------|------|----|
| Master | ST | SAD + W |     | SUB |     | SR | SAD + R |     |      | NMAK | SP |
| Slave  |    |         | SAK |     | SAK |    |         | SAK | DATA |      |    |

**Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave**

|        |    |       |     |     |     |    |       |     |      |     |      |     |      |      |    |
|--------|----|-------|-----|-----|-----|----|-------|-----|------|-----|------|-----|------|------|----|
| Master | ST | SAD+W |     | SUB |     | SR | SAD+R |     |      | MAK |      | MAK |      | NMAK | SP |
| Slave  |    |       | SAK |     | SAK |    |       | SAK | DATA |     | DATA |     | DATA |      |    |

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

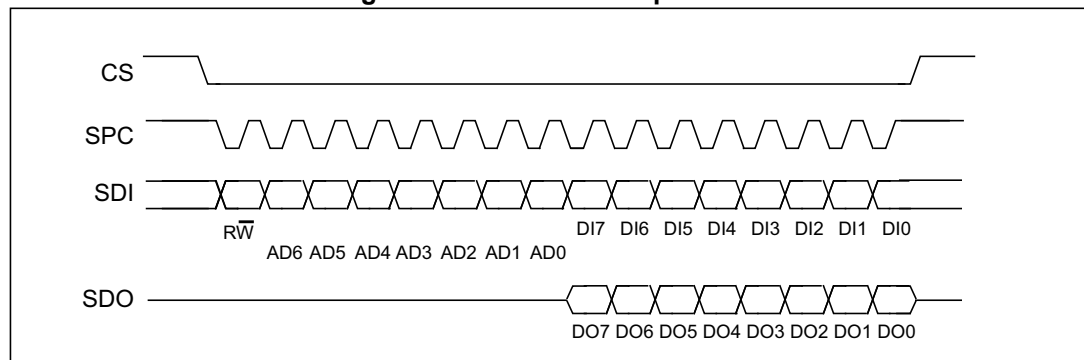
In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

## 6.2 SPI bus interface

The LSM6DS3 SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface communicates to the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

**Figure 8. Read and write protocol**



**CS** is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

**bit 0:**  $\overline{RW}$  bit. When 0, the data  $DI(7:0)$  is written into the device. When 1, the data  $DO(7:0)$  from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

**bit 1-7:** address  $AD(6:0)$ . This is the address field of the indexed register.

**bit 8-15:** data  $DI(7:0)$  (write mode). This is the data that is written into the device (MSb first).

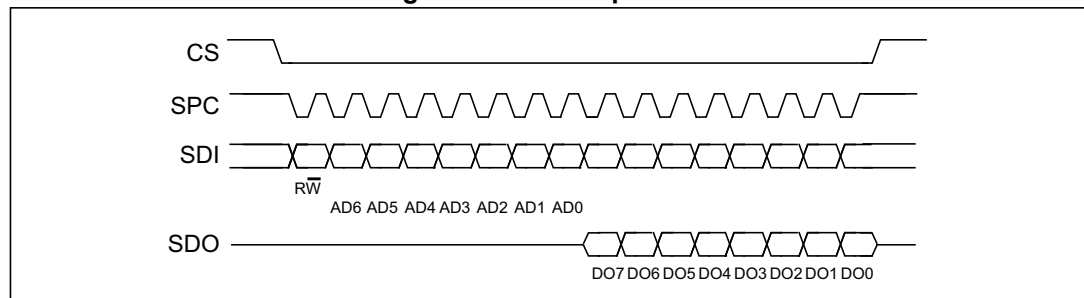
**bit 8-15:** data  $DO(7:0)$  (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the **CTRL3\_C (12h)** (**IF\_INC**) bit is '0', the address used to read/write data remains the same for every block. When the **CTRL3\_C (12h)** (**IF\_INC**) bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

### 6.2.1 SPI read

Figure 9. SPI read protocol



The SPI Read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

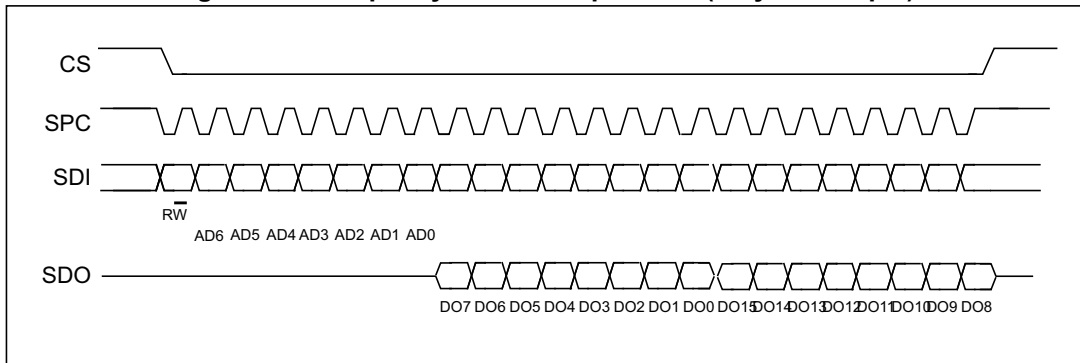
**bit 0:** READ bit. The value is 1.

**bit 1-7:** address  $AD(6:0)$ . This is the address field of the indexed register.

**bit 8-15:** data  $DO(7:0)$  (read mode). This is the data that will be read from the device (MSb first).

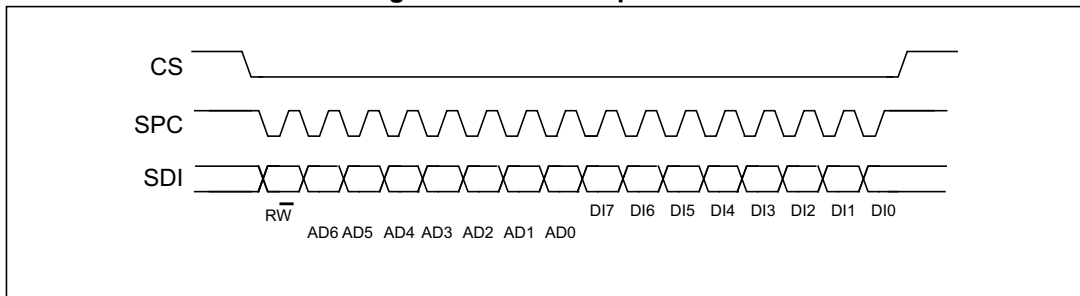
**bit 16-...:** data  $DO(...-8)$ . Further data in multiple byte reads.

Figure 10. Multiple byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 11. SPI write protocol



The SPI Write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

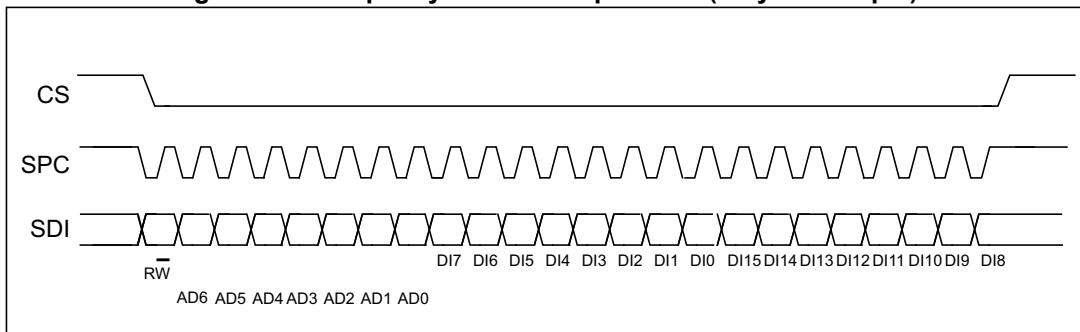
**bit 0:** WRITE bit. The value is 0.

**bit 1 -7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writes.

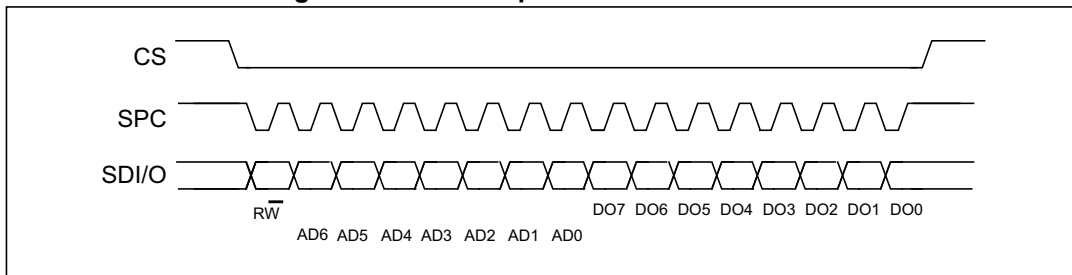
Figure 12. Multiple byte SPI write protocol (2-byte example)



### 6.2.3 SPI read in 3-wire mode

A 3-wire mode is entered by setting the *CTRL3\_C (12h)* (SIM) bit equal to '1' (SPI serial interface mode selection).

**Figure 13. SPI read protocol in 3-wire mode**



The SPI read command is performed with 16 clock pulses:

**bit 0:** READ bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

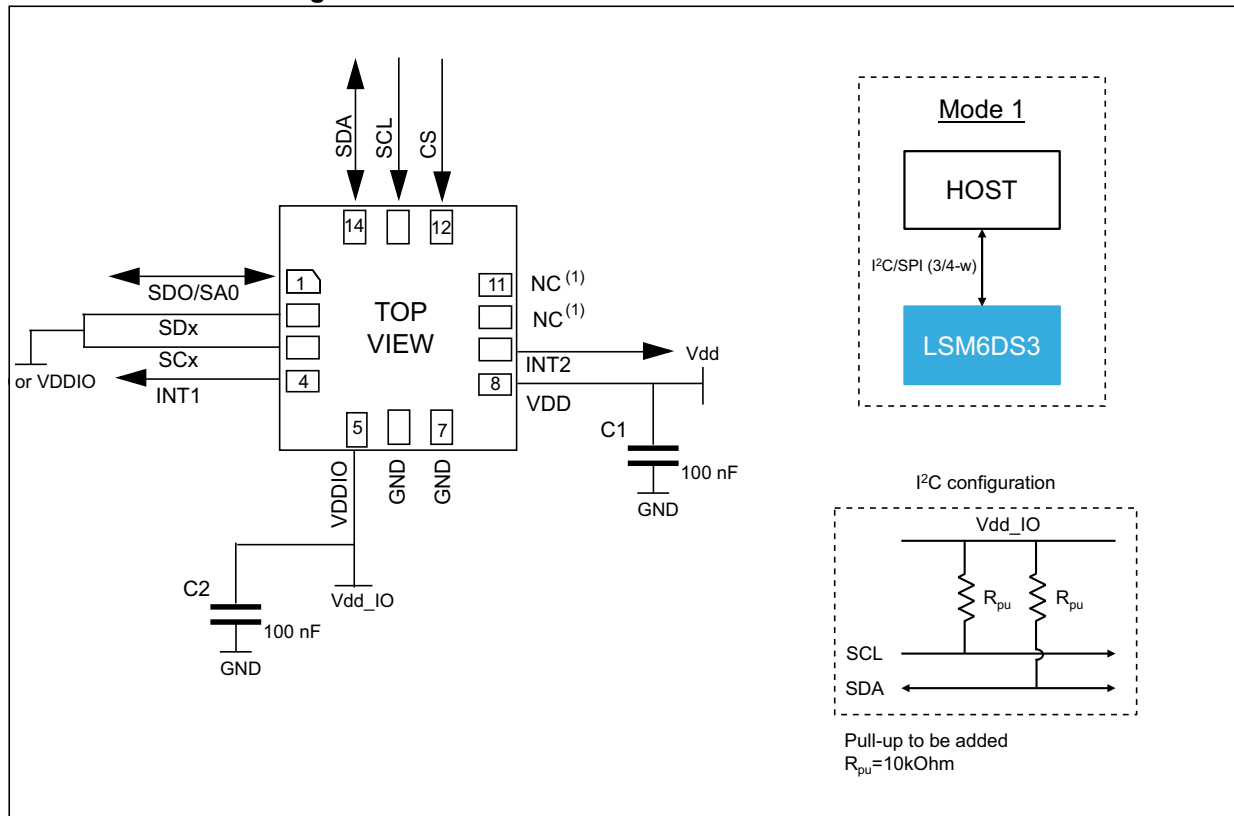
**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

## 7 Application hints

### 7.1 LSM6DS3 electrical connections in Mode 1

Figure 14. LSM6DS3 electrical connections in Mode 1



1. Leave pin electrically unconnected and soldered to PCB.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

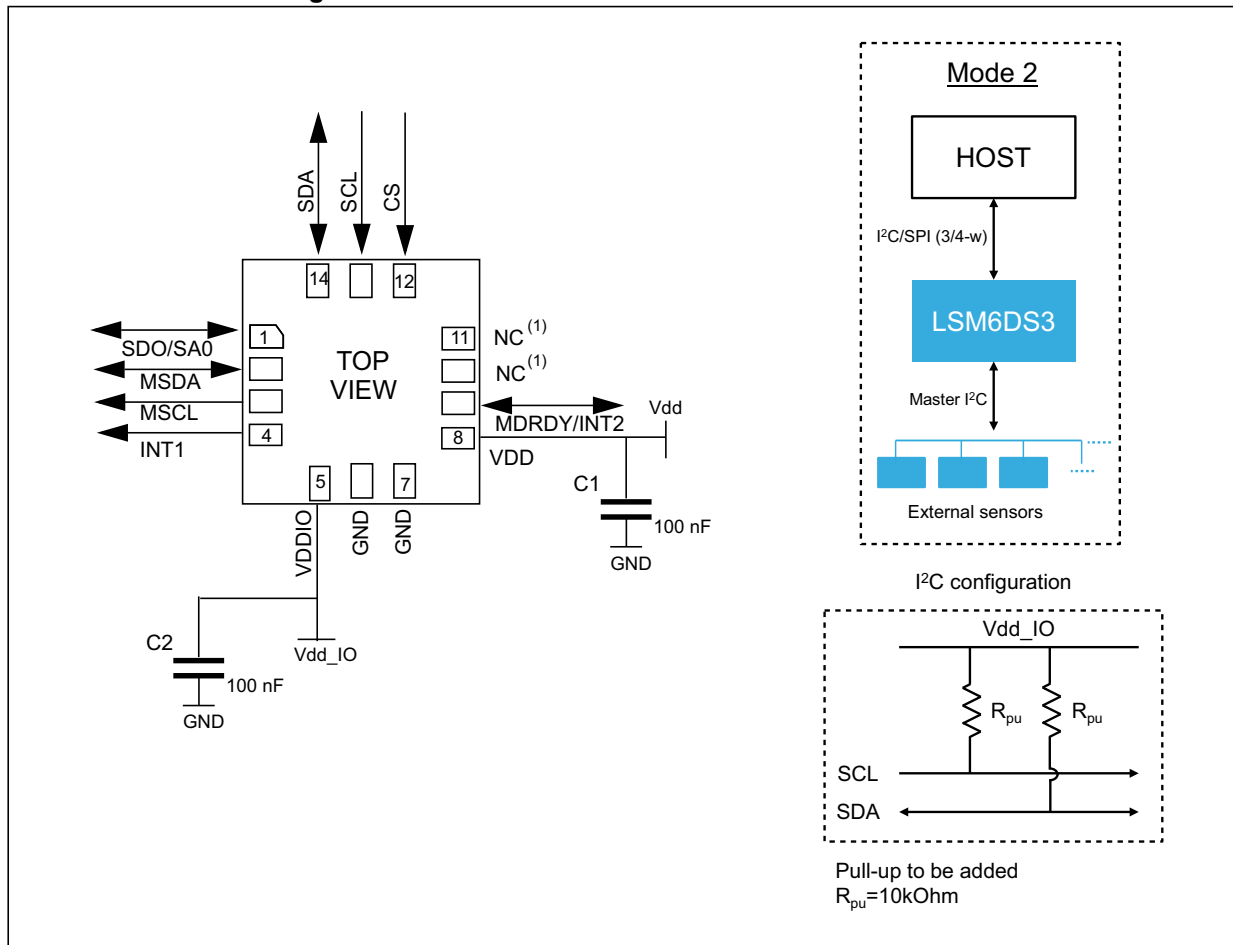
The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I<sup>2</sup>C interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I<sup>2</sup>C interface.



## 7.2 LSM6DS3 electrical connections in Mode 2

Figure 15. LSM6DS3 electrical connections in Mode 2



1. Leave pin electrically unconnected and soldered to PCB.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I<sup>2</sup>C interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I<sup>2</sup>C interface.

## 8 Register mapping

The table given below provides a list of the 8/16 bit registers embedded in the device and the corresponding addresses.

**Table 16. Registers address map**

| Name                   | Type | Register address |           | Default  | Comment                                       |
|------------------------|------|------------------|-----------|----------|---|
|                        |      | Hex              | Binary    |          |   |
| RESERVED               | -    | 00               | 00000000  | -        | Reserved                                      |
| FUNC_CFG_ACCESS        | r/w  | 01               | 00000001  | 00000000 | Embedded functions configuration register     |
| RESERVED               | -    | 02               | 00000010  | -        | Reserved                                      |
| RESERVED               | -    | 03               | 00000011  | -        | Reserved                                      |
| SENSOR_SYNC_TIME_FRAME | r/w  | 04               | 00000100  | 00000000 | Sensor sync configuration register            |
| RESERVED               | -    | 05               | 00000101  | -        | Reserved                                      |
| FIFO_CTRL1             | r/w  | 06               | 00000110  | 00000000 | FIFO configuration registers                  |
| FIFO_CTRL2             | r/w  | 07               | 00000111  | 00000000 |   |
| FIFO_CTRL3             | r/w  | 08               | 00001000  | 00000000 |   |
| FIFO_CTRL4             | r/w  | 09               | 00001001  | 00000000 |   |
| FIFO_CTRL5             | r/w  | 0A               | 00001010  | 00000000 |   |
| ORIENT_CFG_G           | r/w  | 0B               | 00001011  | 00000000 |   |
| RESERVED               | -    | 0C               | 00001100  | -        | Reserved                                      |
| INT1_CTRL              | r/w  | 0D               | 00001101  | 00000000 | INT1 pin control                              |
| INT2_CTRL              | r/w  | 0E               | 00001110  | 00000000 | INT2 pin control                              |
| WHO_AM_I               | r    | 0F               | 00001111  | 01101001 | Who I am ID                                   |
| CTRL1_XL               | r/w  | 10               | 00010000  | 00000000 | Accelerometer and gyroscope control registers |
| CTRL2_G                | r/w  | 11               | 00010001  | 00000000 |   |
| CTRL3_C                | r/w  | 12               | 00010010  | 00000100 |   |
| CTRL4_C                | r/w  | 13               | 00010011  | 00000000 |   |
| CTRL5_C                | r/w  | 14               | 00010100  | 00000000 |   |
| CTRL6_C                | r/w  | 15               | 00010101  | 00000000 |   |
| CTRL7_G                | r/w  | 16               | 00010110  | 00000000 |   |
| CTRL8_XL               | r/w  | 17               | 0001 0111 | 00000000 |   |
| CTRL9_XL               | r/w  | 18               | 00011000  | 00111000 |   |
| CTRL10_C               | r/w  | 19               | 00011001  | 00111000 |   |

Table 16. Registers address map (continued)

| Name          | Type | Register address |          | Default  | Comment  |
|---------------|------|------------------|----------|----------|--|
|               |      | Hex              | Binary   |          |  |
| MASTER_CONFIG | r/w  | 1A               | 00011010 | 00000000 | I <sup>2</sup> C master configuration register |
| WAKE_UP_SRC   | r    | 1B               | 00011011 | output   | Interrupts registers                           |
| TAP_SRC       | r    | 1C               | 00011100 | output   |  |
| D6D_SRC       | r    | 1D               | 00011101 | output   |  |
| STATUS_REG    | r    | 1E               | 00011110 | output   | Status data register                           |
| RESERVED      | -    | 1F               | 00011111 | -        | Reserved                                       |
| OUT_TEMP_L    | r    | 20               | 00100000 | output   | Temperature output data register               |
| OUT_TEMP_H    | r    | 21               | 00100001 | output   |  |
| OUTX_L_G      | r    | 22               | 00100010 | output   | Gyroscope output register                      |
| OUTX_H_G      | r    | 23               | 00100011 | output   |  |
| OUTY_L_G      | r    | 24               | 00100100 | output   |  |
| OUTY_H_G      | r    | 25               | 00100101 | output   |  |
| OUTZ_L_G      | r    | 26               | 00100110 | output   |  |
| OUTZ_H_G      | r    | 27               | 00100111 | output   |  |
| OUTX_L_XL     | r    | 28               | 00101000 | output   | Accelerometer output register                  |
| OUTX_H_XL     | r    | 29               | 00101001 | output   |  |
| OUTY_L_XL     | r    | 2A               | 00101010 | output   |  |
| OUTY_H_XL     | r    | 2B               | 00101011 | output   |  |
| OUTZ_L_XL     | r    | 2C               | 00101100 | output   |  |
| OUTZ_H_XL     | r    | 2D               | 00101101 | output   |  |

Table 16. Registers address map (continued)

| Name             | Type | Register address |           | Default | Comment                          |
|------------------|------|------------------|-----------|---------|----------------------------------|
|                  |      | Hex              | Binary    |         |                                  |
| SENSORHUB1_REG   | r    | 2E               | 00101110  | output  | Sensor hub output registers      |
| SENSORHUB2_REG   | r    | 2F               | 00101111  | output  |                                  |
| SENSORHUB3_REG   | r    | 30               | 00110000  | output  |                                  |
| SENSORHUB4_REG   | r    | 31               | 00110001  | output  |                                  |
| SENSORHUB5_REG   | r    | 32               | 00110010  | output  |                                  |
| SENSORHUB6_REG   | r    | 33               | 00110011  | output  |                                  |
| SENSORHUB7_REG   | r    | 34               | 00110100  | output  |                                  |
| SENSORHUB8_REG   | r    | 35               | 00110101  | output  |                                  |
| SENSORHUB9_REG   | r    | 36               | 00110110  | output  |                                  |
| SENSORHUB10_REG  | r    | 37               | 00110111  | output  |                                  |
| SENSORHUB11_REG  | r    | 38               | 00111000  | output  |                                  |
| SENSORHUB12_REG  | r    | 39               | 00111001  | output  |                                  |
| FIFO_STATUS1     | r    | 3A               | 00111010  | output  | FIFO status registers            |
| FIFO_STATUS2     | r    | 3B               | 00111011  | output  |                                  |
| FIFO_STATUS3     | r    | 3C               | 00111100  | output  |                                  |
| FIFO_STATUS4     | r    | 3D               | 00111101  | output  |                                  |
| FIFO_DATA_OUT_L  | r    | 3E               | 00111110  | output  | FIFO data output registers       |
| FIFO_DATA_OUT_H  | r    | 3F               | 00111111  | output  |                                  |
| TIMESTAMP0_REG   | r    | 40               | 01000000  | output  | Timestamp output registers       |
| TIMESTAMP1_REG   | r    | 41               | 01000001  | output  |                                  |
| TIMESTAMP2_REG   | r/w  | 42               | 01000010  | output  |                                  |
| RESERVED         | -    | 43-48            |           | -       | Reserved                         |
| STEP_TIMESTAMP_L | r    | 49               | 0100 1001 | output  | Step counter timestamp registers |
| STEP_TIMESTAMP_H | r    | 4A               | 0100 1010 | output  |                                  |
| STEP_COUNTER_L   | r    | 4B               | 01001011  | output  | Step counter output registers    |
| STEP_COUNTER_H   | r    | 4C               | 01001100  | output  |                                  |
| SENSORHUB13_REG  | r    | 4D               | 01001101  | output  | Sensor hub output registers      |
| SENSORHUB14_REG  | r    | 4E               | 01001110  | output  |                                  |
| SENSORHUB15_REG  | r    | 4F               | 01001111  | output  |                                  |
| SENSORHUB16_REG  | r    | 50               | 01010000  | output  |                                  |
| SENSORHUB17_REG  | r    | 51               | 01010001  | output  |                                  |
| SENSORHUB18_REG  | r    | 52               | 01010010  | output  |                                  |
| FUNC_SRC         | r    | 53               | 01010011  | output  | Interrupt register               |

**Table 16. Registers address map (continued)**

| Name            | Type | Register address |           | Default  | Comment   |
|-----------------|------|------------------|-----------|----------|---|
|                 |      | Hex              | Binary    |          |   |
| RESERVED        | -    | 54-57            |           | -        | Reserved  |
| TAP_CFG         | r/w  | 58               | 01011000  | 00000000 | Interrupt registers                             |
| TAP_THS_6D      | r/w  | 59               | 01011001  | 00000000 |   |
| INT_DUR2        | r/w  | 5A               | 01011010  | 00000000 |   |
| WAKE_UP_THS     | r/w  | 5B               | 01011011  | 00000000 |   |
| WAKE_UP_DUR     | r/w  | 5C               | 01011100  | 00000000 |   |
| FREE_FALL       | r/w  | 5D               | 01011101  | 00000000 |   |
| MD1_CFG         | r/w  | 5E               | 01011110  | 00000000 |   |
| MD2_CFG         | r/w  | 5F               | 01011111  | 00000000 |   |
| RESERVED        | -    | 60-65            |           | -        | Reserved  |
| OUT_MAG_RAW_X_L | r    | 66               | 0110 0110 | output   | External magnetometer raw data output registers |
| OUT_MAG_RAW_X_H | r    | 67               | 0110 0111 | output   |   |
| OUT_MAG_RAW_Y_L | r    | 68               | 0110 1000 | output   |   |
| OUT_MAG_RAW_Y_H | r    | 69               | 0110 1001 | output   |   |
| OUT_MAG_RAW_Z_L | r    | 6A               | 0110 1010 | output   |   |
| OUT_MAG_RAW_Z_H | r    | 6B               | 0110 1011 | output   |   |

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

## 9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

### 9.1 FUNC\_CFG\_ACCESS (01h)

Enable embedded functions register (r/w).

**Table 17. FUNC\_CFG\_ACCESS register**

|             |                  |                  |                  |                  |                  |                  |                  |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| FUNC_CFG_EN | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 18. FUNC\_CFG\_ACCESS register description**

|             |   |
|-------------|---|
| FUNC_CFG_EN | Enable access to the embedded functions configuration registers <sup>(1)</sup> from address 02h to 32h. Default value: 0.<br>(0: disable access to embedded functions configuration registers;<br>1: enable access to embedded functions configuration registers) |
|-------------|---|

1. The embedded functions configuration registers details are available in [10: Embedded functions register mapping](#) and [11: Embedded functions registers description](#).

### 9.2 SENSOR\_SYNC\_TIME\_FRAME (04h)

Sensor synchronization time frame register (r/w).

**Table 19. SENSOR\_SYNC\_TIME\_FRAME register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TPH_7 | TPH_6 | TPH_5 | TPH_4 | TPH_3 | TPH_2 | TPH_1 | TPH_0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 20. SENSOR\_SYNC\_TIME\_FRAME register description**

|            |   |
|------------|---|
| TPH_ [7:0] | Sensor synchronization time frame with the step of 500 ms and full range of 5 s.<br>Unsigned 8-bit.<br>Default value: 0000 0000 |
|------------|---|

### 9.3 FIFO\_CTRL1 (06h)

FIFO control register (r/w).

**Table 21. FIFO\_CTRL1 register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| FTH_7 | FTH_6 | FTH_5 | FTH_4 | FTH_3 | FTH_2 | FTH_1 | FTH_0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 22. FIFO\_CTRL1 register description**

|            |   |
|------------|---|
| FTH_ [7:0] | FIFO threshold level setting <sup>(1)</sup> . Default value: 0000 0000.<br>Watermark flag rises when the number of bytes written to FIFO after the next write is greater than or equal to the threshold level.<br>Minimum resolution for the FIFO is 1 LSB = 2 bytes (1 word) in FIFO |
|------------|---|

1. For a complete watermark threshold configuration, consider FTH\_ [11:8] in [FIFO\\_CTRL2 \(07h\)](#).

### 9.4 FIFO\_CTRL2 (07h)

FIFO control register (r/w).

**Table 23. FIFO\_CTRL2 register**

|                    |                      |                  |                  |        |       |       |       |
|--------------------|----------------------|------------------|------------------|--------|-------|-------|-------|
| TIMER_PEDO_FIF0_EN | TIMER_PEDO_FIF0_DRDY | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | FTH_11 | FTH10 | FTH_9 | FTH_8 |
|--------------------|----------------------|------------------|------------------|--------|-------|-------|-------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 24. FIFO\_CTRL2 register description**

|                      |  |
|----------------------|--|
| TIMER_PEDO_FIF0_EN   | Enable pedometer step counter and timestamp as 4 <sup>th</sup> FIFO data set. Default: 0 (0: disable step counter and timestamp data as 4 <sup>th</sup> FIFO data set; 1: enable step counter and timestamp data as 4 <sup>th</sup> FIFO data set)                             |
| TIMER_PEDO_FIF0_DRDY | FIFO write mode <sup>(1)</sup> . Default: 0 (0: enable write in FIFO based on XL/Gyro data-ready; 1: enable write in FIFO at every step detected by step counter.)   |
| FTH_[11:8]           | FIFO threshold level setting <sup>(2)</sup> . Default value: 0000<br>Watermark flag rises when the number of bytes written to FIFO after the next write is greater than or equal to the threshold level.<br>Minimum resolution for the FIFO is 1LSB = 2 bytes (1 word) in FIFO |

1. This bit is effective if the DATA\_VALID\_SEL\_FIF0 bit of the *MASTER\_CONFIG (1Ah)* register is set to 0.
2. For a complete watermark threshold configuration, consider FTH\_[7:0] in *FIF0\_CTRL1 (06h)*

### 9.5 FIFO\_CTRL3 (08h)

FIFO control register (r/w).

**Table 25. FIFO\_CTRL3 register**

|                  |                  |                |                |                |              |              |              |
|------------------|------------------|----------------|----------------|----------------|--------------|--------------|--------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | DEC_FIF0_GYRO2 | DEC_FIF0_GYRO1 | DEC_FIF0_GYRO0 | DEC_FIF0_XL2 | DEC_FIF0_XL1 | DEC_FIF0_XL0 |
|------------------|------------------|----------------|----------------|----------------|--------------|--------------|--------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 26. FIFO\_CTRL3 register description**

|                     |   |
|---------------------|---|
| DEC_FIF0_GYRO [2:0] | Gyro FIFO (first data set) decimation setting. Default: 000<br>For the configuration setting, refer to <a href="#">Table 27</a> .           |
| DEC_FIF0_XL [2:0]   | Accelerometer FIFO (second data set) decimation setting. Default: 000<br>For the configuration setting, refer to <a href="#">Table 28</a> . |

**Table 27. Gyro FIFO decimation setting**

| DEC_FIFO_GYRO [2:0] | Configuration             |
|---------------------|---------------------------|
| 000                 | Gyro sensor not in FIFO   |
| 001                 | No decimation             |
| 010                 | Decimation with factor 2  |
| 011                 | Decimation with factor 3  |
| 100                 | Decimation with factor 4  |
| 101                 | Decimation with factor 8  |
| 110                 | Decimation with factor 16 |
| 111                 | Decimation with factor 32 |

**Table 28. Accelerometer FIFO decimation setting**

| DEC_FIFO_XL [2:0] | Configuration                    |
|-------------------|----------------------------------|
| 000               | Accelerometer sensor not in FIFO |
| 001               | No decimation                    |
| 010               | Decimation with factor 2         |
| 011               | Decimation with factor 3         |
| 100               | Decimation with factor 4         |
| 101               | Decimation with factor 8         |
| 110               | Decimation with factor 16        |
| 111               | Decimation with factor 32        |

## 9.6 FIFO\_CTRL4 (09h)

FIFO control register (r/w).

**Table 29. FIFO\_CTRL4 register**

|                  |                |               |               |               |               |               |               |
|------------------|----------------|---------------|---------------|---------------|---------------|---------------|---------------|
| 0 <sup>(1)</sup> | ONLY_HIGH_DATA | DEC_DS4_FIFO2 | DEC_DS4_FIFO1 | DEC_DS4_FIFO0 | DEC_DS3_FIFO2 | DEC_DS3_FIFO1 | DEC_DS3_FIFO0 |
|------------------|----------------|---------------|---------------|---------------|---------------|---------------|---------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 30. FIFO\_CTRL4 register description**

|                   |  |
|-------------------|--|
| ONLY_HIGH_DATA    | 8-bit data storage in FIFO. Default: 0<br>(0: disable MSByte only memorization in FIFO for XL and Gyro;<br>1: enable MSByte only memorization in FIFO for XL and Gyro in FIFO) |
| DEC_DS4_FIFO[2:0] | Fourth FIFO data set decimation setting. Default: 000<br>For the configuration setting, refer to <a href="#">Table 31</a> .  |
| DEC_DS3_FIFO[2:0] | Third FIFO data set decimation setting. Default: 000<br>For the configuration setting, refer to <a href="#">Table 32</a> .   |



**Table 31. Fourth FIFO data set decimation setting**

| DEC_DS4_FIFO[2:0] | Configuration                    |
|-------------------|----------------------------------|
| 000               | Fourth FIFO data set not in FIFO |
| 001               | No decimation                    |
| 010               | Decimation with factor 2         |
| 011               | Decimation with factor 3         |
| 100               | Decimation with factor 4         |
| 101               | Decimation with factor 8         |
| 110               | Decimation with factor 16        |
| 111               | Decimation with factor 32        |

**Table 32. Third FIFO data set decimation setting**

| DEC_DS3_FIFO[2:0] | Configuration                   |
|-------------------|---------------------------------|
| 000               | Third FIFO data set not in FIFO |
| 001               | No decimation                   |
| 010               | Decimation with factor 2        |
| 011               | Decimation with factor 3        |
| 100               | Decimation with factor 4        |
| 101               | Decimation with factor 8        |
| 110               | Decimation with factor 16       |
| 111               | Decimation with factor 32       |

## 9.7 FIFO\_CTRL5 (0Ah)

FIFO control register (r/w).

**Table 33. FIFO\_CTRL5 register**

|                  |            |            |            |            |             |             |             |
|------------------|------------|------------|------------|------------|-------------|-------------|-------------|
| 0 <sup>(1)</sup> | ODR_FIF0_3 | ODR_FIF0_2 | ODR_FIF0_1 | ODR_FIF0_0 | FIF0_MODE_2 | FIF0_MODE_1 | FIF0_MODE_0 |
|------------------|------------|------------|------------|------------|-------------|-------------|-------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 34. FIFO\_CTRL5 register description**

|                 |  |
|-----------------|--|
| ODR_FIF0_[3:0]  | FIFO ODR selection, setting FIF0_MODE also. Default: 0000<br>For the configuration setting, refer to <a href="#">Table 35</a>          |
| FIF0_MODE_[2:0] | FIFO mode selection bits, setting ODR_FIF0 also. Default value: 000<br>For the configuration setting refer to <a href="#">Table 36</a> |

Table 35. FIFO ODR selection

| ODR_FIFO_[3:0] | Configuration <sup>(1)</sup> |
|----------------|------------------------------|
| 0000           | FIFO disabled                |
| 0001           | FIFO ODR is set to 12.5 Hz   |
| 0010           | FIFO ODR is set to 26 Hz     |
| 0011           | FIFO ODR is set to 52 Hz     |
| 0100           | FIFO ODR is set to 104 Hz    |
| 0101           | FIFO ODR is set to 208 Hz    |
| 0110           | FIFO ODR is set to 416 Hz    |
| 0111           | FIFO ODR is set to 833 Hz    |
| 1000           | FIFO ODR is set to 1.66 kHz  |
| 1001           | FIFO ODR is set to 3.33 kHz  |
| 1010           | FIFO ODR is set to 6.66 kHz  |

1. If the device is working at an ODR slower than the one selected, FIFO ODR is limited to that ODR value. Moreover, these bits are effective if both the DATA\_VALID\_SEL FIFO bit of *MASTER\_CONFIG (1Ah)* and the TIMER\_PEDO\_FIFO\_DRDY bit of *FIFO\_CTRL2 (07h)* are set to 0.

Table 36. FIFO mode selection

| FIFO_MODE_[2:0] | Configuration mode   |
|-----------------|--|
| 000             | Bypass mode. FIFO disabled.  |
| 001             | FIFO mode. Stops collecting data when FIFO is full.                            |
| 010             | Reserved   |
| 011             | Continuous mode until trigger is deasserted, then FIFO mode.                   |
| 100             | Bypass mode until trigger is deasserted, then Continuous mode.                 |
| 101             | Reserved   |
| 110             | Continuous mode. If the FIFO is full, the new sample overwrites the older one. |
| 111             | Reserved   |

## 9.8 ORIENT\_CFG\_G (0Bh)

Angular rate sensor sign and orientation register (r/w).

Table 37. ORIENT\_CFG\_G register

|                  |                  |         |         |         |          |          |          |
|------------------|------------------|---------|---------|---------|----------|----------|----------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | SignX_G | SignY_G | SignZ_G | Orient_2 | Orient_1 | Orient_0 |
|------------------|------------------|---------|---------|---------|----------|----------|----------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 38. ORIENT\_CFG\_G register description**

|              |  |
|--------------|--|
| SignX_G      | Pitch axis (X) angular rate sign. Default value: 0<br>(0: positive sign; 1: negative sign)                                       |
| SignY_G      | Roll axis (Y) angular rate sign. Default value: 0<br>(0: positive sign; 1: negative sign)  |
| SignZ_G      | Yaw axis (Z) angular rate sign. Default value: 0<br>(0: positive sign; 1: negative sign)   |
| Orient [2:0] | Directional user-orientation selection. Default value: 000<br>For the configuration setting, refer to <a href="#">Table 39</a> . |

**Table 39. Settings for orientation of axes**

| Orient [2:0] | 000 | 001 | 010 | 011 | 100 | 101 |
|--------------|-----|-----|-----|-----|-----|-----|
| Pitch        | X   | X   | Y   | Y   | Z   | Z   |
| Roll         | Y   | Z   | X   | Z   | X   | Y   |
| Yaw          | Z   | Y   | Z   | X   | Y   | X   |

## 9.9 INT1\_CTRL (0Dh)

INT1 pad control register (r/w).

Each bit in this register enables a signal to be carried through INT1. The pad's output will supply the OR combination of the selected signals.

**Table 40. INT1\_CTRL register**

|                    |               |                |               |          |           |             |              |
|--------------------|---------------|----------------|---------------|----------|-----------|-------------|--------------|
| INT1_STEP_DETECTOR | INT1_SIGN_MOT | INT1_FULL_FLAG | INT1_FIFO_OVR | INT1_FTH | INT1_BOOT | INT1_DRDY_G | INT1_DRDY_XL |
|--------------------|---------------|----------------|---------------|----------|-----------|-------------|--------------|

**Table 41. INT1\_CTRL register description**

|                    |  |
|--------------------|--|
| INT1_STEP_DETECTOR | Pedometer step recognition interrupt enable on INT1 pad. Default value: 0<br>(0: disabled; 1: enabled) |
| INT1_SIGN_MOT      | Significant motion interrupt enable on INT1 pad. Default value: 0<br>(0: disabled; 1: enabled)         |
| INT1_FULL_FLAG     | FIFO full flag interrupt enable on INT1 pad. Default value: 0<br>(0: disabled; 1: enabled)             |
| INT1_FIFO_OVR      | FIFO overrun interrupt on INT1 pad. Default value: 0<br>(0: disabled; 1: enabled)                      |
| INT1_FTH           | FIFO threshold interrupt on INT1 pad. Default value: 0<br>(0: disabled; 1: enabled)                    |
| INT1_BOOT          | Boot status available on INT1 pad. Default value: 0<br>(0: disabled; 1: enabled)                       |
| INT1_DRDY_G        | Gyroscope Data Ready on INT1 pad. Default value: 0<br>(0: disabled; 1: enabled)                        |
| INT1_DRDY_XL       | Accelerometer Data Ready on INT1 pad. Default value: 0<br>(0: disabled; 1: enabled)                    |

## 9.10 INT2\_CTRL (0Eh)

INT2 pad control register (r/w).

Each bit in this register enables a signal to be carried through INT2. The pad's output will supply the OR combination of the selected signals.

**Table 42. INT2\_CTRL register**

|                 |                    |                |               |          |                |             |              |
|-----------------|--------------------|----------------|---------------|----------|----------------|-------------|--------------|
| INT2_STEP_DELTA | INT2_STEP_COUNT_OV | INT2_FULL_FLAG | INT2_FIFO_OVR | INT2_FTH | INT2_DRDY_TEMP | INT2_DRDY_G | INT2_DRDY_XL |
|-----------------|--------------------|----------------|---------------|----------|----------------|-------------|--------------|

**Table 43. INT2\_CTRL register description**

|                    |   |
|--------------------|---|
| INT2_STEP_DELTA    | Pedometer step recognition interrupt on delta time <sup>(1)</sup> enable on INT2 pad. Default value: 0<br>(0: disabled; 1: enabled) |
| INT2_STEP_COUNT_OV | Step counter overflow interrupt enable on INT2 pad. Default value: 0<br>(0: disabled; 1: enabled)                                   |
| INT2_FULL_FLAG     | FIFO full flag interrupt enable on INT2 pad. Default value: 0<br>(0: disabled; 1: enabled)  |
| INT2_FIFO_OVR      | FIFO overrun interrupt on INT2 pad. Default value: 0<br>(0: disabled; 1: enabled)   |
| INT2_FTH           | FIFO threshold interrupt on INT2 pad. Default value: 0<br>(0: disabled; 1: enabled)   |
| INT2_DRDY_TEMP     | Temperature Data Ready in INT2 pad. Default value: 0<br>(0: disabled; 1: enabled)   |
| INT2_DRDY_G        | Gyroscope Data Ready on INT2 pad. Default value: 0<br>(0: disabled; 1: enabled)   |
| INT2_DRDY_XL       | Accelerometer Data Ready on INT2 pad. Default value: 0<br>(0: disabled; 1: enabled)   |

1. Delta time value is defined in register STEP\_COUNT\_DELTA (15h).

## 9.11 WHO\_AM\_I (0Fh)

Who\_AM\_I register (r). This register is a read-only register. Its value is fixed at 69h.

**Table 44. WHO\_AM\_I register**

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
|---|---|---|---|---|---|---|---|

## 9.12 CTRL1\_XL (10h)

Linear acceleration sensor control register 1 (r/w).

**Table 45. CTRL1\_XL register**

|         |         |         |         |        |        |        |        |
|---------|---------|---------|---------|--------|--------|--------|--------|
| ODR_XL3 | ODR_XL2 | ODR_XL1 | ODR_XL0 | FS_XL1 | FS_XL0 | BW_XL1 | BW_XL0 |
|---------|---------|---------|---------|--------|--------|--------|--------|

**Table 46. CTRL1\_XL register description**

|              |  |
|--------------|--|
| ODR_XL [3:0] | Output data rate and power mode selection. Default value: 0000 (see <a href="#">Table 47</a> ).                |
| FS_XL [1:0]  | Accelerometer full-scale selection. Default value: 00.<br>(00: ±2 g; 01: ±16 g; 10: ±4 g; 11: ±8 g)            |
| BW_XL [1:0]  | Anti-aliasing filter bandwidth selection. Default value: 00<br>(00: 400 Hz; 01: 200 Hz; 10: 100 Hz; 11: 50 Hz) |

**Table 47. Accelerometer ODR register setting**

| ODR_XL3 | ODR_XL2 | ODR_XL1 | ODR_XL0 | ODR selection [Hz] when XL_HM_MODE = 1 | ODR selection [Hz] when XL_HM_MODE = 0 |
|---------|---------|---------|---------|--|--|
| 0       | 0       | 0       | 0       | Power-down                             | Power-down                             |
| 0       | 0       | 0       | 1       | 12.5 Hz (low power)                    | 12.5 Hz (high performance)             |
| 0       | 0       | 1       | 0       | 26 Hz (low power)                      | 26 Hz (high performance)               |
| 0       | 0       | 1       | 1       | 52 Hz (low power)                      | 52 Hz (high performance)               |
| 0       | 1       | 0       | 0       | 104 Hz (normal mode)                   | 104 Hz (high performance)              |
| 0       | 1       | 0       | 1       | 208 Hz (normal mode)                   | 208 Hz (high performance)              |
| 0       | 1       | 1       | 0       | 416 Hz (high performance)              | 416 Hz (high performance)              |
| 0       | 1       | 1       | 1       | 833 Hz (high performance)              | 833 Hz (high performance)              |
| 1       | 0       | 0       | 0       | 1.66 kHz (high performance)            | 1.66 kHz (high performance)            |
| 1       | 0       | 0       | 1       | 3.33 kHz (high performance)            | 3.33 kHz (high performance)            |
| 1       | 0       | 1       | 0       | 6.66 kHz (high performance)            | 6.66 kHz (high performance)            |

**Table 48. BW and ODR (high-performance mode)**

| ODR <sup>(1)</sup> | Analog filter BW (XL_HM_MODE = 0) |   |
|--------------------|-----------------------------------|---|
|                    | XL_BW_SCAL_ODR = 0                | XL_BW_SCAL_ODR = 1  |
| 6.66 - 3.33 kHz    | Filter not used                   | Bandwidth is determined by setting BW_XL[1:0] in <a href="#">CTRL1_XL (10h)</a> |
| 1.66 kHz           | 400 Hz                            |   |
| 833 Hz             | 400 Hz                            |   |
| 416 Hz             | 200 Hz                            |   |
| 208 Hz             | 100 Hz                            |   |
| 104 - 12.5 Hz      | 50 Hz                             |   |

1. Filter not used when accelerometer is in normal and low-power modes.

### 9.13 CTRL2\_G (11h)

Angular rate sensor control register 2 (r/w).

**Table 49. CTRL2\_G register**

|        |        |        |        |       |       |        |                  |
|--------|--------|--------|--------|-------|-------|--------|------------------|
| ODR_G3 | ODR_G2 | ODR_G1 | ODR_G0 | FS_G1 | FS_G0 | FS_125 | 0 <sup>(1)</sup> |
|--------|--------|--------|--------|-------|-------|--------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 50. CTRL2\_G register description**

|             |   |
|-------------|---|
| ODR_G [3:0] | Gyroscope output data rate selection. Default value: 0000<br>(Refer to <a href="#">Table 51</a> )           |
| FS_G [1:0]  | Gyroscope full-scale selection. Default value: 00<br>(00: 245 dps; 01: 500 dps; 10: 1000 dps; 11: 2000 dps) |
| FS_125      | Gyroscope full-scale at 125 dps. Default value: 0<br>(0: disabled; 1: enabled)                              |

**Table 51. Gyroscope ODR configuration setting**

| ODR_G3 | ODR_G2 | ODR_G1 | ODR_G0 | ODR [Hz] when G_HM_MODE = 1 | ODR [Hz] when G_HM_MODE = 0 |
|--------|--------|--------|--------|-----------------------------|-----------------------------|
| 0      | 0      | 0      | 0      | Power down                  | Power down                  |
| 0      | 0      | 0      | 1      | 12.5 Hz (low power)         | 12.5 Hz (high performance)  |
| 0      | 0      | 1      | 0      | 26 Hz (low power)           | 26 Hz (high performance)    |
| 0      | 0      | 1      | 1      | 52 Hz (low power)           | 52 Hz (high performance)    |
| 0      | 1      | 0      | 0      | 104 Hz (normal mode)        | 104 Hz (high performance)   |
| 0      | 1      | 0      | 1      | 208 Hz (normal mode)        | 208 Hz (high performance)   |
| 0      | 1      | 1      | 0      | 416 Hz (high performance)   | 416 Hz (high performance)   |
| 0      | 1      | 1      | 1      | 833 Hz (high performance)   | 833 Hz (high performance)   |
| 1      | 0      | 0      | 0      | 1.66 kHz (high performance) | 1.66 kHz (high performance) |

## 9.14 CTRL3\_C (12h)

Control register 3 (r/w).

**Table 52. CTRL3\_C register**

|      |     |           |       |     |        |     |          |
|------|-----|-----------|-------|-----|--------|-----|----------|
| BOOT | BDU | H_LACTIVE | PP_OD | SIM | IF_INC | BLE | SW_RESET |
|------|-----|-----------|-------|-----|--------|-----|----------|

**Table 53. CTRL3\_C register description**

|           |   |
|-----------|---|
| BOOT      | Reboot memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content <sup>(1)</sup> )   |
| BDU       | Block Data Update. Default value: 0<br>(0: continuous update; 1: output registers not updated until MSB and LSB have been read)   |
| H_LACTIVE | Interrupt activation level. Default value: 0<br>(0: interrupt output pads active high; 1: interrupt output pads active low)   |
| PP_OD     | Push-pull/open-drain selection on INT1 and INT2 pads. Default value: 0<br>(0: push-pull mode; 1: open-drain mode)   |
| SIM       | SPI Serial Interface Mode selection. Default value: 0<br>(0: 4-wire interface; 1: 3-wire interface).  |
| IF_INC    | Register address automatically incremented during a multiple byte access with a serial interface (I <sup>2</sup> C or SPI). Default value: 1<br>(0: disabled; 1: enabled) |
| BLE       | Big/Little Endian Data selection. Default value 0<br>(0: data LSB @ lower address; 1: data MSB @ lower address)   |
| SW_RESET  | Software reset. Default value: 0<br>(0: normal mode; 1: reset device)<br>This bit is cleared by hardware after next flash boot.   |

1. Boot request is executed as soon as internal oscillator is turned on. It is possible to set bit while in power-down mode, in this case it will be served at the next normal mode or sleep mode.

## 9.15 CTRL4\_C (13h)

Control register 4 (r/w).

**Table 54. CTRL4\_C register**

|                    |         |                  |                  |               |             |                  |                  |
|--------------------|---------|------------------|------------------|---------------|-------------|------------------|------------------|
| XL_BW_<br>SCAL_ODR | SLEEP_G | INT2_on_<br>INT1 | FIFO_<br>TEMP_EN | DRDY_<br>MASK | I2C_disable | 0 <sup>(1)</sup> | STOP_ON_<br>_FTH |
|--------------------|---------|------------------|------------------|---------------|-------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 55. CTRL4\_C register description**

|                    |   |
|--------------------|---|
| XL_BW_<br>SCAL_ODR | Accelerometer bandwidth selection. Default value: 0<br>(0 <sup>(1)</sup> : bandwidth determined by ODR selection, refer to <a href="#">Table 48</a> ;<br>1 <sup>(2)</sup> : bandwidth determined by setting BW_XL[1:0] in <a href="#">CTRL1_XL (10h)</a> register.) |
| SLEEP_G            | Gyroscope sleep mode enable. Default value: 0<br>(0: disabled; 1: enabled)  |
| INT2_on_INT1       | All interrupt signals available on INT1 pad enable. Default value: 0<br>(0: interrupt signals divided between INT1 and INT2 pads;<br>1: all interrupt signals in logic or on INT1 pad)  |
| FIFO_TEMP_EN       | Enable temperature data as 4 <sup>th</sup> FIFO data set <sup>(3)</sup> . Default: 0<br>(0: disable temperature data as 4 <sup>th</sup> FIFO data set;<br>1: enable temperature data as 4 <sup>th</sup> FIFO data set)  |
| DRDY_MASK          | Data-ready mask enable. If enabled, when switching from Power-Down to an active mode, the accelerometer and gyroscope data-ready signals are masked until the settling of the sensor filters is completed. Default value: 0<br>(0: disabled; 1: enabled)            |
| I2C_disable        | Disable I <sup>2</sup> C interface. Default value: 0<br>(0: both I <sup>2</sup> C and SPI enabled; 1: I <sup>2</sup> C disabled, SPI only)  |
| STOP_ON_FTH        | Enable FIFO threshold level use. Default value: 0<br>(0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level)  |

1. Filter used in high-performance mode only with ODR less than 3.33 kHz.

2. Filter used in high-performance mode only.

3. This bit is effective if the TIMER\_PEDO\_FIFO\_EN bit of [FIFO\\_CTRL2 \(07h\)](#) register is set to 0.

## 9.16 CTRL5\_C (14h)

Control register 5 (r/w).

**Table 56. CTRL5\_C register**

|           |           |           |                  |       |       |        |        |
|-----------|-----------|-----------|------------------|-------|-------|--------|--------|
| ROUNDING2 | ROUNDING1 | ROUNDING0 | 0 <sup>(1)</sup> | ST1_G | ST0_G | ST1_XL | ST0_XL |
|-----------|-----------|-----------|------------------|-------|-------|--------|--------|

1. This bit must be set to '0' for the correct operation of the device



**Table 57. CTRL5\_C register description**

|               |  |
|---------------|--|
| ROUNDING[2:0] | Circular burst-mode (rounding) read from output registers. Default: 000 (000: no rounding; Others: refer to <a href="#">Table 58</a> ) |
| ST_G [1:0]    | Angular rate sensor self-test enable. Default value: 00 (00: Self-test disabled; Other: refer to <a href="#">Table 59</a> )            |
| ST_XL [1:0]   | Linear acceleration sensor self-test enable. Default value: 00 (00: Self-test disabled; Other: refer to <a href="#">Table 60</a> )     |

**Table 58. Output registers rounding pattern**

| ROUNDING[2:0] | Rounding pattern  |
|---------------|---|
| 000           | No rounding   |
| 001           | Accelerometer only  |
| 010           | Gyroscope only  |
| 011           | Gyroscope + accelerometer   |
| 100           | Registers from <a href="#">SENSORHUB1_REG (2Eh)</a> to <a href="#">SENSORHUB6_REG (33h)</a> only  |
| 101           | Accelerometer + registers from <a href="#">SENSORHUB1_REG (2Eh)</a> to <a href="#">SENSORHUB6_REG (33h)</a>   |
| 110           | Gyroscope + accelerometer + registers from <a href="#">SENSORHUB1_REG (2Eh)</a> to <a href="#">SENSORHUB6_REG (33h)</a> and registers from <a href="#">SENSORHUB7_REG (34h)</a> to <a href="#">SENSORHUB12_REG(39h)</a> |
| 111           | Gyroscope + accelerometer + registers from <a href="#">SENSORHUB1_REG (2Eh)</a> to <a href="#">SENSORHUB6_REG (33h)</a>   |

**Table 59. Angular rate sensor self-test mode selection**

| ST1_G | ST0_G | Self-test mode          |
|-------|-------|-------------------------|
| 0     | 0     | Normal mode             |
| 0     | 1     | Positive sign self-test |
| 1     | 0     | Not allowed             |
| 1     | 1     | Negative sign self-test |

**Table 60. Linear acceleration sensor self-test mode selection**

| ST1_XL | ST0_XL | Self-test mode          |
|--------|--------|-------------------------|
| 0      | 0      | Normal mode             |
| 0      | 1      | Positive sign self-test |
| 1      | 0      | Negative sign self-test |
| 1      | 1      | Not allowed             |

## 9.17 CTRL6\_C (15h)

Angular rate sensor control register 6 (r/w).

**Table 61. CTRL6\_C register**

|         |       |         |            |                  |                  |                  |                  |
|---------|-------|---------|------------|------------------|------------------|------------------|------------------|
| TRIG_EN | LVLen | LVL2_EN | XL_HM_MODE | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|---------|-------|---------|------------|------------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 62. CTRL6\_C register description**

|            |   |
|------------|---|
| TRIG_EN    | Gyroscope data edge-sensitive trigger enable. Default value: 0<br>(0: external trigger disabled; 1: external trigger enabled)   |
| LVLen      | Gyroscope data level-sensitive trigger enable. Default value: 0<br>(0: level-sensitive trigger disabled; 1: level sensitive trigger enabled)  |
| LVL2_EN    | Gyroscope level-sensitive latched enable. Default value: 0<br>(0: level-sensitive latched disabled; 1: level sensitive latched enabled)   |
| XL_HM_MODE | High-performance operating mode disable for accelerometer <sup>(1)</sup> . Default value: 0<br>(0: high-performance operating mode enabled;<br>1: high-performance operating mode disabled) |

1. Normal and low-power mode depends on the ODR setting, for details refer to [Table 47](#).

## 9.18 CTRL7\_G (16h)

Angular rate sensor control register 7 (r/w).

**Table 63. CTRL7\_G register**

|           |         |         |         |          |                 |                  |                  |
|-----------|---------|---------|---------|----------|-----------------|------------------|------------------|
| G_HM_MODE | HP_G_EN | HPCF_G1 | HPCF_G0 | HP_G_RST | ROUNDING_STATUS | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|-----------|---------|---------|---------|----------|-----------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 64. CTRL7\_G register description**

|                 |  |
|-----------------|--|
| G_HM_MODE       | High-performance operating mode disable for gyroscope <sup>(1)</sup> . Default: 0<br>(0: high-performance operating mode enabled;<br>1: high-performance operating mode disabled)                            |
| HP_G_EN         | Gyroscope digital high-pass filter enable. The filter is enabled only if the gyro is in HP mode. Default value: 0<br>(0: HPF disabled; 1: HPF enabled)   |
| HP_G_RST        | Gyro digital HP filter reset. Default: 0<br>(0: gyro digital HP filter reset OFF; 1: gyro digital HP filter reset ON)  |
| ROUNDING_STATUS | Source register rounding function enable on <a href="#">STATUS_REG (1Eh)</a> , <a href="#">FUNC_SRC (53h)</a> and <a href="#">WAKE_UP_SRC (1Bh)</a> registers. Default value: 0<br>(0: disabled; 1: enabled) |
| HPCF_G[1:0]     | Gyroscope high-pass filter cutoff frequency selection. Default value: 00.<br>Refer to <a href="#">Table 65</a> .   |

1. Normal and low-power mode depends on the ODR setting, for details refer to [Table 51](#).

**Table 65. Gyroscope high-pass filter mode configuration**

| HPCF_G1 | HPCF_G0 | High-pass filter cutoff frequency |
|---------|---------|-----------------------------------|
| 0       | 0       | 0.0081 Hz                         |
| 0       | 1       | 0.0324 Hz                         |
| 1       | 0       | 2.07 Hz                           |
| 1       | 1       | 16.32 Hz                          |

## 9.19 CTRL8\_XL (17h)

Linear acceleration sensor control register 8 (r/w).

**Table 66. CTRL8\_XL register**

|            |          |          |                  |                  |                |                  |                |
|------------|----------|----------|------------------|------------------|----------------|------------------|----------------|
| LPF2_XL_EN | HPCF_XL1 | HPCF_XL0 | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | HP_SLOPE_XL_EN | 0 <sup>(1)</sup> | LOW_PASS_ON_6D |
|------------|----------|----------|------------------|------------------|----------------|------------------|----------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 67. CTRL8\_XL register description**

|                |  |
|----------------|--|
| LPF2_XL_EN     | Accelerometer low-pass filter LPF2 selection. Refer to <a href="#">Figure 6</a> .  |
| HPCF_XL[1:0]   | Accelerometer slope filter and high-pass filter configuration and cutoff setting. Refer to <a href="#">Table 68</a> . It is also used to select the cutoff frequency of the LPF2 filter, as shown in <a href="#">Table 69</a> . This low-pass filter can also be used in the 6D/4D functionality by setting the LOW_PASS_ON_6D bit of <a href="#">CTRL8_XL (17h)</a> to 1. |
| HP_SLOPE_XL_EN | Accelerometer slope filter / high-pass filter selection. Refer to <a href="#">Figure 6</a> .   |
| LOW_PASS_ON_6D | Low-pass filter on 6D function selection. Refer to <a href="#">Figure 6</a> .  |

**Table 68. Accelerometer slope and high-pass filter selection and cutoff frequency**

| HPCF_XL[1:0] | Applied filter | HP filter cutoff frequency [Hz] |
|--------------|----------------|---------------------------------|
| 00           | Slope          | ODR_XL/4                        |
| 01           | High-pass      | ODR_XL/100                      |
| 10           | High-pass      | ODR_XL/9                        |
| 11           | High-pass      | ODR_XL/400                      |

**Table 69. Accelerometer LPF2 cutoff frequency**

| HPCF_XL[1:0] | LPF2 digital filter cutoff frequency [Hz] |
|--------------|---|
| 00           | ODR_XL/50                                 |
| 01           | ODR_XL/100                                |
| 10           | ODR_XL/9                                  |
| 11           | ODR_XL/400                                |

## 9.20 CTRL9\_XL (18h)

Linear acceleration sensor control register 9 (r/w).

**Table 70. CTRL9\_XL register**

|                  |                  |        |        |        |         |                  |                  |
|------------------|------------------|--------|--------|--------|---------|------------------|------------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | Zen_XL | Yen_XL | Xen_XL | SOFT_EN | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|------------------|------------------|--------|--------|--------|---------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 71. CTRL9\_XL register description**

|         |   |
|---------|---|
| Zen_XL  | Accelerometer Z-axis output enable. Default value: 1<br>(0: Z-axis output disabled; 1: Z-axis output enabled)   |
| Yen_XL  | Accelerometer Y-axis output enable. Default value: 1<br>(0: Y-axis output disabled; 1: Y-axis output enabled)   |
| Xen_XL  | Accelerometer X-axis output enable. Default value: 1<br>(0: X-axis output disabled; 1: X-axis output enabled)   |
| SOFT_EN | Enable soft-iron correction algorithm for magnetometer <sup>(1)</sup> . Default value: 0<br>(0: soft-iron correction algorithm disabled;<br>1: soft-iron correction algorithm disabled) |

1. This bit is effective if the IRON\_EN bit of *MASTER\_CONFIG (1Ah)* is set to 1.

## 9.21 CTRL10\_C (19h)

Control register 10 (r/w).

**Table 72. CTRL10\_C register**

|                  |                  |       |       |       |         |               |                |
|------------------|------------------|-------|-------|-------|---------|---------------|----------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | Zen_G | Yen_G | Xen_G | FUNC_EN | PEDO_RST_STEP | SIGN_MOTION_EN |
|------------------|------------------|-------|-------|-------|---------|---------------|----------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 73. CTRL10\_C register description**

|                |   |
|----------------|---|
| Zen_G          | Gyroscope yaw axis (Z) output enable. Default value: 1<br>(0: Z-axis output disabled; 1: Z-axis output enabled)   |
| Yen_G          | Gyroscope roll axis (Y) output enable. Default value: 1<br>(0: Y-axis output disabled; 1: Y axis output enabled)  |
| Xen_G          | Gyroscope pitch axis (X) output enable. Default value: 1<br>(0: X-axis output disabled; 1: X-axis output enabled)   |
| FUNC_EN        | Enable embedded functionalities (pedometer, tilt, significant motion, sensor hub and ironing) and accelerometer HP and LPF2 filters (refer to <i>Figure 6</i> ). Default value: 0<br>(0: disable functionalities of embedded functions and accelerometer filters;<br>1: enable functionalities of embedded functions and accelerometer filters) |
| PEDO_RST_STEP  | Reset pedometer step counter. Default value: 0<br>(0: disabled; 1: enabled)   |
| SIGN_MOTION_EN | Enable significant motion function. Default value: 0<br>(0: disabled; 1: enabled)   |

## 9.22 MASTER\_CONFIG (1Ah)

Master configuration register (r/w).

**Table 74. MASTER\_CONFIG register**

|              |                     |                  |              |            |                   |         |           |
|--------------|---------------------|------------------|--------------|------------|-------------------|---------|-----------|
| DRDY_ON_INT1 | DATA_VALID_SEL_FIFO | 0 <sup>(1)</sup> | START_CONFIG | PULL_UP_EN | PASS_THROUGH_MODE | IRON_EN | MASTER_ON |
|--------------|---------------------|------------------|--------------|------------|-------------------|---------|-----------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 75. MASTER\_CONFIG register description**

|                     |   |
|---------------------|---|
| DRDY_ON_INT1        | Manage the Master DRDY signal on INT1 pad. Default: 0<br>(0: disable Master DRDY on INT1; 1: enable Master DRDY on INT1)  |
| DATA_VALID_SEL_FIFO | Selection of FIFO data-valid signal. Default value: 0<br>(0: data-valid signal used to write data in FIFO is the XL/Gyro data-ready or step detection <sup>(1)</sup> ;<br>1: data-valid signal used to write data in FIFO is the sensor hub data-ready) |
| START_CONFIG        | Sensor Hub trigger signal selection. Default value: 0<br>(0: Sensor hub signal is the XL/Gyro data-ready;<br>1: Sensor hub signal external from INT2 pad.)  |
| PULL_UP_EN          | Auxiliary I <sup>2</sup> C pull-up. Default value: 0<br>(0: internal pull-up on auxiliary I <sup>2</sup> C line disabled;<br>1: internal pull-up on auxiliary I <sup>2</sup> C line enabled)  |
| PASS_THROUGH_MODE   | I <sup>2</sup> C interface pass-through. Default value: 0<br>(0: through disabled; 1: through enabled)  |
| IRON_EN             | Enable hard-iron correction algorithm for magnetometer. Default value: 0<br>(0: hard-iron correction algorithm disabled;<br>1: hard-iron correction algorithm enabled)  |
| MASTER_ON           | Sensor hub I <sup>2</sup> C master enable. Default: 0<br>(0: master I <sup>2</sup> C of sensor hub disabled; 1: master I <sup>2</sup> C of sensor hub enabled)  |

1. If the `TIMER_PEDO_FIFO_DRDY` bit in `FIFO_CTRL2 (07h)` is set to 0, the trigger for writing data in FIFO is XL/Gyro data-ready, otherwise it's the step detection.

## 9.23 WAKE\_UP\_SRC (1Bh)

Wake up interrupt source register (r).

**Table 76. WAKE\_UP\_SRC register**

|                  |                  |       |                |       |      |      |      |
|------------------|------------------|-------|----------------|-------|------|------|------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | FF_IA | SLEEP_STATE_IA | WU_IA | X_WU | Y_WU | Z_WU |
|------------------|------------------|-------|----------------|-------|------|------|------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 77. WAKE\_UP\_SRC register description**

|                |   |
|----------------|---|
| FF_IA          | Free-fall event detection status. Default: 0<br>(0: free-fall event not detected; 1: free-fall event detected)                            |
| SLEEP_STATE_IA | Sleep event status. Default value: 0<br>(0: sleep event not detected; 1: sleep event detected)  |
| WU_IA          | Wakeup event detection status. Default value: 0<br>(0: wakeup event not detected; 1: wakeup event detected.)                              |
| X_WU           | Wakeup event detection status on X-axis. Default value: 0<br>(0: wakeup event on X-axis not detected; 1: wakeup event on X-axis detected) |
| Y_WU           | Wakeup event detection status on Y-axis. Default value: 0<br>(0: wakeup event on Y-axis not detected; 1: wakeup event on Y-axis detected) |
| Z_WU           | Wakeup event detection status on Z-axis. Default value: 0<br>(0: wakeup event on Z-axis not detected; 1: wakeup event on Z-axis detected) |

## 9.24 TAP\_SRC (1Ch)

Tap source register (r).

**Table 78. TAP\_SRC register**

|                  |        |            |            |          |       |       |       |
|------------------|--------|------------|------------|----------|-------|-------|-------|
| 0 <sup>(1)</sup> | TAP_IA | SINGLE_TAP | DOUBLE_TAP | TAP_SIGN | X_TAP | Y_TAP | Z_TAP |
|------------------|--------|------------|------------|----------|-------|-------|-------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 79. TAP\_SRC register description**

|            |   |
|------------|---|
| TAP_IA     | Tap event detection status. Default: 0<br>(0: tap event not detected; 1: tap event detected)  |
| SINGLE_TAP | Single-tap event status. Default value: 0<br>(0: single tap event not detected; 1: single tap event detected)   |
| DOUBLE_TAP | Double-tap event detection status. Default value: 0<br>(0: double-tap event not detected; 1: double-tap event detected.)  |
| TAP_SIGN   | Sign of acceleration detected by tap event. Default: 0<br>(0: positive sign of acceleration detected by tap event;<br>1: negative sign of acceleration detected by tap event) |
| X_TAP      | Tap event detection status on X-axis. Default value: 0<br>(0: tap event on X-axis not detected; 1: tap event on X-axis detected)  |
| Y_TAP      | Tap event detection status on Y-axis. Default value: 0<br>(0: tap event on Y-axis not detected; 1: tap event on Y-axis detected)  |
| Z_TAP      | Tap event detection status on Z-axis. Default value: 0<br>(0: tap event on Z-axis not detected; 1: tap event on Z-axis detected)  |

## 9.25 D6D\_SRC (1Dh)

Portrait, landscape, face-up and face-down source register (r).

**Table 80. D6D\_SRC register**

|                  |        |    |    |    |    |    |    |
|------------------|--------|----|----|----|----|----|----|
| 0 <sup>(1)</sup> | D6D_IA | ZH | ZL | YH | YL | XH | XL |
|------------------|--------|----|----|----|----|----|----|

1. This bit must be set to '0' for the correct operation of the device.

**Table 81. D6D\_SRC register description**

|        |  |
|--------|--|
| D6D_IA | Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0<br>(0: change position not detected; 1: change position detected) |
| ZH     | Z-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over threshold) detected)  |
| ZL     | Z-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected)   |
| YH     | Y-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over-threshold) detected)  |
| YL     | Y-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected)   |
| X_H    | X-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over threshold) detected)  |
| X_L    | X-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected)   |

## 9.26 STATUS\_REG (1Eh)

**Table 82. STATUS\_REG register**

|   |   |   |   |         |     |     |      |
|---|---|---|---|---------|-----|-----|------|
| - | - | - | - | EV_BOOT | TDA | GDA | XLDA |
|---|---|---|---|---------|-----|-----|------|

**Table 83. STATUS\_REG register description**

|      |  |
|------|--|
|      |  |
| TDA  | Temperature new data available. Default: 0<br>(0: no set of data is available at temperature sensor output;<br>1: a new set of data is available at temperature sensor output) |
| GDA  | Gyroscope new data available. Default value: 0<br>(0: no set of data available at gyroscope output;<br>1: a new set of data is available at gyroscope output)                  |
| XLDA | Accelerometer new data available. Default value: 0<br>(0: no set of data available at accelerometer output;<br>1: a new set of data is available at accelerometer output)      |

## 9.27 OUT\_TEMP\_L (20h), OUT\_TEMP(21h)

Temperature data output register (r). L and H registers together express a 16-bit word in two's complement.

**Table 84. OUT\_TEMP\_L register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Temp7 | Temp6 | Temp5 | Temp4 | Temp3 | Temp2 | Temp1 | Temp0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 85. OUT\_TEMP\_H register**

|        |        |        |        |        |        |       |       |
|--------|--------|--------|--------|--------|--------|-------|-------|
| Temp15 | Temp14 | Temp13 | Temp12 | Temp11 | Temp10 | Temp9 | Temp8 |
|--------|--------|--------|--------|--------|--------|-------|-------|

**Table 86. OUT\_TEMP register description**

|            |  |
|------------|--|
| Temp[15:0] | Temperature sensor output data<br>The value is expressed as two's complement sign extended on the MSB. |
|------------|--|

## 9.28 OUTX\_L\_G (22h)

Angular rate sensor pitch axis (X) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 87. OUTX\_L\_G register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 88. OUTX\_L\_G register description**

|        |  |
|--------|--|
| D[7:0] | Pitch axis (X) angular rate value (LSbyte) |
|--------|--|

## 9.29 OUTX\_H\_G (23h)

Angular rate sensor pitch axis (X) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 89. OUTX\_H\_G register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 90. OUTX\_H\_G register description**

|         |  |
|---------|--|
| D[15:8] | Pitch axis (X) angular rate value (MSbyte) |
|---------|--|

## 9.30 OUTY\_L\_G (24h)

Angular rate sensor roll axis (Y) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 91. OUTY\_L\_G register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 92. OUTY\_L\_G register description**

|        |   |
|--------|---|
| D[7:0] | Roll axis (Y) angular rate value (LSbyte) |
|--------|---|



### 9.31 OUTY\_H\_G (25h)

Angular rate sensor roll axis (Y) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 93. OUTY\_H\_G register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 94. OUTY\_H\_G register description**

|         |   |
|---------|---|
| D[15:8] | Roll axis (Y) angular rate value (MSbyte) |
|---------|---|

### 9.32 OUTZ\_L\_G (26h)

Angular rate sensor yaw axis (Z) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 95. OUTZ\_L\_G register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 96. OUTZ\_L\_G register description**

|        |  |
|--------|--|
| D[7:0] | Yaw axis (Z) angular rate value (LSbyte) |
|--------|--|

### 9.33 OUTZ\_H\_G (27h)

Angular rate sensor Yaw axis (Z) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 97. OUTZ\_H\_G register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 98. OUTZ\_H\_G register description**

|         |  |
|---------|--|
| D[15:8] | Yaw axis (Z) angular rate value (MSbyte) |
|---------|--|

### 9.34 OUTX\_L\_XL (28h)

Linear acceleration sensor X-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 99. OUTX\_L\_XL register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 100. OUTX\_L\_XL register description**

|        |   |
|--------|---|
| D[7:0] | X-axis linear acceleration value (LSbyte) |
|--------|---|

### 9.35 OUTX\_H\_XL (29h)

Linear acceleration sensor X-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 101. OUTX\_H\_XL register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 102. OUTX\_H\_XL register description**

|         |   |
|---------|---|
| D[15:8] | X-axis linear acceleration value (MSbyte) |
|---------|---|

### 9.36 OUTY\_L\_XL (2Ah)

Linear acceleration sensor Y-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 103. OUTY\_L\_XL register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 104. OUTY\_L\_XL register description**

|        |   |
|--------|---|
| D[7:0] | Y-axis linear acceleration value (LSbyte) |
|--------|---|

### 9.37 OUTY\_H\_XL (2Bh)

Linear acceleration sensor Y-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 105. OUTY\_H\_G register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 106. OUTY\_H\_G register description**

|         |   |
|---------|---|
| D[15:8] | Y-axis linear acceleration value (MSbyte) |
|---------|---|

### 9.38 OUTZ\_L\_XL (2Ch)

Linear acceleration sensor Z-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 107. OUTZ\_L\_XL register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 108. OUTZ\_L\_XL register description**

|        |   |
|--------|---|
| D[7:0] | Z-axis linear acceleration value (LSbyte) |
|--------|---|

### 9.39 OUTZ\_H\_XL (2Dh)

Linear acceleration sensor Z-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 109. OUTZ\_H\_XL register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 110. OUTZ\_H\_XL register description**

|         |   |
|---------|---|
| D[15:8] | Z-axis linear acceleration value (MSbyte) |
|---------|---|

### 9.40 SENSORHUB1\_REG (2Eh)

First byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 111. SENSORHUB1\_REG register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub1_7 | SHub1_6 | SHub1_5 | SHub1_4 | SHub1_3 | SHub1_2 | SHub1_1 | SHub1_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 112. SENSORHUB1\_REG register description**

|             |   |
|-------------|---|
| SHub1_[7:0] | First byte associated to external sensors |
|-------------|---|

### 9.41 SENSORHUB2\_REG (2Fh)

Second byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operations configurations (for external sensors from x = 0 to x = 3).

**Table 113. SENSORHUB2\_REG register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub2_7 | SHub2_6 | SHub2_5 | SHub2_4 | SHub2_3 | SHub2_2 | SHub2_1 | SHub2_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 114. SENSORHUB2\_REG register description**

|             |  |
|-------------|--|
| SHub2_[7:0] | Second byte associated to external sensors |
|-------------|--|

### 9.42 SENSORHUB3\_REG (30h)

Third byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operations configurations (for external sensors from x = 0 to x = 3).

**Table 115. SENSORHUB3\_REG register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub3_7 | SHub3_6 | SHub3_5 | SHub3_4 | SHub3_3 | SHub3_2 | SHub3_1 | SHub3_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 116. SENSORHUB3\_REG register description**

|             |   |
|-------------|---|
| SHub3_[7:0] | Third byte associated to external sensors |
|-------------|---|

### 9.43 SENSORHUB4\_REG (31h)

Fourth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 117. SENSORHUB4\_REG register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub4_7 | SHub4_6 | SHub4_5 | SHub4_4 | SHub4_3 | SHub4_2 | SHub4_1 | SHub4_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 118. SENSORHUB4\_REG register description**

|             |  |
|-------------|--|
| SHub4_[7:0] | Fourth byte associated to external sensors |
|-------------|--|

### 9.44 SENSORHUB5\_REG (32h)

Fifth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 119. SENSORHUB5\_REG register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub5_7 | SHub5_6 | SHub5_5 | SHub5_4 | SHub5_3 | SHub5_2 | SHub5_1 | SHub5_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 120. SENSORHUB5\_REG register description**

|             |   |
|-------------|---|
| SHub5_[7:0] | Fifth byte associated to external sensors |
|-------------|---|

### 9.45 SENSORHUB6\_REG (33h)

Sixth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 121. SENSORHUB6\_REG register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub6_7 | SHub6_6 | SHub6_5 | SHub6_4 | SHub6_3 | SHub6_2 | SHub6_1 | SHub6_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 122. SENSORHUB6\_REG register description**

|             |   |
|-------------|---|
| SHub6_[7:0] | Sixth byte associated to external sensors |
|-------------|---|

### 9.46 SENSORHUB7\_REG (34h)

Seventh byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 123. SENSORHUB7\_REG register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub7_7 | SHub7_6 | SHub7_5 | SHub7_4 | SHub7_3 | SHub7_2 | SHub7_1 | SHub7_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 124. SENSORHUB7\_REG register description**

|             |   |
|-------------|---|
| SHub7_[7:0] | Seventh byte associated to external sensors |
|-------------|---|

### 9.47 SENSORHUB8\_REG(35h)

Eighth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 125. SENSORHUB8\_REG register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub8_7 | SHub8_6 | SHub8_5 | SHub8_4 | SHub8_3 | SHub8_2 | SHub8_1 | SHub8_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 126. SENSORHUB8\_REG register description**

|             |  |
|-------------|--|
| SHub8_[7:0] | Eighth byte associated to external sensors |
|-------------|--|

### 9.48 SENSORHUB9\_REG (36h)

Ninth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 127. SENSORHUB9\_REG register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHub9_7 | SHub9_6 | SHub9_5 | SHub9_4 | SHub9_3 | SHub9_2 | SHub9_1 | SHub9_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 128. SENSORHUB9\_REG register description**

|             |   |
|-------------|---|
| SHub9_[7:0] | Ninth byte associated to external sensors |
|-------------|---|

### 9.49 SENSORHUB10\_REG (37h)

Tenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 129. SENSORHUB10\_REG register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub10_7 | SHub10_6 | SHub10_5 | SHub10_4 | SHub10_3 | SHub10_2 | SHub10_1 | SHub10_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 130. SENSORHUB10\_REG register description**

|              |   |
|--------------|---|
| SHub10_[7:0] | Tenth byte associated to external sensors |
|--------------|---|

### 9.50 SENSORHUB11\_REG (38h)

Eleventh byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 131. SENSORHUB11\_REG register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub11_7 | SHub11_6 | SHub11_5 | SHub11_4 | SHub11_3 | SHub11_2 | SHub11_1 | SHub11_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 132. SENSORHUB11\_REG register description**

|              |  |
|--------------|--|
| SHub11_[7:0] | Eleventh byte associated to external sensors |
|--------------|--|

### 9.51 SENSORHUB12\_REG(39h)

Twelfth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 133. SENSORHUB12\_REG register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub12_7 | SHub12_6 | SHub12_5 | SHub12_4 | SHub12_3 | SHub12_2 | SHub12_1 | SHub12_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 134. SENSORHUB12\_REG register description**

|             |   |
|-------------|---|
| SHub12[7:0] | Twelfth byte associated to external sensors |
|-------------|---|

### 9.52 FIFO\_STATUS1 (3Ah)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in CTRL3\_C (12h) to 1.

**Table 135. FIFO\_STATUS1 register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| DIFF_FIFO_7 | DIFF_FIFO_6 | DIFF_FIFO_5 | DIFF_FIFO_4 | DIFF_FIFO_3 | DIFF_FIFO_2 | DIFF_FIFO_1 | DIFF_FIFO_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 136. FIFO\_STATUS1 register description**

|                 |  |
|-----------------|--|
| DIFF_FIFO_[7:0] | Number of unread words (16-bit axes) stored in FIFO <sup>(1)</sup> . |
|-----------------|--|

1. For a complete number of unread samples, consider DIFF\_FIFO [11:8] in FIFO\_STATUS2 (3Bh)

### 9.53 FIFO\_STATUS2 (3Bh)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in CTRL3\_C (12h) to 1.

**Table 137. FIFO\_STATUS2 register**

|     |               |           |            |              |              |             |             |
|-----|---------------|-----------|------------|--------------|--------------|-------------|-------------|
| FTH | FIFO_OVER_RUN | FIFO_FULL | FIFO_EMPTY | DIFF_FIFO_11 | DIFF_FIFO_10 | DIFF_FIFO_9 | DIFF_FIFO_8 |
|-----|---------------|-----------|------------|--------------|--------------|-------------|-------------|

**Table 138. FIFO\_STATUS2 register description**

|                 |   |
|-----------------|---|
| FTH             | FIFO watermark status. Default value: 0<br>(0: FIFO filling is lower than watermark level <sup>(1)</sup> ;<br>1: FIFO filling is equal to or higher than the watermark level) |
| FIFO_OVER_RUN   | FIFO overrun status. Default value: 0<br>(0: FIFO is not completely filled; 1: FIFO is completely filled)   |
| FIFO_FULL       | FIFO full status. Default value: 0<br>(0: FIFO is not full; 1: FIFO will be full at the next ODR)   |
| FIFO_EMPTY      | FIFO empty bit. Default value: 0<br>(0: FIFO contains data; 1: FIFO is empty)   |
| DIFF_FIFO_[7:0] | Number of unread words (16-bit axes) stored in FIFO <sup>(2)</sup> .  |

1. FIFO watermark level is set in FTH\_[11:0] in FIFO\_CTRL1 (06h) and FIFO\_CTRL2 (07h)

2. For a complete number of unread samples, consider DIFF\_FIFO [11:8] in FIFO\_STATUS1 (3Ah)

### 9.54 FIFO\_STATUS3 (3Ch)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3\\_C \(12h\)](#) to 1.

**Table 139. FIFO\_STATUS3 register**

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| FIFO_PATTERN_7 | FIFO_PATTERN_6 | FIFO_PATTERN_5 | FIFO_PATTERN_4 | FIFO_PATTERN_3 | FIFO_PATTERN_2 | FIFO_PATTERN_1 | FIFO_PATTERN_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**Table 140. FIFO\_STATUS3 register description**

|                    |   |
|--------------------|---|
| FIFO_PATTERN_[7:0] | Word of recursive pattern read at the next reading. |
|--------------------|---|

### 9.55 FIFO\_STATUS4 (3Dh)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3\\_C \(12h\)](#) to 1.

**Table 141. FIFO\_STATUS4 register**

|                  |                  |                  |                  |                  |                  |                |                |
|------------------|------------------|------------------|------------------|------------------|------------------|----------------|----------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | FIFO_PATTERN_9 | FIFO_PATTERN_8 |
|------------------|------------------|------------------|------------------|------------------|------------------|----------------|----------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 142. FIFO\_STATUS4 register description**

|                    |   |
|--------------------|---|
| FIFO_PATTERN_[9:8] | Word of recursive pattern read at the next reading. |
|--------------------|---|

### 9.56 FIFO\_DATA\_OUT\_L (3Eh)

FIFO data output register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3\\_C \(12h\)](#) to 1.

**Table 143. FIFO\_DATA\_OUT\_L register**

|                   |                   |                   |                   |                   |                   |                   |                   |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| DATA_OUT_FIFO_L_7 | DATA_OUT_FIFO_L_6 | DATA_OUT_FIFO_L_5 | DATA_OUT_FIFO_L_4 | DATA_OUT_FIFO_L_3 | DATA_OUT_FIFO_L_2 | DATA_OUT_FIFO_L_1 | DATA_OUT_FIFO_L_0 |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|

**Table 144. FIFO\_DATA\_OUT\_L register description**

|                       |                               |
|-----------------------|-------------------------------|
| DATA_OUT_FIFO_L_[7:0] | FIFO data output (first byte) |
|-----------------------|-------------------------------|

## 9.57 FIFO\_DATA\_OUT\_H (3Fh)

FIFO data output register (r). For a proper reading of the register, it is recommended to set the BDU bit in *CTRL3\_C (12h)* to 1.

**Table 145. FIFO\_DATA\_OUT\_H register**

|                           |                           |                           |                           |                           |                           |                           |                           |
|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| DATA_<br>OUT_<br>FIFO_H_7 | DATA_<br>OUT_<br>FIFO_H_6 | DATA_<br>OUT_<br>FIFO_H_5 | DATA_<br>OUT_<br>FIFO_H_4 | DATA_<br>OUT_<br>FIFO_H_3 | DATA_<br>OUT_<br>FIFO_H_2 | DATA_<br>OUT_<br>FIFO_H_1 | DATA_<br>OUT_<br>FIFO_H_0 |
|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|

**Table 146. FIFO\_DATA\_OUT\_H register description**

|                       |                                |
|-----------------------|--------------------------------|
| DATA_OUT_FIFO_H_[7:0] | FIFO data output (second byte) |
|-----------------------|--------------------------------|

## 9.58 TIMESTAMP0\_REG (40h)

Timestamp first byte data output register (r). The value is expressed as a 24-bit word and the bit resolution is defined by setting the value in *WAKE\_UP\_DUR (5Ch)*.

**Table 147. TIMESTAMP0\_REG register**

|                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| TIMESTA<br>MP0_7 | TIMESTA<br>MP0_6 | TIMESTA<br>MP0_5 | TIMESTA<br>MP0_4 | TIMESTA<br>MP0_3 | TIMESTA<br>MP0_2 | TIMESTA<br>MP0_1 | TIMESTA<br>MP0_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

**Table 148. TIMESTAMP0\_REG register description**

|                  |                                  |
|------------------|----------------------------------|
| TIMESTAMP0_[7:0] | TIMESTAMP first byte data output |
|------------------|----------------------------------|

## 9.59 TIMESTAMP1\_REG (41h)

Timestamp second byte data output register (r). The value is expressed as a 24-bit word and the bit resolution is defined by setting value in *WAKE\_UP\_DUR (5Ch)*.

**Table 149. TIMESTAMP1\_REG register**

|                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| TIMESTA<br>MP1_7 | TIMESTA<br>MP1_6 | TIMESTA<br>MP1_5 | TIMESTA<br>MP1_4 | TIMESTA<br>MP1_3 | TIMESTA<br>MP1_2 | TIMESTA<br>MP1_1 | TIMESTA<br>MP1_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

**Table 150. TIMESTAMP1\_REG register description**

|                  |                                   |
|------------------|-----------------------------------|
| TIMESTAMP1_[7:0] | TIMESTAMP second byte data output |
|------------------|-----------------------------------|

## 9.60 TIMESTAMP2\_REG (42h)

Timestamp third byte data output register (r/w). The value is expressed as a 24-bit word and the bit resolution is defined by setting the value in *WAKE\_UP\_DUR (5Ch)*. To reset the timer, the AAh value has to be stored in this register.

**Table 151. TIMESTAMP2\_REG register**

|                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| TIMESTA<br>MP2_7 | TIMESTA<br>MP2_6 | TIMESTA<br>MP2_5 | TIMESTA<br>MP2_4 | TIMESTA<br>MP2_3 | TIMESTA<br>MP2_2 | TIMESTA<br>MP2_1 | TIMESTA<br>MP2_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

**Table 152. TIMESTAMP2\_REG register description**

|                  |                                  |
|------------------|----------------------------------|
| TIMESTAMP2_[7:0] | TIMESTAMP third byte data output |
|------------------|----------------------------------|



### 9.61 STEP\_TIMESTAMP\_L (49h)

Step counter timestamp information register (r). When a step is detected, the value of TIMESTAMP\_REG1 register is copied in STEP\_TIMESTAMP\_L.

**Table 153. STEP\_TIMESTAMP\_L register**

|                    |                    |                    |                    |                    |                    |                    |                    |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| STEP_TIMESTAMP_L_7 | STEP_TIMESTAMP_L_6 | STEP_TIMESTAMP_L_5 | STEP_TIMESTAMP_L_4 | STEP_TIMESTAMP_L_3 | STEP_TIMESTAMP_L_2 | STEP_TIMESTAMP_L_1 | STEP_TIMESTAMP_L_0 |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|

**Table 154. STEP\_TIMESTAMP\_L register description**

|                       |                                  |
|-----------------------|----------------------------------|
| STEP_TIMESTAMP_L[7:0] | Timestamp of last step detected. |
|-----------------------|----------------------------------|

### 9.62 STEP\_TIMESTAMP\_H (4Ah)

Step counter timestamp information register (r). When a step is detected, the value of TIMESTAMP\_REG2 register is copied in STEP\_TIMESTAMP\_H.

**Table 155. STEP\_TIMESTAMP\_H register**

|                    |                    |                    |                    |                    |                    |                    |                    |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| STEP_TIMESTAMP_H_7 | STEP_TIMESTAMP_H_6 | STEP_TIMESTAMP_H_5 | STEP_TIMESTAMP_H_4 | STEP_TIMESTAMP_H_3 | STEP_TIMESTAMP_H_2 | STEP_TIMESTAMP_H_1 | STEP_TIMESTAMP_H_0 |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|

**Table 156. STEP\_TIMESTAMP\_H register description**

|                       |                                  |
|-----------------------|----------------------------------|
| STEP_TIMESTAMP_H[7:0] | Timestamp of last step detected. |
|-----------------------|----------------------------------|

### 9.63 STEP\_COUNTER\_L (4Bh)

Step counter output register (r).

**Table 157. STEP\_COUNTER\_L register**

|                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| STEP_COUNTER_L_7 | STEP_COUNTER_L_6 | STEP_COUNTER_L_5 | STEP_COUNTER_L_4 | STEP_COUNTER_L_3 | STEP_COUNTER_L_2 | STEP_COUNTER_L_1 | STEP_COUNTER_L_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

**Table 158. STEP\_COUNTER\_L register description**

|                     |                              |
|---------------------|------------------------------|
| STEP_COUNTER_L[7:0] | Step counter output (LSbyte) |
|---------------------|------------------------------|

### 9.64 STEP\_COUNTER\_H (4Ch)

Step counter output register (r).

**Table 159. STEP\_COUNTER\_H register**

|                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| STEP_COUNTER_H_7 | STEP_COUNTER_H_6 | STEP_COUNTER_H_5 | STEP_COUNTER_H_4 | STEP_COUNTER_H_3 | STEP_COUNTER_H_2 | STEP_COUNTER_H_1 | STEP_COUNTER_H_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

**Table 160. STEP\_COUNTER\_H register description**

|                     |                              |
|---------------------|------------------------------|
| STEP_COUNTER_H[7:0] | Step counter output (MSbyte) |
|---------------------|------------------------------|

## 9.65 SENSORHUB13\_REG (4Dh)

Thirteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 161. SENSORHUB13\_REG register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub13_7 | SHub13_6 | SHub13_5 | SHub13_4 | SHub13_3 | SHub13_2 | SHub13_1 | SHub13_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 162. SENSORHUB13\_REG register description**

|              |  |
|--------------|--|
| SHub13_[7:0] | Thirteenth byte associated to external sensors |
|--------------|--|

## 9.66 SENSORHUB14\_REG (4Eh)

Fourteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 163. SENSORHUB14\_REG register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub14_7 | SHub14_6 | SHub14_5 | SHub14_4 | SHub14_3 | SHub14_2 | SHub14_1 | SHub14_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 164. SENSORHUB14\_REG register description**

|              |  |
|--------------|--|
| SHub14_[7:0] | Fourteenth byte associated to external sensors |
|--------------|--|

## 9.67 SENSORHUB15\_REG (4Fh)

Fifteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 165. SENSORHUB15\_REG register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub15_7 | SHub15_6 | SHub15_5 | SHub15_4 | SHub15_3 | SHub15_2 | SHub15_1 | SHub15_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 166. SENSORHUB15\_REG register description**

|              |   |
|--------------|---|
| SHub15_[7:0] | Fifteenth byte associated to external sensors |
|--------------|---|

## 9.68 SENSORHUB16\_REG (50h)

Sixteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 167. SENSORHUB16\_REG register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub16_7 | SHub16_6 | SHub16_5 | SHub16_4 | SHub16_3 | SHub16_2 | SHub16_1 | SHub16_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 168. SENSORHUB16\_REG register description**

|              |   |
|--------------|---|
| SHub16_[7:0] | Sixteenth byte associated to external sensors |
|--------------|---|

### 9.69 SENSORHUB17\_REG (51h)

Seventeenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 169. SENSORHUB17\_REG register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub17_7 | SHub17_6 | SHub17_5 | SHub17_4 | SHub17_3 | SHub17_2 | SHub17_1 | SHub17_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 170. SENSORHUB17\_REG register description**

|              |   |
|--------------|---|
| SHub17_[7:0] | Seventeenth byte associated to external sensors |
|--------------|---|

### 9.70 SENSORHUB18\_REG (52h)

Eighteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 171. SENSORHUB18\_REG register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHub18_7 | SHub18_6 | SHub18_5 | SHub18_4 | SHub18_3 | SHub18_2 | SHub18_1 | SHub18_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 172. SENSORHUB18\_REG register description**

|              |  |
|--------------|--|
| SHub18_[7:0] | Eighteenth byte associated to external sensors |
|--------------|--|

### 9.71 FUNC\_SRC (53h)

Significant motion, tilt, step detector, hard/soft-iron and sensor hub interrupt source register (r).

**Table 173. FUNC\_SRC register**

|                     |                |         |               |               |                  |           |                   |
|---------------------|----------------|---------|---------------|---------------|------------------|-----------|-------------------|
| STEP_COUNT_DELTA_IA | SIGN_MOTION_IA | TILT_IA | STEP_DETECTED | STEP_OVERFLOW | 0 <sup>(1)</sup> | SI_END_OP | SENSOR_HUB_END_OP |
|---------------------|----------------|---------|---------------|---------------|------------------|-----------|-------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 174. FUNC\_SRC register description**

|                     |   |
|---------------------|---|
| STEP_COUNT_DELTA_IA | Pedometer step recognition on delta time status. Default value: 0<br>(0: no step recognized during delta time; 1: at least one step recognized during delta time) |
| SIGN_MOTION_IA      | Significant motion event detection status. Default value: 0<br>(0: significant motion event not detected; 1: significant motion event detected)                   |
| TILT_IA             | Tilt event detection status. Default value: 0<br>(0: tilt event not detected; 1: tilt event detected)   |
| STEP_DETECTED       | Step detector event detection status. Default value: 0<br>(0: step detector event not detected; 1: step detector event detected)                                  |
| STEP_OVERFLOW       | Step counter overflow status. Default value: 0<br>(0: step counter value < 2 <sup>16</sup> ; 1: step counter value reached 2 <sup>16</sup> )                      |

**Table 174. FUNC\_SRC register description (continued)**

|                  |   |
|------------------|---|
| SI_END_OP        | Hard/soft-iron calculation status. Default value: 0<br>(0: Hard/soft-iron calculation not concluded; 1: Hard/soft-iron calculation concluded) |
| SENSORHUB_END_OP | Sensor hub communication status. Default value: 0<br>(0: sensor hub communication not concluded;<br>1: sensor hub communication concluded)    |

## 9.72 TAP\_CFG (58h)

Timestamp, pedometer, tilt, filtering, and tap recognition functions configuration register (r/w).

**Table 175. TAP\_CFG register**

|          |         |         |           |          |          |          |     |
|----------|---------|---------|-----------|----------|----------|----------|-----|
| TIMER_EN | PEDO_EN | TILT_EN | SLOPE_FDS | TAP_X_EN | TAP_Y_EN | TAP_Z_EN | LIR |
|----------|---------|---------|-----------|----------|----------|----------|-----|

**Table 176. TAP\_CFG register description**

|           |  |
|-----------|--|
| TIMER_EN  | Timestamp count enable, output data are collected in <i>TIMESTAMP0_REG (40h)</i> , <i>TIMESTAMP1_REG (41h)</i> , <i>TIMESTAMP2_REG (42h)</i> register. Default: 0<br>(0: timestamp count disabled; 1: timestamp count enabled) |
| PEDO_EN   | Pedometer algorithm enable. Default value: 0<br>(0: pedometer algorithm disabled; 1: pedometer algorithm enabled)  |
| TILT_EN   | Tilt calculation enable. Default value: 0<br>(0: tilt calculation disabled; 1: tilt calculation enabled.)  |
| SLOPE_FDS | Enable accelerometer HP and LPF2 filters (refer to <i>Figure 6</i> ). Default value: 0<br>(0: disable; 1: enable)  |
| TAP_X_EN  | Enable X direction in tap recognition. Default value: 0<br>(0: X direction disabled; 1:X direction enabled)  |
| TAP_Y_EN  | Enable Y direction in tap recognition. Default value: 0<br>(0: Y direction disabled; 1:Y direction enabled)  |
| TAP_Z_EN  | Enable Z direction in tap recognition. Default value: 0<br>(0: Z direction disabled; 1:Z direction enabled)  |
| LIR       | Latched Interrupt. Default value: 0<br>(0: interrupt request not latched; 1: interrupt request latched)  |

## 9.73 TAP\_THS\_6D (59h)

Portrait/landscape position and tap function threshold register (r/w).

**Table 177. TAP\_THS\_6D register**

|        |               |               |              |              |              |              |              |
|--------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|
| D4D_EN | SIXD_THS<br>1 | SIXD_THS<br>0 | TAP_THS<br>4 | TAP_THS<br>3 | TAP_THS<br>2 | TAP_THS<br>1 | TAP_THS<br>0 |
|--------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|

**Table 178. TAP\_THS\_6D register description**

|               |  |
|---------------|--|
| D4D_EN        | 4D orientation detection enable. Z-axis position detection is disabled.<br>Default value: 0<br>(0: enabled; 1: disabled) |
| SIXD_THS[1:0] | Threshold for D6D function. Default value: 00<br>For details, refer to <a href="#">Table 179</a> .                       |
| TAP_THS[4:0]  | Threshold for tap recognition. Default value: 00000  |

**Table 179. Threshold for D4D/D6D function**

| SIXD_THS[1:0] | Threshold value |
|---------------|-----------------|
| 00            | 80 degrees      |
| 01            | 70 degrees      |
| 10            | 60 degrees      |
| 11            | 50 degrees      |

## 9.74 INT\_DUR2 (5Ah)

Tap recognition function setting register (r/w).

**Table 180. INT\_DUR2 register**

|      |      |      |      |        |        |        |        |
|------|------|------|------|--------|--------|--------|--------|
| DUR3 | DUR2 | DUR1 | DUR0 | QUIET1 | QUIET0 | SHOCK1 | SHOCK0 |
|------|------|------|------|--------|--------|--------|--------|

**Table 181. INT\_DUR2 register description**

|            |  |
|------------|--|
| DUR[3:0]   | Duration of maximum time gap for double tap recognition. Default: 0000<br>When double tap recognition is enabled, this register expresses the maximum time between two consecutive detected taps to determine a double tap event. The default value of these bits is 0000b which corresponds to 16*ODR_XL time. If the DUR[3:0] bits are set to a different value, 1LSB corresponds to 32*ODR_XL time. |
| QUIET[1:0] | Expected quiet time after a tap detection. Default value: 00<br>Quiet time is the time after the first detected tap in which there must not be any overthreshold event. The default value of these bits is 00b which corresponds to 2*ODR_XL time. If the QUIET[1:0] bits are set to a different value, 1LSB corresponds to 4*ODR_XL time.   |
| SHOCK[1:0] | Maximum duration of overthreshold event. Default value: 00<br>Maximum duration is the maximum time of an overthreshold signal detection to be recognized as a tap event. The default value of these bits is 00b which corresponds to 4*ODR_XL time. If the SHOCK[1:0] bits are set to a different value, 1LSB corresponds to 8*ODR_XL time.  |

## 9.75 WAKE\_UP\_THS (5Bh)

Single and double-tap function threshold register (r/w).

**Table 182. WAKE\_UP\_THS register**

|                      |            |         |         |         |         |         |         |
|----------------------|------------|---------|---------|---------|---------|---------|---------|
| SINGLE_ DOUBLE_ _TAP | INACTIVITY | WK_THS5 | WK_THS4 | WK_THS3 | WK_THS2 | WK_THS1 | WK_THS0 |
|----------------------|------------|---------|---------|---------|---------|---------|---------|

**Table 183. WAKE\_UP\_THS register description**

|                   |   |
|-------------------|---|
| SINGLE_DOUBLE_TAP | Single/double-tap event enable. Default: 0<br>(0: only single-tap event enabled;<br>1: both single and double-tap events enabled) |
| INACTIVITY        | Inactivity event enable. Default value: 0<br>(0: sleep disabled; 1: sleep enabled)  |
| WK_THS[5:0]       | Threshold for wakeup. Default value: 000000   |

## 9.76 WAKE\_UP\_DUR (5Ch)

Free-fall, wakeup, timestamp and sleep mode functions duration setting register (r/w).

**Table 184. WAKE\_UP\_DUR register**

|         |            |            |           |             |             |             |             |
|---------|------------|------------|-----------|-------------|-------------|-------------|-------------|
| FF_DUR5 | WAKE_ DUR1 | WAKE_ DUR0 | TIMER_ HR | SLEEP_ DUR3 | SLEEP_ DUR2 | SLEEP_ DUR1 | SLEEP_ DUR0 |
|---------|------------|------------|-----------|-------------|-------------|-------------|-------------|

**Table 185. WAKE\_UP\_DUR register description**

|                |  |
|----------------|--|
| FF_DUR5        | Free fall duration event. Default: 0<br>For the complete configuration of the free-fall duration, refer to FF_DUR[4:0] in <a href="#">FREE_FALL (5Dh)</a> configuration. |
| WAKE_DUR[1:0]  | Wake up duration event. Default: 00<br>1LSB = 1 ODR_time   |
| TIMER_HR       | Timestamp register resolution setting <sup>(1)</sup> . Default value: 0<br>(0: 1LSB = 6.4 ms; 1: 1LSB = 25 µs)   |
| SLEEP_DUR[3:0] | Duration to go in sleep mode. Default value: 0000<br>1 LSB = 512 ODR   |

1. Configuration of this bit affects [TIMESTAMP0\\_REG \(40h\)](#), [TIMESTAMP1\\_REG \(41h\)](#), [TIMESTAMP2\\_REG \(42h\)](#), [STEP\\_TIMESTAMP\\_L \(49h\)](#), [STEP\\_TIMESTAMP\\_H \(4Ah\)](#), and [STEP\\_COUNT\\_DELTA \(15h\)](#) registers.

### 9.77 FREE\_FALL (5Dh)

Free-fall function duration setting register (r/w).

**Table 186. FREE\_FALL register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| FF_DUR4 | FF_DUR3 | FF_DUR2 | FF_DUR1 | FF_DUR0 | FF_THS2 | FF_THS1 | FF_THS0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 187. FREE\_FALL register description**

|             |   |
|-------------|---|
| FF_DUR[4:0] | Free-fall duration event. Default: 0<br>For the complete configuration of the free fall duration, refer to FF_DUR5 in <a href="#">WAKE_UP_DUR (5Ch)</a> configuration |
| FF_THS[2:0] | Free fall threshold setting. Default: 000<br>For details refer to <a href="#">Table 188</a> .   |

**Table 188. Threshold for free-fall function**

| FF_THS[2:0] | Threshold value |
|-------------|-----------------|
| 000         | 156 mg          |
| 001         | 219 mg          |
| 010         | 250 mg          |
| 011         | 312 mg          |
| 100         | 344 mg          |
| 101         | 406 mg          |
| 110         | 469 mg          |
| 111         | 500 mg          |

### 9.78 MD1\_CFG (5Eh)

Functions routing on INT1 register (r/w).

**Table 189. MD1\_CFG register**

|                  |                 |         |         |                 |         |           |            |
|------------------|-----------------|---------|---------|-----------------|---------|-----------|------------|
| INT1_INACT_STATE | INT1_SINGLE_TAP | INT1_WU | INT1_FF | INT1_DOUBLE_TAP | INT1_6D | INT1_TILT | INT1_TIMER |
|------------------|-----------------|---------|---------|-----------------|---------|-----------|------------|

**Table 190. MD1\_CFG register description**

|                  |  |
|------------------|--|
| INT1_INACT_STATE | Routing on INT1 of inactivity mode. Default: 0<br>(0: routing on INT1 of inactivity disabled; 1: routing on INT1 of inactivity enabled)                    |
| INT1_SINGLE_TAP  | Single-tap recognition routing on INT1. Default: 0<br>(0: routing of single-tap event on INT1 disabled;<br>1: routing of single-tap event on INT1 enabled) |
| INT1_WU          | Routing of wakeup event on INT1. Default value: 0<br>(0: routing of wakeup event on INT1 disabled;<br>1: routing of wakeup event on INT1 enabled)          |

**Table 190. MD1\_CFG register description**

|                 |   |
|-----------------|---|
| INT1_FF         | Routing of free-fall event on INT1. Default value: 0<br>(0: routing of free-fall event on INT1 disabled;<br>1: routing of free-fall event on INT1 enabled)  |
| INT1_DOUBLE_TAP | Routing of tap event on INT1. Default value: 0<br>(0: routing of double-tap event on INT1 disabled;<br>1: routing of double-tap event on INT1 enabled)  |
| INT1_6D         | Routing of 6D event on INT1. Default value: 0<br>(0: routing of 6D event on INT1 disabled; 1: routing of 6D event on INT1 enabled)  |
| INT1_TILT       | Routing of tilt event on INT1. Default value: 0<br>(0: routing of tilt event on INT1 disabled; 1: routing of tilt event on INT1 enabled)  |
| INT1_TIMER      | Routing of end counter event of timer on INT1. Default value: 0<br>(0: routing of end counter event of timer on INT1 disabled;<br>1: routing of end counter event of timer event on INT1 enabled) |

## 9.79 MD2\_CFG (5Fh)

Functions routing on INT2 register (r/w).

**Table 191. MD2\_CFG register**

| INT2_INACT_STATE | INT2_SINGLE_TAP | INT2_WU | INT2_FF | INT2_DOUBLE_TAP | INT2_6D | INT2_TILT | INT2_IRON |
|------------------|-----------------|---------|---------|-----------------|---------|-----------|-----------|
|------------------|-----------------|---------|---------|-----------------|---------|-----------|-----------|

**Table 192. MD2\_CFG register description**

|                  |  |
|------------------|--|
| INT2_INACT_STATE | Routing on INT2 of inactivity mode. Default: 0<br>(0: routing on INT2 of inactivity disabled; 1: routing on INT2 of inactivity enabled)  |
| INT2_SINGLE_TAP  | Single-tap recognition routing on INT2. Default: 0<br>(0: routing of single-tap event on INT2 disabled;<br>1: routing of single-tap event on INT2 enabled)   |
| INT2_WU          | Routing of wakeup event on INT2. Default value: 0<br>(0: routing of wakeup event on INT2 disabled;<br>1: routing of wake-up event on INT2 enabled)   |
| INT2_FF          | Routing of free-fall event on INT2. Default value: 0<br>(0: routing of free-fall event on INT2 disabled;<br>1: routing of free-fall event on INT2 enabled)   |
| INT2_DOUBLE_TAP  | Routing of tap event on INT2. Default value: 0<br>(0: routing of double-tap event on INT2 disabled;<br>1: routing of double-tap event on INT2 enabled)   |
| INT2_6D          | Routing of 6D event on INT2. Default value: 0<br>(0: routing of 6D event on INT2 disabled; 1: routing of 6D event on INT2 enabled)   |
| INT2_TILT        | Routing of tilt event on INT2. Default value: 0<br>(0: routing of tilt event on INT2 disabled; 1: routing of tilt event on INT2 enabled)   |
| INT2_IRON        | Routing of soft-iron/hard-iron algorithm end event on INT2. Default value: 0<br>(0: routing of soft-iron/hard-iron algorithm end event on INT2 disabled;<br>1: routing of soft-iron/hard-iron algorithm end event on INT2 enabled) |



### 9.80 OUT\_MAG\_RAW\_X\_L (66h)

External magnetometer raw data (r).

**Table 193. OUT\_MAG\_RAW\_X\_L register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 194. OUT\_MAG\_RAW\_X\_L register description**

|        |   |
|--------|---|
| D[7:0] | X-axis external magnetometer value (LSbyte) |
|--------|---|

### 9.81 OUT\_MAG\_RAW\_X\_H (67h)

External magnetometer raw data (r).

**Table 195. OUT\_MAG\_RAW\_X\_H register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 196. OUT\_MAG\_RAW\_X\_H register description**

|         |   |
|---------|---|
| D[15:8] | X-axis external magnetometer value (MSbyte) |
|---------|---|

### 9.82 OUT\_MAG\_RAW\_Y\_L (68h)

External magnetometer raw data (r).

**Table 197. OUT\_MAG\_RAW\_Y\_L register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 198. OUT\_MAG\_RAW\_Y\_L register description**

|        |   |
|--------|---|
| D[7:0] | Y-axis external magnetometer value (LSbyte) |
|--------|---|

### 9.83 OUT\_MAG\_RAW\_Y\_H (69h)

External magnetometer raw data (r).

**Table 199. OUT\_MAG\_RAW\_Y\_H register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 200. OUT\_MAG\_RAW\_Y\_H register description**

|         |   |
|---------|---|
| D[15:8] | Y-axis external magnetometer value (MSbyte) |
|---------|---|

**9.84 OUT\_MAG\_RAW\_Z\_L (6Ah)**

External magnetometer raw data (r).

**Table 201. OUT\_MAG\_RAW\_Z\_L register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 202. OUT\_MAG\_RAW\_Z\_L register description**

|        |   |
|--------|---|
| D[7:0] | Z-axis external magnetometer value (LSbyte) |
|--------|---|

**9.85 OUT\_MAG\_RAW\_Z\_H (6Bh)**

External magnetometer raw data (r).

**Table 203. OUT\_MAG\_RAW\_Z\_H register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 204. OUT\_MAG\_RAW\_Z\_H register description**

|         |   |
|---------|---|
| D[15:8] | Z-axis external magnetometer value (MSbyte) |
|---------|---|

## 10 Embedded functions register mapping

The table given below provides a list of the registers for the embedded functions available in the device and the corresponding addresses. Embedded functions registers are accessible when FUNC\_CFG\_EN is set to '1' in [FUNC\\_CFG\\_ACCESS \(01h\)](#).

*Note:* All modifications of the content of the embedded functions registers have to be performed with the device in power-down mode.

**Table 205. Registers address map - embedded functions**

| Name                        | Type | Register address |           | Default  | Comment  |
|-----------------------------|------|------------------|-----------|----------|----------|
|                             |      | Hex              | Binary    |          |          |
| SLV0_ADD                    | r/w  | 02               | 00000010  | 00000000 |          |
| SLV0_SUBADD                 | r/w  | 03               | 00000011  | 00000000 |          |
| SLAVE0_CONFIG               | r/w  | 04               | 00000100  | 00000000 |          |
| SLV1_ADD                    | r/w  | 05               | 00000101  | 00000000 |          |
| SLV1_SUBADD                 | r/w  | 06               | 00000110  | 00000000 |          |
| SLAVE1_CONFIG               | r/w  | 07               | 00000111  | 00000000 |          |
| SLV2_ADD                    | r/w  | 08               | 00001000  | 00000000 |          |
| SLV2_SUBADD                 | r/w  | 09               | 00001001  | 00000000 |          |
| SLAVE2_CONFIG               | r/w  | 0A               | 00001010  | 00000000 |          |
| SLV3_ADD                    | r/w  | 0B               | 00001011  | 00000000 |          |
| SLV3_SUBADD                 | r/w  | 0C               | 00001100  | 00000000 |          |
| SLAVE3_CONFIG               | r/w  | 0D               | 00001101  | 00000000 |          |
| DATAWRITE_SRC_MODE_SUB_SLV0 | r/w  | 0E               | 00001110  | 00000000 |          |
| PEDO_THS_REG                | r/w  | 0F               | 00001111  | 00010000 |          |
| RESERVED                    | -    | 10-12            |           | -        | Reserved |
| SM_THS                      | r/w  | 13               | 00010011  | 00000110 |          |
| PEDO_DEB_REG                | r/w  | 14               | 00010100  | 01101110 |          |
| STEP_COUNT_DELTA            | r/w  | 15               | 0001 0101 | 00000000 |          |
| MAG_SI_XX                   | r/w  | 24               | 00100100  | 00001000 |          |
| MAG_SI_XY                   | r/w  | 25               | 00100101  | 00000000 |          |
| MAG_SI_XZ                   | r/w  | 26               | 00100110  | 00000000 |          |
| MAG_SI_YX                   | r/w  | 27               | 00100111  | 00000000 |          |
| MAG_SI_YY                   | r/w  | 28               | 00101000  | 00001000 |          |
| MAG_SI_YZ                   | r/w  | 29               | 00101001  | 00000000 |          |
| MAG_SI_ZX                   | r/w  | 2A               | 00101010  | 00000000 |          |
| MAG_SI_ZY                   | r/w  | 2B               | 00101011  | 00000000 |          |

**Table 205. Registers address map - embedded functions (continued)**

| Name       | Type | Register address |          | Default  | Comment |
|------------|------|------------------|----------|----------|---------|
|            |      | Hex              | Binary   |          |         |
| MAG_SI_ZZ  | r/w  | 2C               | 00101100 | 00001000 |         |
| MAG_OFFX_L | r/w  | 2D               | 00101101 | 00000000 |         |
| MAG_OFFX_H | r/w  | 2E               | 00101110 | 00000000 |         |
| MAG_OFFY_L | r/w  | 2F               | 00101111 | 00000000 |         |
| MAG_OFFY_H | r/w  | 30               | 00110000 | 00000000 |         |
| MAG_OFFZ_L | r/w  | 31               | 00110001 | 00000000 |         |
| MAG_OFFZ_H | r/w  | 32               | 00110010 | 00000000 |         |

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

## 11 Embedded functions registers description

*Note:* All modifications of the content of the embedded functions registers have to be performed with the device in power-down mode.

### 11.1 SLV0\_ADD (02h)

I<sup>2</sup>C slave address of the first external sensor (Sensor1) register (r/w).

**Table 206. SLV0\_ADD register**

|             |             |             |             |             |             |             |      |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------|
| Slave0_add6 | Slave0_add5 | Slave0_add4 | Slave0_add3 | Slave0_add2 | Slave0_add1 | Slave0_add0 | rw_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------|

**Table 207. SLV0\_ADD register description**

|                 |   |
|-----------------|---|
| Slave0_add[6:0] | I <sup>2</sup> C slave address of Sensor1 that can be read by sensor hub.<br>Default value: 0000000 |
| rw_0            | Read/write operation on Sensor1. Default value: 0<br>(0: write operation; 1: read operation)        |

### 11.2 SLV0\_SUBADD (03h)

Address of register on the first external sensor (Sensor1) register (r/w).

**Table 208. SLV0\_SUBADD register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Slave0_reg7 | Slave0_reg6 | Slave0_reg5 | Slave0_reg4 | Slave0_reg3 | Slave0_reg2 | Slave0_reg1 | Slave0_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 209. SLV0\_SUBADD register description**

|                 |  |
|-----------------|--|
| Slave0_reg[7:0] | Address of register on Sensor1 that has to be read/write according to the rw_0 bit value in <a href="#">SLV0_ADD (02h)</a> . Default value: 00000000 |
|-----------------|--|

### 11.3 SLAVE0\_CONFIG (04h)

First external sensor (Sensor1) configuration and sensor hub settings register (r/w).

**Table 210. SLAVE0\_CONFIG register**

|              |              |              |              |          |               |               |               |
|--------------|--------------|--------------|--------------|----------|---------------|---------------|---------------|
| Slave0_rate1 | Slave0_rate0 | Aux_sens_on1 | Aux_sens_on0 | Src_mode | Slave0_numop2 | Slave0_numop1 | Slave0_numop0 |
|--------------|--------------|--------------|--------------|----------|---------------|---------------|---------------|

**Table 211. SLAVE0\_CONFIG register description**

|                   |   |
|-------------------|---|
| Slave0_rate[1:0]  | Decimation of read operation on Sensor1 starting from the sensor hub trigger.<br>Default value: 00<br>(00: no decimation<br>01: update every 2 samples<br>10: update every 4 samples<br>11: update every 8 samples) |
| Aux_sens_on[1:0]  | Number of external sensors to be read by sensor hub. Default value: 00<br>(00: one sensor<br>01: two sensors<br>10: three sensors<br>11: four sensors)  |
| Src_mode          | Source mode conditioned read <sup>(1)</sup> . Default value: 0<br>(0: source mode read disabled; 1: source mode read enabled)   |
| Slave0_numop[2:0] | Number of read operations on Sensor1.   |

1. Read conditioned by the content of the register at address specified in *DATAWRITE\_SRC\_MODE\_SUB\_SLV0 (0Eh)* register. If the content is non-zero the operation continues with the reading of the address specified in the *SLV0\_SUBADD (03h)* register, else the operation is interrupted.

### 11.4 SLV1\_ADD (05h)

I<sup>2</sup>C slave address of the second external sensor (Sensor2) register (r/w).

**Table 212. SLV1\_ADD register**

|             |             |             |             |             |             |             |     |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|
| Slave1_add6 | Slave1_add5 | Slave1_add4 | Slave1_add3 | Slave1_add2 | Slave1_add1 | Slave1_add0 | r_1 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|

**Table 213. SLV1\_ADD register description**

|                 |   |
|-----------------|---|
| Slave1_add[6:0] | I <sup>2</sup> C slave address of Sensor2 that can be read by sensor hub.<br>Default value: 0000000           |
| r_1             | Read operation on Sensor2 enable. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

### 11.5 SLV1\_SUBADD (06h)

Address of register on the second external sensor (Sensor2) register (r/w).

**Table 214. SLV1\_SUBADD register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Slave1_reg7 | Slave1_reg6 | Slave1_reg5 | Slave1_reg4 | Slave1_reg3 | Slave1_reg2 | Slave1_reg1 | Slave1_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 215. SLV1\_SUBADD register description**

|                 |  |
|-----------------|--|
| Slave1_reg[7:0] | Address of register on Sensor2 that has to be read according to the r_1 bit value in <i>SLV1_ADD (05h)</i> . Default value: 00000000 |
|-----------------|--|

### 11.6 SLAVE1\_CONFIG (07h)

Second external sensor (Sensor2) configuration register (r/w).

**Table 216. SLAVE1\_CONFIG register**

|              |              |                  |                  |                  |               |               |               |
|--------------|--------------|------------------|------------------|------------------|---------------|---------------|---------------|
| Slave1_rate1 | Slave1_rate0 | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | Slave1_numop2 | Slave1_numop1 | Slave1_numop0 |
|--------------|--------------|------------------|------------------|------------------|---------------|---------------|---------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 217. SLAVE1\_CONFIG register description**

|                   |   |
|-------------------|---|
| Slave1_rate[1:0]  | Decimation of read operation on Sensor2 starting from the sensor hub trigger.<br>Default value: 00<br>(00: no decimation<br>01: update every 2 samples<br>10: update every 4 samples<br>11: update every 8 samples) |
| Slave1_numop[2:0] | Number of read operations on Sensor2.   |

### 11.7 SLV2\_ADD (08h)

I<sup>2</sup>C slave address of the third external sensor (Sensor3) register (r/w).

**Table 218. SLV2\_ADD register**

|             |             |             |             |             |             |             |     |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|
| Slave2_add6 | Slave2_add5 | Slave2_add4 | Slave2_add3 | Slave2_add2 | Slave2_add1 | Slave2_add0 | r_2 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|

**Table 219. SLV2\_ADD register description**

|                 |   |
|-----------------|---|
| Slave2_add[6:0] | I <sup>2</sup> C slave address of Sensor3 that can be read by sensor hub.<br>Default value: 0000000           |
| r_2             | Read operation on Sensor3 enable. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

### 11.8 SLV2\_SUBADD (09h)

Address of register on the third external sensor (Sensor3) register (r/w).

**Table 220. SLV2\_SUBADD register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Slave2_reg7 | Slave2_reg6 | Slave2_reg5 | Slave2_reg4 | Slave2_reg3 | Slave2_reg2 | Slave2_reg1 | Slave2_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 221. SLV2\_SUBADD register description**

|                 |  |
|-----------------|--|
| Slave2_reg[7:0] | Address of register on Sensor3 that has to be read according to the r_2 bit value in <i>SLV2_ADD (08h)</i> . Default value: 00000000 |
|-----------------|--|

### 11.9 SLAVE2\_CONFIG (0Ah)

Third external sensor (Sensor3) configuration register (r/w).

**Table 222. SLAVE2\_CONFIG register**

|              |              |                  |                  |                  |               |               |               |
|--------------|--------------|------------------|------------------|------------------|---------------|---------------|---------------|
| Slave2_rate1 | Slave2_rate0 | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | Slave2_numop2 | Slave2_numop1 | Slave2_numop0 |
|--------------|--------------|------------------|------------------|------------------|---------------|---------------|---------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 223. SLAVE2\_CONFIG register description**

|                   |   |
|-------------------|---|
| Slave2_rate[1:0]  | Decimation of read operation on Sensor3 starting from the sensor hub trigger.<br>Default value: 00<br>(00: no decimation<br>01: update every 2 samples<br>10: update every 4 samples<br>11: update every 8 samples) |
| Slave2_numop[2:0] | Number of read operations on Sensor3.   |

### 11.10 SLV3\_ADD (0Bh)

I<sup>2</sup>C slave address of the fourth external sensor (Sensor4) register (r/w).

**Table 224. SLV3\_ADD register**

|             |             |             |             |             |             |             |     |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|
| Slave3_add6 | Slave3_add5 | Slave3_add4 | Slave3_add3 | Slave3_add2 | Slave3_add1 | Slave3_add0 | r_3 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|

**Table 225. SLV3\_ADD register description**

|                 |   |
|-----------------|---|
| Slave3_add[6:0] | I <sup>2</sup> C slave address of Sensor4 that can be read by the sensor hub.<br>Default value: 0000000       |
| r_3             | Read operation on Sensor4 enable. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

### 11.11 SLV3\_SUBADD (0Ch)

Address of register on the fourth external sensor (Sensor4) register (r/w).

**Table 226. SLV3\_SUBADD register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Slave3_reg7 | Slave3_reg6 | Slave3_reg5 | Slave3_reg4 | Slave3_reg3 | Slave3_reg2 | Slave3_reg1 | Slave3_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 227. SLV3\_SUBADD register description**

|                 |  |
|-----------------|--|
| Slave3_reg[7:0] | Address of register on Sensor4 that has to be read according to the r_3 bit value in <i>SLV3_ADD (0Bh)</i> . Default value: 00000000 |
|-----------------|--|



## 11.12 SLAVE3\_CONFIG (0Dh)

Fourth external sensor (Sensor4) configuration register (r/w).

**Table 228. SLAVE3\_CONFIG register**

|              |              |                  |                  |                  |               |               |               |
|--------------|--------------|------------------|------------------|------------------|---------------|---------------|---------------|
| Slave3_rate1 | Slave3_rate0 | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | Slave3_numop2 | Slave3_numop1 | Slave3_numop0 |
|--------------|--------------|------------------|------------------|------------------|---------------|---------------|---------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 229. SLAVE3\_CONFIG register description**

|                   |   |
|-------------------|---|
| Slave3_rate[1:0]  | Decimation of read operation on Sensor4 starting from the sensor hub trigger.<br>Default value: 00<br>(00: no decimation<br>01: update every 2 samples<br>10: update every 4 samples<br>11: update every 8 samples) |
| Slave3_numop[2:0] | Number of read operations on Sensor4.   |

## 11.13 DATAWRITE\_SRC\_MODE\_SUB\_SLV0 (0Eh)

Data to be written into the slave device register (r/w).

**Table 230. DATAWRITE\_SRC\_MODE\_SUB\_SLV0 register**

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Slave_dataw7 | Slave_dataw6 | Slave_dataw5 | Slave_dataw4 | Slave_dataw3 | Slave_dataw2 | Slave_dataw1 | Slave_dataw0 |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

**Table 231. DATAWRITE\_SRC\_MODE\_SUB\_SLV0 register description**

|                  |  |
|------------------|--|
| Slave_dataw[7:0] | Data to be written into the slave device according to the rw_0 bit in <a href="#">SLV0_ADD (02h)</a> register or address to be read in source mode.<br>Default value: 00000000 |
|------------------|--|

### 11.14 PEDO\_THS\_REG (0Fh)

Pedometer minimum threshold and internal full-scale configuration register (r/w).

**Table 232. PEDO\_THS\_REG register default values**

|         |   |   |          |          |          |          |          |
|---------|---|---|----------|----------|----------|----------|----------|
| PEDO_4G | - | - | THS_MIN4 | THS_MIN3 | THS_MIN2 | THS_MIN1 | THS_MIN0 |
|---------|---|---|----------|----------|----------|----------|----------|

**Table 233. PEDO\_THS\_REG register description**

|              |   |
|--------------|---|
| PEDO_4G      | This bit sets the internal full scale used in pedometer functions. Using this bit, saturation is avoided (e.g. FAST walk).<br>0: internal full scale = 2 g.<br>1: internal full scale 4 g (device full_scale @CTRL1_XL must be ≥ 4 g, otherwise internal full scale is 2 g) |
| THS_MIN[4:0] | Configurable minimum threshold. 1LSB = 16 mg @PEDO_4G=0, 1LSB = 32 mg @PEDO_4G=1  |

### 11.15 SM\_THS (13h)

Significant motion configuration register (r/w).

**Table 234. SM\_THS register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SM_THS_7 | SM_THS_6 | SM_THS_5 | SM_THS_4 | SM_THS_3 | SM_THS_2 | SM_THS_1 | SM_THS_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 235. SM\_THS register description**

|             |  |
|-------------|--|
| SM_THS[7:0] | Significant motion threshold. Default value: 0000110 |
|-------------|--|

### 11.16 PEDO\_DEB\_REG (14h)

Pedometer debounce configuration register (r/w).

**Table 236. PEDO\_DEB\_REG register default values**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| DEB_TIME4 | DEB_TIME3 | DEB_TIME2 | DEB_TIME1 | DEB_TIME0 | DEB_STEP2 | DEB_STEP1 | DEB_STEP0 |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

**Table 237. PEDO\_DEB\_REG register description**

|               |  |
|---------------|--|
| DEB_TIME[4:0] | Debounce time. If the time between two consecutive steps is greater than DEB_TIME*80ms, the debouncer is reactivated. Default value: 01101 |
| DEB_STEP[2:0] | Debounce threshold. Minimum number of steps to increment the step counter (debounce). Default value: 110                                   |

### 11.17 STEP\_COUNT\_DELTA (15h)

Time period register for step detection on delta time (r/w).

**Table 238. STEP\_COUNT\_DELTA register**

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| SC_<br>DELTA_7 | SC_<br>DELTA_6 | SC_<br>DELTA_5 | SC_<br>DELTA_4 | SC_<br>DELTA_3 | SC_<br>DELTA_2 | SC_<br>DELTA_1 | SC_<br>DELTA_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**Table 239. STEP\_COUNT\_DELTA register description**

|               |  |
|---------------|--|
| SC_DELTA[7:0] | Time period value <sup>(1)</sup> (1LSB = 1.6384 s) |
|---------------|--|

1. This value is effective if the TIMER\_EN bit of the *TAP\_CFG (58h)* register is set to 1 and the TIMER\_HR bit of the *WAKE\_UP\_DUR (5Ch)* register is set to 0.

### 11.18 MAG\_SI\_XX (24h)

Soft-iron matrix correction register (r/w).

**Table 240. MAG\_SI\_XX register**

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| MAG_SI_<br>XX_7 | MAG_SI_<br>XX_6 | MAG_SI_<br>XX_5 | MAG_SI_<br>XX_4 | MAG_SI_<br>XX_3 | MAG_SI_<br>XX_2 | MAG_SI_<br>XX_1 | MAG_SI_<br>XX_0 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

**Table 241. MAG\_SI\_XX register description**

|                 |   |
|-----------------|---|
| MAG_SI_XX_[7:0] | Soft-iron correction row1 col1 coefficient <sup>(1)</sup> . Default value: 00001000 |
|-----------------|---|

1. Value is expressed in sign-module format.

### 11.19 MAG\_SI\_XY (25h)

Soft-iron matrix correction register (r/w).

**Table 242. MAG\_SI\_XY register**

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| MAG_SI_<br>XY_7 | MAG_SI_<br>XY_6 | MAG_SI_<br>XY_5 | MAG_SI_<br>XY_4 | MAG_SI_<br>XY_3 | MAG_SI_<br>XY_2 | MAG_SI_<br>XY_1 | MAG_SI_<br>XY_0 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

**Table 243. MAG\_SI\_XY register description**

|                 |   |
|-----------------|---|
| MAG_SI_XY_[7:0] | Soft-iron correction row1 col2 coefficient <sup>(1)</sup> . Default value: 00000000 |
|-----------------|---|

1. Value is expressed in sign-module format.

### 11.20 MAG\_SI\_XZ (26h)

Soft-iron matrix correction register (r/w).

**Table 244. MAG\_SI\_XZ register**

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| MAG_SI_<br>XZ_7 | MAG_SI_<br>XZ_6 | MAG_SI_<br>XZ_5 | MAG_SI_<br>XZ_4 | MAG_SI_<br>XZ_3 | MAG_SI_<br>XZ_2 | MAG_SI_<br>XZ_1 | MAG_SI_<br>XZ_0 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

**Table 245. MAG\_SI\_XZ register description**

|                 |   |
|-----------------|---|
| MAG_SI_XZ_[7:0] | Soft-iron correction row1 col3 coefficient <sup>(1)</sup> . Default value: 00000000 |
|-----------------|---|

1. Value is expressed in sign-module format.

### 11.21 MAG\_SI\_YX (27h)

Soft-iron matrix correction register (r/w).

**Table 246. MAG\_SI\_YX register**

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| MAG_SI_<br>YX_7 | MAG_SI_<br>YX_6 | MAG_SI_<br>YX_5 | MAG_SI_<br>YX_4 | MAG_SI_<br>YX_3 | MAG_SI_<br>YX_2 | MAG_SI_<br>YX_1 | MAG_SI_<br>YX_0 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

**Table 247. MAG\_SI\_YX register description**

|                 |   |
|-----------------|---|
| MAG_SI_YX_[7:0] | Soft-iron correction row2 col1 coefficient <sup>(1)</sup> . Default value: 00000000 |
|-----------------|---|

1. Value is expressed in sign-module format.

### 11.22 MAG\_SI\_YY (28h)

Soft-iron matrix correction register (r/w).

**Table 248. MAG\_SI\_YY register**

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| MAG_SI_<br>YY_7 | MAG_SI_<br>YY_6 | MAG_SI_<br>YY_5 | MAG_SI_<br>YY_4 | MAG_SI_<br>YY_3 | MAG_SI_<br>YY_2 | MAG_SI_<br>YY_1 | MAG_SI_<br>YY_0 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

**Table 249. MAG\_SI\_YY register description**

|                 |   |
|-----------------|---|
| MAG_SI_YY_[7:0] | Soft-iron correction row2 col2 coefficient <sup>(1)</sup> . Default value: 00001000 |
|-----------------|---|

1. Value is expressed in sign-module format.

### 11.23 MAG\_SI\_YZ (29h)

Soft-iron matrix correction register (r/w).

**Table 250. MAG\_SI\_YZ register**

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| MAG_SI_<br>YZ_7 | MAG_SI_<br>YZ_6 | MAG_SI_<br>YZ_5 | MAG_SI_<br>YZ_4 | MAG_SI_<br>YZ_3 | MAG_SI_<br>YZ_2 | MAG_SI_<br>YZ_1 | MAG_SI_<br>YZ_0 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

**Table 251. MAG\_SI\_YZ register description**

|                 |   |
|-----------------|---|
| MAG_SI_YZ_[7:0] | Soft-iron correction row2 col3 coefficient <sup>(1)</sup> . Default value: 00000000 |
|-----------------|---|

1. Value is expressed in sign-module format.

### 11.24 MAG\_SI\_ZX (2Ah)

Soft-iron matrix correction register (r/w).

**Table 252. MAG\_SI\_ZX register**

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| MAG_SI_<br>ZX_7 | MAG_SI_<br>ZX_6 | MAG_SI_<br>ZX_5 | MAG_SI_<br>ZX_4 | MAG_SI_<br>ZX_3 | MAG_SI_<br>ZX_2 | MAG_SI_<br>ZX_1 | MAG_SI_<br>ZX_0 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

**Table 253. MAG\_SI\_ZX register description**

|                 |   |
|-----------------|---|
| MAG_SI_ZX_[7:0] | Soft-iron correction row3 col1 coefficient <sup>(1)</sup> . Default value: 00000000 |
|-----------------|---|

1. Value is expressed in sign-module format.

### 11.25 MAG\_SI\_ZY (2Bh)

Soft-iron matrix correction register (r/w).

**Table 254. MAG\_SI\_ZY register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_ZY_7 | MAG_SI_ZY_6 | MAG_SI_ZY_5 | MAG_SI_ZY_4 | MAG_SI_ZY_3 | MAG_SI_ZY_2 | MAG_SI_ZY_1 | MAG_SI_ZY_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 255. MAG\_SI\_ZY register description**

|                 |   |
|-----------------|---|
| MAG_SI_ZY_[7:0] | Soft-iron correction row3 col2 coefficient <sup>(1)</sup> . Default value: 00000000 |
|-----------------|---|

1. Value is expressed in sign-module format.

### 11.26 MAG\_SI\_ZZ (2Ch)

Soft-iron matrix correction register (r/w).

**Table 256. MAG\_SI\_ZZ register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_ZZ_7 | MAG_SI_ZZ_6 | MAG_SI_ZZ_5 | MAG_SI_ZZ_4 | MAG_SI_ZZ_3 | MAG_SI_ZZ_2 | MAG_SI_ZZ_1 | MAG_SI_ZZ_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 257. MAG\_SI\_ZZ register description**

|                 |   |
|-----------------|---|
| MAG_SI_ZZ_[7:0] | Soft-iron correction row3 col3 coefficient <sup>(1)</sup> . Default value: 00001000 |
|-----------------|---|

1. Value is expressed in sign-module format.

### 11.27 MAG\_OFFX\_L (2Dh)

Offset for X-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

**Table 258. MAG\_OFFX\_L register**

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| MAG_OFFX_L_7 | MAG_OFFX_L_6 | MAG_OFFX_L_5 | MAG_OFFX_L_4 | MAG_OFFX_L_3 | MAG_OFFX_L_2 | MAG_OFFX_L_1 | MAG_OFFX_L_0 |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

**Table 259. MAG\_OFFX\_L register description**

|                  |   |
|------------------|---|
| MAG_OFFX_L_[7:0] | Offset for X-axis hard-iron compensation. Default value: 00000000 |
|------------------|---|

### 11.28 MAG\_OFFX\_H (2Eh)

Offset for X-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

**Table 260. MAG\_OFFX\_H register**

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| MAG_OFFX_H_7 | MAG_OFFX_H_6 | MAG_OFFX_H_5 | MAG_OFFX_H_4 | MAG_OFFX_H_3 | MAG_OFFX_H_2 | MAG_OFFX_H_1 | MAG_OFFX_H_0 |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

**Table 261. MAG\_OFFX\_H register description**

|                  |   |
|------------------|---|
| MAG_OFFX_H_[7:0] | Offset for X-axis hard-iron compensation. Default value: 00000000 |
|------------------|---|

### 11.29 MAG\_OFFY\_L (2Fh)

Offset for Y-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

**Table 262. MAG\_OFFY\_L register**

|                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| MAG_OFF<br>Y_L_7 | MAG_OFF<br>Y_L_6 | MAG_OFF<br>Y_L_5 | MAG_OFF<br>Y_L_4 | MAG_OFF<br>Y_L_3 | MAG_OFF<br>Y_L_2 | MAG_OFF<br>Y_L_1 | MAG_OFF<br>Y_L_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

**Table 263. MAG\_OFFY\_L register description**

|                 |   |
|-----------------|---|
| MAG_OFFY_L[7:0] | Offset for Y-axis hard-iron compensation. Default value: 00000000 |
|-----------------|---|

### 11.30 MAG\_OFFY\_H (30h)

Offset for Y-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

**Table 264. MAG\_OFFY\_H register**

|                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| MAG_OFF<br>Y_H_7 | MAG_OFF<br>Y_H_6 | MAG_OFF<br>Y_H_5 | MAG_OFF<br>Y_H_4 | MAG_OFF<br>Y_H_3 | MAG_OFF<br>Y_H_2 | MAG_OFF<br>Y_H_1 | MAG_OFF<br>Y_H_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

**Table 265. MAG\_OFFY\_H register description**

|                 |   |
|-----------------|---|
| MAG_OFFY_H[7:0] | Offset for Y-axis hard-iron compensation. Default value: 00000000 |
|-----------------|---|

### 11.31 MAG\_OFFZ\_L (31h)

Offset for Z-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

**Table 266. MAG\_OFFZ\_L register**

|                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| MAG_OFF<br>Z_L_7 | MAG_OFF<br>Z_L_6 | MAG_OFF<br>Z_L_5 | MAG_OFF<br>Z_L_4 | MAG_OFF<br>Z_L_3 | MAG_OFF<br>Z_L_2 | MAG_OFF<br>Z_L_1 | MAG_OFF<br>Z_L_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

**Table 267. MAG\_OFFZ\_L register description**

|                 |   |
|-----------------|---|
| MAG_OFFZ_L[7:0] | Offset for Z-axis hard-iron compensation. Default value: 00000000 |
|-----------------|---|

### 11.32 MAG\_OFFZ\_H (32h)

Offset for Z-axis hard-iron compensation register (r/w). The value is expressed as a 16-bit word in two's complement.

**Table 268. MAG\_OFFZ\_H register**

|                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| MAG_OFF<br>Z_H_7 | MAG_OFF<br>Z_H_6 | MAG_OFF<br>Z_H_5 | MAG_OFF<br>Z_H_4 | MAG_OFF<br>Z_H_3 | MAG_OFF<br>Z_H_2 | MAG_OFF<br>Z_H_1 | MAG_OFF<br>Z_H_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

**Table 269. MAG\_OFFZ\_H register description**

|                 |   |
|-----------------|---|
| MAG_OFFZ_H[7:0] | Offset for Z-axis hard-iron compensation. Default value: 00000000 |
|-----------------|---|

## 12 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and "Green" standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave "Pin 1 Indicator" unconnected during soldering.

Land pattern and soldering recommendations are available at [www.st.com/mems](http://www.st.com/mems).





### 13.2 LGA-14 package information

Figure 17. Carrier tape information for LGA-14 package

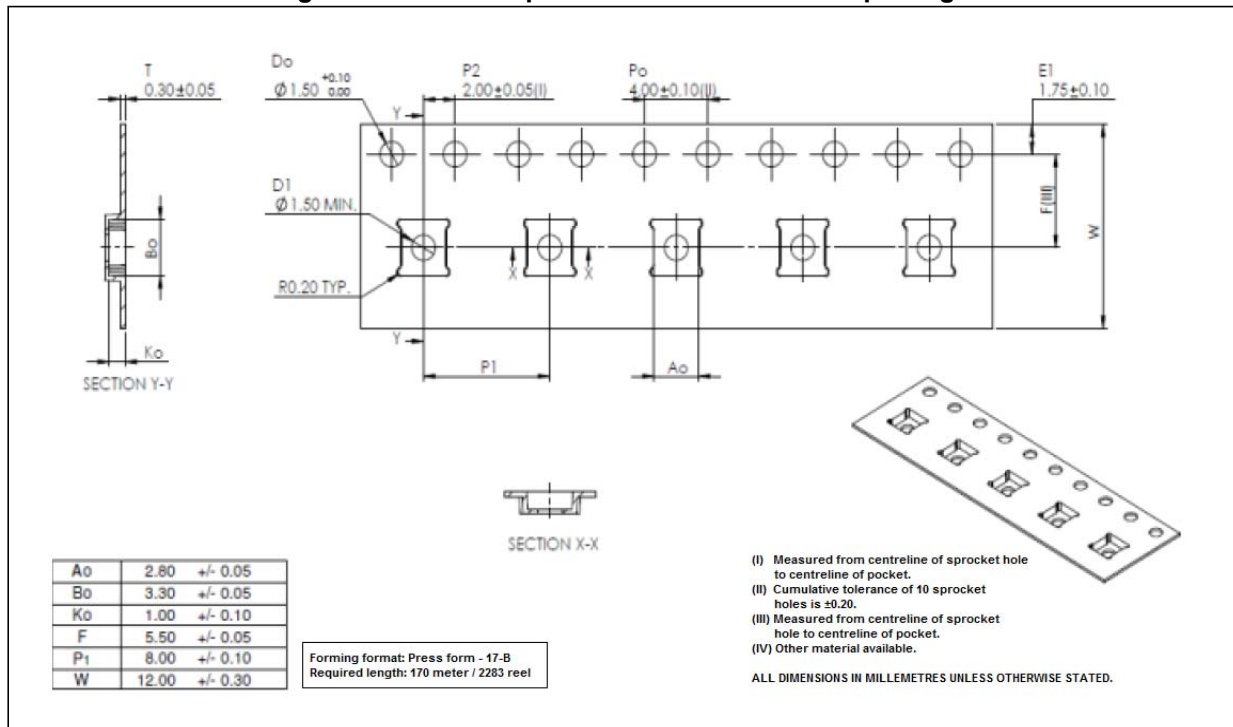


Figure 18. LGA-14 package orientation in carrier tape

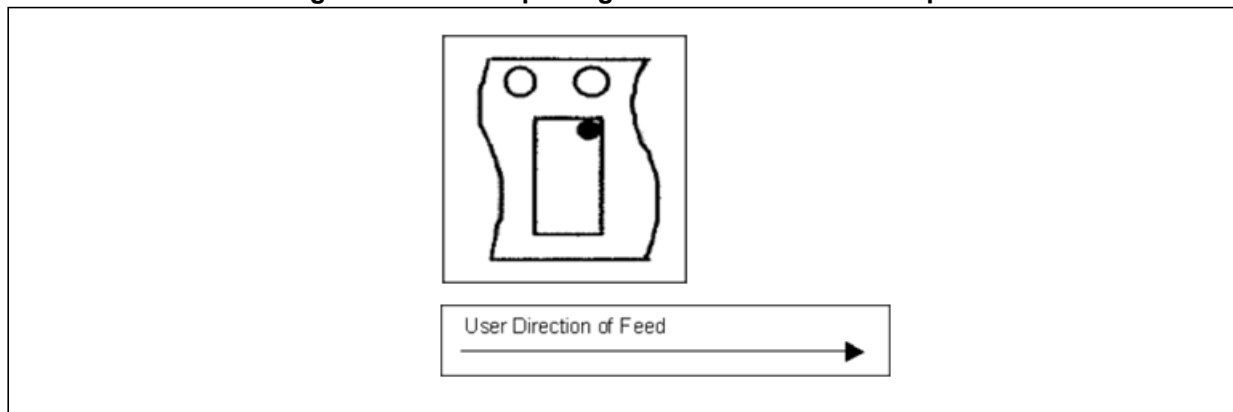


Figure 19. Reel information for carrier tape of LGA-14 package

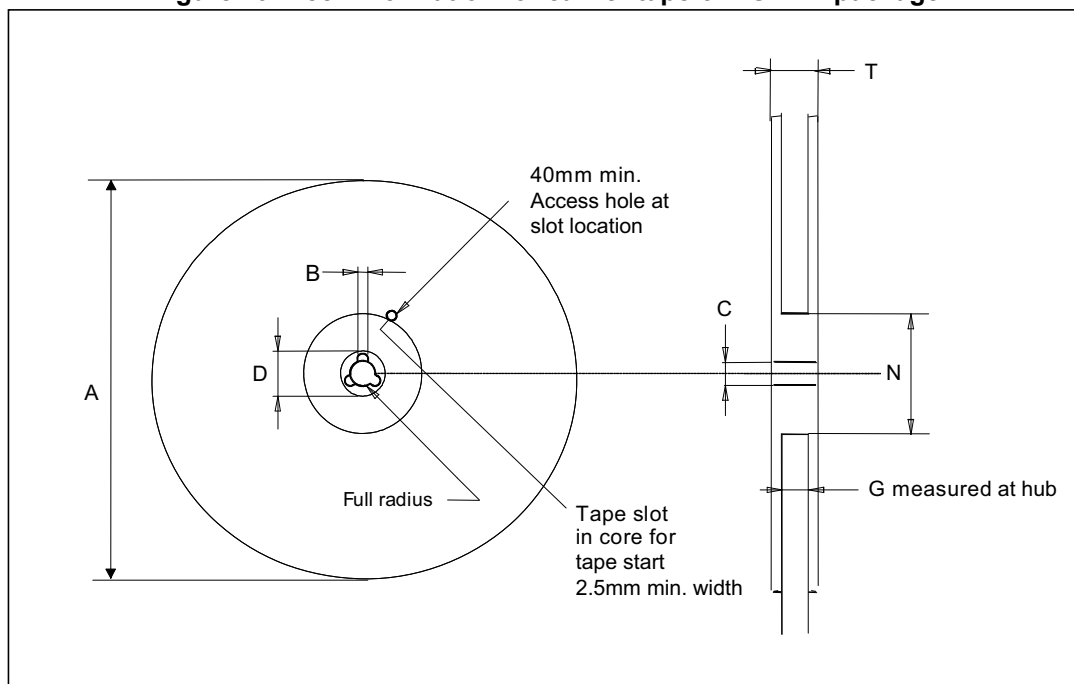


Table 270. Reel dimensions for carrier tape of LGA-14 package

| Reel dimensions (mm) |            |
|----------------------|------------|
| A (max)              | 330        |
| B (min)              | 1.5        |
| C                    | 13 ±0.25   |
| D (min)              | 20.2       |
| N (min)              | 60         |
| G                    | 12.4 +2/-0 |
| T (max)              | 18.4       |

## 14 Revision history

**Table 271. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 03-Nov-2014 | 1        | Initial release  |
| 18-Dec-2014 | 2        | Updated <a href="#">Section 2: Embedded low-power features</a> and subsection<br>Updated <a href="#">Section 5.4: FIFO</a> and subsections<br>Added <a href="#">Section 5.4.7: Filter block diagrams</a><br>Updated IddLP in <a href="#">Table 4</a> and TODR in <a href="#">Table 5: Temperature sensor characteristics</a><br>Updated <a href="#">Table 16: Registers address map</a><br>Revised registers in <a href="#">Section 9: Register description</a><br>Updated <a href="#">Table 205: Registers address map - embedded functions</a><br>Revised registers in <a href="#">Section 11: Embedded functions registers description</a><br>Textual update in <a href="#">Figure 16: LGA-14 2.5x3x0.86 mm 14L package outline and mechanical data</a> |
| 05-Mar-2015 | 3        | Document status promoted from preliminary to production data<br>Updated bit 0 in <a href="#">Section 9.79: MD2_CFG (5Fh)</a>   |
| 23-Apr-2015 | 4        | Updated Vdd_IO (max) in <a href="#">Table 4: Electrical characteristics</a><br>Added D4D_EN bit to <a href="#">Section 9.73: TAP_THS_6D (59h)</a><br>Updated <a href="#">Table 181: INT-DUR2 register description</a>  |
| 06-May-2015 | 5        | Updated direction of rotation of Y-axis in <a href="#">Figure 1: Pin connections</a><br>Updated <a href="#">Table 68: Accelerometer slope and high-pass filter selection and cutoff frequency</a>  |
| 16-Jul-2015 | 6        | Updated chamfer of pin 1 indicator in <a href="#">Figure 1</a> , <a href="#">Figure 13</a> , <a href="#">Figure 14</a> , <a href="#">Figure 15</a><br>Added footnote 2 to <a href="#">Table 3: Mechanical characteristics</a><br>Updated recommendation to set BDU bit to 1 (CTRL3_C (12h)) in <a href="#">Section 9.52: FIFO_STATUS1 (3Ah)</a> through <a href="#">Section 9.57: FIFO_DATA_OUT_H (3Fh)</a><br>Updated <a href="#">Figure 16: LGA-14 2.5x3x0.86 mm 14L package outline and mechanical data</a>   |
| 09-Oct-2015 | 7        | Updated <a href="#">Figure 6: Accelerometer composite filter</a> and <a href="#">Figure 16: LGA-14 2.5x3x0.86 mm 14L package outline and mechanical data</a><br>Updated description of HPCF_XL bits in <a href="#">Table 67: CTRL8_XL register description</a><br>Added <a href="#">Table 69: Accelerometer LPF2 cutoff frequency</a><br>Added <a href="#">PEDO_THS_REG (0Fh)</a> and <a href="#">PEDO_DEB_REG (14h)</a><br>Added <a href="#">Section 13.2: LGA-14 packing information</a>   |
| 03-Feb-2016 | 8        | Updated <a href="#">Figure 1: Pin connections</a> and <a href="#">Table 2: Pin description</a><br>Updated <a href="#">Table 3: Mechanical characteristics</a><br>Updated <a href="#">Table 4: Electrical characteristics</a><br>Updated <a href="#">Table 8: Absolute maximum ratings</a><br>Updated <a href="#">Figure 6: Accelerometer composite filter</a><br>Updated <a href="#">Register description</a>  |

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