MAX690A/MAX692A/ MAX802L/MAX802M/ MAX805L

Microprocessor Supervisory Circuits

General Description

The MAX690A/MAX692A/MAX802L/MAX802M/MAX805L reduce the complexity and number of components required for power-supply monitoring and battery-control functions in microprocessor (µP) systems. They significantly improve system reliability and accuracy compared to separate ICs or discrete components.

These parts provide four functions:

1) A reset output during power-up, power-down, and brownout conditions.
2) Battery-backup switching for CMOS RAM, CMOS µP, or other low-power logic.
3) A reset pulse if the optional watchdog timer has not been toggled within 1.6s.
4) A 1.25V threshold detector for power-fail warning or low-battery detection, or to monitor a power supply other than +5V.

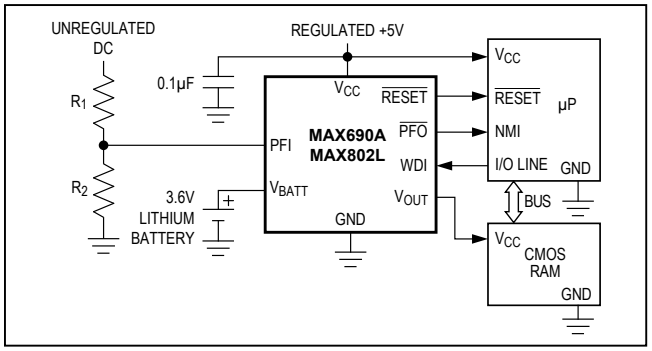
The parts differ in their reset-voltage threshold levels and reset outputs. The MAX690A/MAX802L/MAX805L generate a reset pulse when the supply voltage drops below 4.65V, and the MAX692A/MAX802M generate a reset below 4.40V. The MAX802L/MAX802M guarantee power-fail accuracies to ±2%. The MAX805L is the same as the MAX690A except that RESET is provided instead of $\overline{\text{RESET}}$.

All parts are available in 8-pin DIP and SO packages. The MAX690A/MAX802L are pin compatible with the MAX690 and MAX694. The MAX692A/MAX802M are pin compatible with the MAX692.

Applications

- Battery-Powered Computers and Controllers
- Intelligent Instruments
- Critical µP Power Monitoring

Typical Operating Circuit



Features

- Precision Supply Voltage Monitor:
  4.65V for MAX690A/MAX802L/MAX805L
  4.40V for MAX692A/MAX802M
- Reset Time Delay: 200ms
- Watchdog Timer: 1.6s Timeout
- Battery-Backup Power Switching
- 200µA Quiescent Supply Current
- 50nA Quiescent Supply Current in Battery-Backup Mode
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Power-Fail Accuracy Guaranteed to ±2% (MAX802L/M)
- Guaranteed $\overline{\text{RESET}}$ Assertion to V_{CC} = 1V
- 8-Pin SO and DIP Packages

Ordering Information

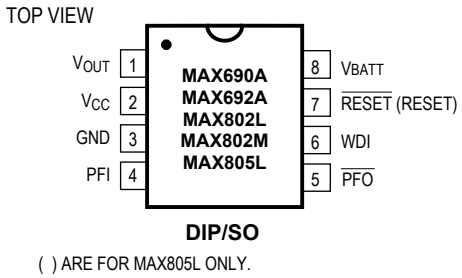
PART	TEMP RANGE	PIN-PACKAGE
MAX690ACPA	0°C to +70°C	8 Plastic DIP
MAX690ACSA	0°C to +70°C	8 SO
MAX690AC/D	0°C to +70°C	Dice*
MAX690AEPA	-40°C to +85°C	8 Plastic DIP
MAX690AESA	-40°C to +85°C	8 SO
MAX690AMJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C*

***Contact factory for availability and processing to MIL STD-883. Devices in PDIP and SO packages are available in both leaded and lead(Pb)-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering. Lead free not available for CERDIP package.*

Pin Configurations



DIP/SO

( ) ARE FOR MAX805L ONLY.

maxim integrated™

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6.0V
- V_{BATT} ..... -0.3V to +6.0V

All Other Inputs (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... Short-Circuit Protected for up to 10s
- All Other Outputs 20mA

Rate of Rise, V_{CC}, V_{BATT} 100V/µs

Continuous Power Dissipation
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX69_AC_ _, MAX80_ _ C_ _ ..... 0°C to +70°C
- MAX69_AE_ _, MAX80_ _ E_ _ ..... -40°C to +85°C
- MAX69_AMJA, MAX805LMJA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10s) ..... +300°C

Note 1: The input voltage limits on PFI and WDI may be exceeded if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 4.75V to 5.5V for MAX690A/MAX802L/MAX805L, V_{CC} = 4.5V to 5.5V for MAX692A/MAX802M, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}, V_{BATT} (Note 2)		MAX69_AC, MAX802_C		1.0		5.5	V
		MAX805LC		1.1		5.5	
		MAX69_AE/M, MAX80_ _E		1.2		5.5	
Supply Current (Excluding I_{OUT})	I_{SUPPLY}	MAX69_AC, MAX802_C			200	350	µA
		MAX69_AE/M, MAX802_E, MAX805LE/M			200	500	
I_{SUPPLY} in Battery-Backup Mode (Excluding I_{OUT})		V_{CC} = 0V, V_{BATT} = 2.8V	T_A = +25°C		0.05	1.0	µA
			T_A = T_{MIN} to T_{MAX}			5.0	
VBATT Standby Current (Note 3)		5.5V > V_{CC} > V_{BATT} +0.2V	T_A = +25°C	-0.1		0.02	µA
			T_A = T_{MIN} to T_{MAX}	-1.0		0.02	
V_{OUT} Output		I_{OUT} = 5mA		V_{CC} - 0.05	V_{CC} - 0.025		V
		I_{OUT} = 50mA		V_{CC} - 0. 5	V_{CC} - 0. 25		
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, V_{CC} < V_{BATT} - 0.2V		V_{BATT} - 0.1	V_{BATT} - 0.02		V
Battery Switch Threshold, V_{CC} to V_{BATT}		V_{CC} < V_{RT}	Power-up		20		mV
			Power-down		-20		
Battery Switchover Hysteresis					40		mV
Reset Threshold	V_{RT}	MAX690A, MAX802L, MAX805L		4.50	4.65	4.75	V
		MAX692A, MAX802M		4.25	4.40	4.50	
		MAX802L, T_A = +25°C, V_{CC} falling		4.55		4.70	
		MAX802M, T_A = +25°C, V_{CC} falling		4.30		4.45	
Reset Threshold Hysteresis					40		mV
Reset Pulse Width	t_{RS}			140	200	280	ms

Electrical Characteristics (continued)

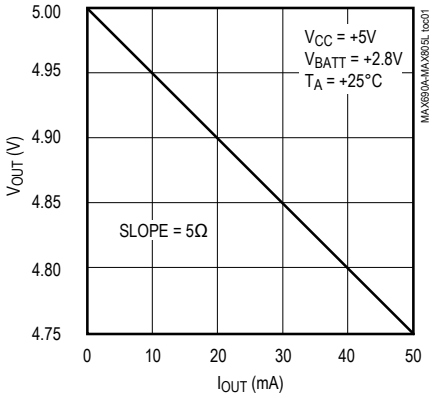
(V_{CC} = 4.75V to 5.5V for MAX690A/MAX802L/MAX805L, V_{CC} = 4.5V to 5.5V for MAX692A/MAX802M, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800µA					V
		I_{SINK} = 3.2mA				0.4	
		MAX69_AC, MAX802_C, V_{CC} = 1.0V I_{SINK} = 50µA				0.3	
		MAX69_AE/M, MAX802_E, V_{CC} = 1.2V, I_{SINK} = 100µA				0.3	
RESET Output Voltage		MAX805LC, I_{SOURCE} = 4µA, V_{CC} = 1.1V		0.8			V
		MAX805LE/M, I_{SOURCE} = 4µA, V_{CC} = 1.2V		0.9			
		MAX805L, I_{SOURCE} = 800µA		V_{CC} - 1.5			
		MAX805L, I_{SINK} = 3.2mA				0.4	
Watchdog Timeout	t_{WD}			1.00	1.60	2.25	s
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = (0.8) (V_{CC})		50			ns
WDI Input Threshold (Note 4)		V_{CC} = 5V	Logic low			0.8	V
			Logic high	3.5			
WDI Input Current		WDI = V_{CC}			50	150	µA
		WDI = 0V		-150	-50		
PFI Input Threshold		MAX69_A, MAX805L, V_{CC} = 5V		1.20	1.25	1.30	V
		MAX802_C/E, V_{CC} = 5V		1.225	1.250	1.275	
PFI Input Current				-25	0.01	25	nA
$\overline{PFO}$ Output Voltage		I_{SOURCE} = 800µA		V_{CC} - 1.5			V
		I_{SINK} = 3.2mA				0.4	

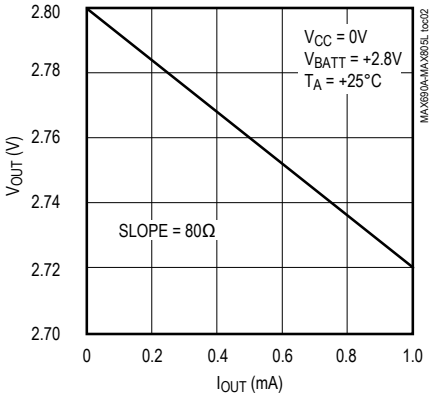
Note 2: Either V_{CC} or V_{BATT} can go to 0V, if the other is greater than 2.0V.
Note 3: "-" = battery-charging current, "+" = battery-discharging current.
Note 4: WDI is guaranteed to be in an intermediate, non-logic level state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 35% of V_{CC} with an input impedance of 50kΩ.

Typical Operating Characteristics

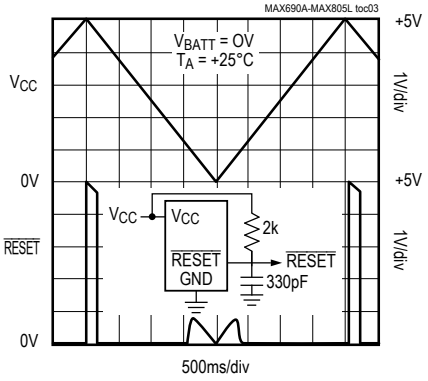
OUTPUT VOLTAGE vs. LOAD CURRENT



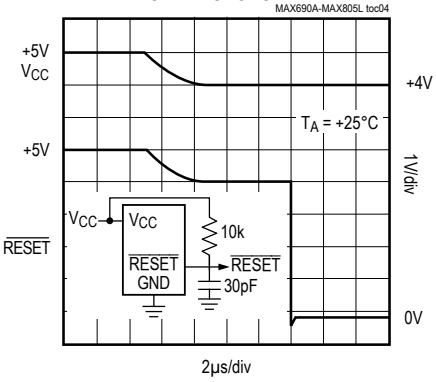
OUTPUT VOLTAGE vs. LOAD CURRENT



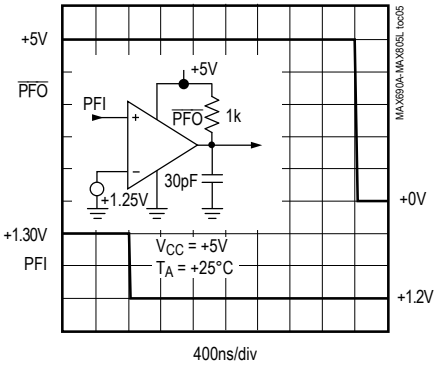
MAX690A $\overline{\text{RESET}}$ OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



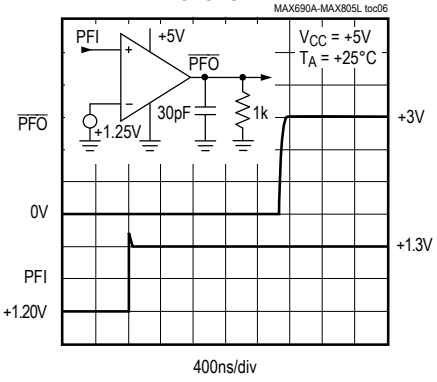
MAX690A $\overline{\text{RESET}}$ RESPONSE TIME



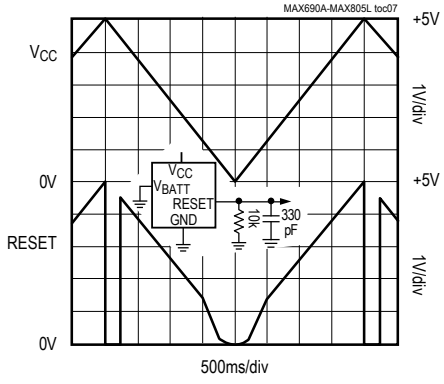
POWER-FAIL COMPARATOR RESPONSE TIME



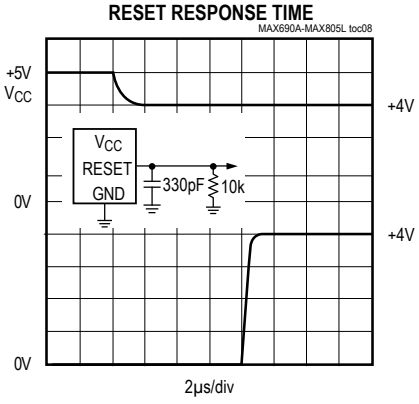
POWER-FAIL COMPARATOR RESPONSE TIME



MAX805L RESET OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



MAX805L RESET RESPONSE TIME



Pin Description

PIN		NAME	FUNCTION
MAX690A/MAX692A MAX802L/MAX802M	MAX805L		
1	1	V_{OUT}	Supply Output for CMOS RAM. When V_{CC} is above the reset threshold, V_{OUT} connects to V_{CC} through a P-channel MOSFET switch. When V_{CC} is below the reset threshold, the higher of V_{CC} or V_{BATT} will be connected to V_{OUT}.
2	2	V_{CC}	+5V Supply Input
3	3	GND	Ground
4	4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	5	$\overline{PFO}$	Power-Fail Output. When PFI is less than 1.25V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ stays high.
6	6	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and reset is triggered. If WDI is left floating or connected to a high-impedance three-state buffer, the watchdog feature is disabled. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge.
7	7	$\overline{RESET}$	Reset Output. Whenever $\overline{RESET}$ is triggered, it pulses low for 200ms. It stays low when V_{CC} is below the reset threshold (4.65V in the MAX690A/MAX802L and 4.4V in the MAX692A/MAX802M) and remains low for 200ms after V_{CC} rises above the reset threshold. A watchdog timeout also triggers $\overline{RESET}$.
—	—	RESET	Active-High Reset Output is the inverse of $\overline{RESET}$. When RESET is asserted, the RESET output voltage = V_{CC} or V_{BATT}, whichever is higher.
8	8	V_{BATT}	Backup-Battery Input. When V_{CC} falls below the reset threshold, V_{BATT} will be switched to V_{OUT} if V_{BATT} is 20mV greater than V_{CC}. When V_{CC} rises to 20mV above V_{BATT}, V_{OUT} will be reconnected to V_{CC}. The 40mV hysteresis prevents repeated switching if V_{CC} falls slowly.

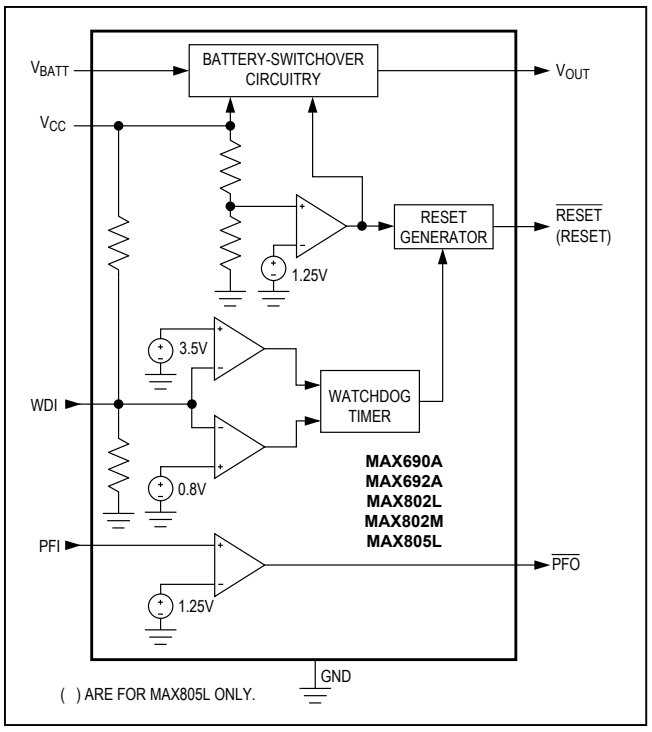


Figure 1. Block Diagram

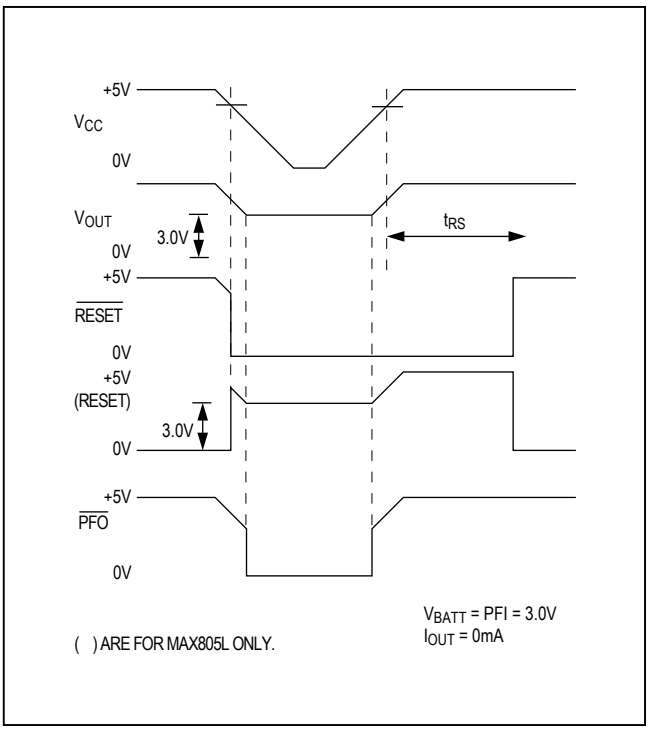


Figure 2. Timing Diagram

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. When the µP is in an unknown state, it should be held in reset. The MAX690A/MAX692A/MAX802L/MAX802M assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is guaranteed to be a logic low. As V_{CC} rises, $\overline{RESET}$ remains low. When V_{CC} exceeds the reset threshold, an internal timer keeps RESET low for a time equal to the reset pulse width; after this interval, $\overline{RESET}$ goes high (Figure 2). If a brownout condition occurs (if V_{CC} dips below the reset threshold), $\overline{RESET}$ is triggered. Each time $\overline{RESET}$ is triggered, it stays low for the reset pulse width interval. Any time V_{CC} goes below the reset threshold, the internal timer restarts the pulse. If a brownout condition interrupts a previously initiated reset pulse, the reset pulse continues for another 200ms. On power-down, once V_{CC} goes below the threshold, $\overline{RESET}$ is guaranteed to be logic low until V_{CC} droops below 1V.

$\overline{RESET}$ is also triggered by a watchdog timeout. If a high or low is continuously applied to the WDI pin for 1.6sec, $\overline{RESET}$ pulses low. As long as $\overline{RESET}$ is asserted, the watchdog timer remains clear. When $\overline{RESET}$ comes high, the watchdog resumes timing and must be serviced within 1.6sec. If WDI is tied high or low, a $\overline{RESET}$ pulse is triggered every 1.8s (t_{WD} plus t_{RS}).

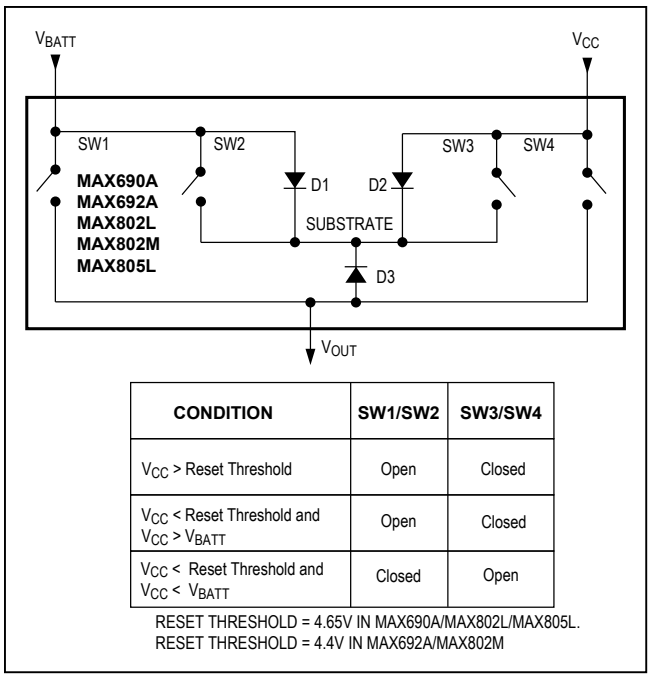
The MAX805L active-high $\overline{RESET}$ output is the inverse of the MAX690A/MAX692A/MAX802L/MAX802M $\overline{RESET}$ output, and is guaranteed to be valid with V_{CC} down to 1.1V. Some µPs, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Input

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec, a reset pulse is triggered. The internal 1.6sec timer is cleared by either a reset pulse or by open circuiting the WDI input. As long as reset is asserted or the WDI input is open circuited, the timer remains cleared and does not count. As soon as reset is released or WDI is driven high or low, the timer starts counting. It can detect pulses as short as 50ns.

Power-Fail Comparator

The PFI input is compared to an internal 1.25V reference. If PFI is less than 1.25V, $\overline{PFO}$ goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply; it need not be



CONDITION	SW1/SW2	SW3/SW4
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold and V_{CC} > V_{BATT}	Open	Closed
V_{CC} < Reset Threshold and V_{CC} < V_{BATT}	Closed	Open

RESET THRESHOLD = 4.65V IN MAX690A/MAX802L/MAX805L.
RESET THRESHOLD = 4.4V IN MAX692A/MAX802M

Figure 3. Backup-Battery Switchover Block Diagram

dedicated to this function though, as it is completely separate from the rest of the circuitry. The external voltage divider drives PFI to sense the unregulated DC input to the +5V regulator (see *Typical Operating Circuit*). The voltage-divider ratio can be chosen such that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. $\overline{PFO}$ then triggers an interrupt which signals the µP to prepare for power-down.

To conserve backup-battery power, the power-fail detector comparator is turned off and $\overline{PFO}$ is forced low when V_{BATT} connects to V_{OUT}.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at V_{BATT}, the devices automatically switch RAM to backup power when V_{CC} fails.

As long as V_{CC} exceeds the reset threshold, V_{OUT} connects to V_{CC} through a 5Ω PMOS power switch. Once VCC falls below the reset threshold, V_{CC} or V_{BATT} (whichever is higher) switches to V_{OUT}. Unlike the MAX690/MAX692, the MAX690A/MAX692A/MAX802L/

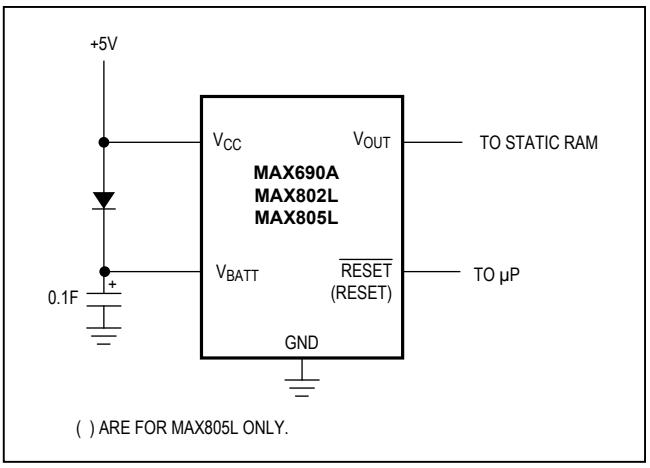


Figure 4. Using a SuperCap as a Backup Power Source with a MAX690A/MAX802L/MAX805L and a +5V ±5% Supply

Table 1. Wiper Position and Attenuation

SIGNAL	STATUS
V_{CC}	Disconnected from V_{OUT}
V_{OUT}	Connected to V_{BATT} through an internal 80Ω PMOS switch
V_{BATT}	Connected to V_{OUT}. Current drawn from the battery is less than 1µA, as long as V_{CC} < V_{BATT} - 1V.
PFI	Power-fail comparator is disabled.
$\overline{PFO}$	Logic low
$\overline{RESET}$	Logic low
RESET	Logic high (MAX805L only)
WDI	Watchdog timer is disabled

MAX802M/MAX805L don't always connect V_{BATT} to V_{OUT} when V_{BATT} is greater than V_{CC}. V_{BATT} connects to V_{OUT} (through an 80Ω switch) only when V_{CC} is below the reset threshold **and** V_{BATT} is greater than V_{CC}.

When V_{CC} exceeds the reset threshold, it is connected to the MAX690A/MAX692A/MAX802L/MAX802M/MAX805L substrate, regardless of the voltage applied to V_{BATT} (Figure 3). During this time, the diode (D1) between V_{BATT} and the substrate will conduct current from V_{BATT} to V_{CC} if V_{BATT} is 0.6V or greater than V_{CC}.

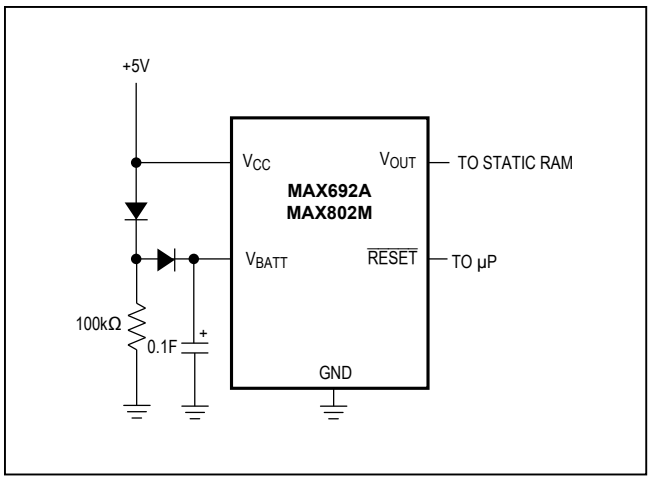


Figure 5. Using a SuperCap as a Backup Power Source with the MAX692A/MAX802M and a +5V ±10% Supply

When V_{BATT} connects to V_{OUT}, backup mode is activated and the internal circuitry is powered from the battery (Table 1). When V_{CC} is just below V_{BATT}, the current drawn from V_{BATT} is typically 30µA. When V_{CC} drops to more than 1V below V_{BATT}, the internal switchover comparator shuts off and the supply current falls to less than 1µA.

Applications Information

Using a SuperCap as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values, on the order of 0.1F. Figure 4 shows a SuperCap used as a backup power source. Do not allow the SuperCap's voltage to exceed the maximum reset threshold by more than 0.6V. In Figure 4's circuit, the SuperCap rapidly charges to within a diode drop of V_{CC}. However, after a long time, the diode leakage current will pull the SuperCap voltage up to V_{CC}. When using a SuperCap with the MAX690A/MAX802L/MAX805L, V_{CC} may not exceed 4.75V + 0.6V = 5.35V.

Use the SuperCap circuit of Figure 5 with a MAX692A or MAX802M and a ±10% supply. This circuit ensures that the SuperCap only charges to V_{CC} - 0.5V. At the maximum V_{CC} of 5.5V, the SuperCap charges up to 5.0V, only 0.5V above the maximum reset threshold—well within the requisite 0.6V.

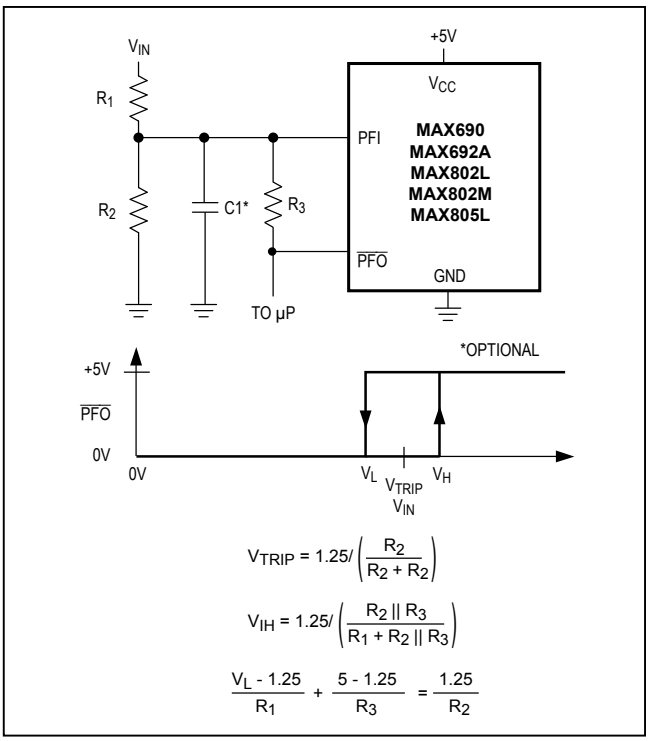


Figure 6. Adding Hysteresis to the Power-Fail Comparator

Table 2. Allowable Backup-Battery Voltages

(see *Using a SuperCap as a Backup Power Source* section for use with a SuperCap)

PART NO.	MAXIMUM BACKUP-BATTERY VOLTAGE (V)
MAX690A/ MAX802L/MAX805L	4.80
MAX692A/ MAX802M	4.55

Allowable Backup Power-Source Batteries

Lithium batteries work very well as backup batteries due to very low self-discharge rates and high energy density. Single lithium batteries with open-circuit voltages of 3.0V to 3.6V are ideal. Any battery with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be connected directly to the V_{BATT} input of the MAX690A/MAX692A/MAX802L/MAX802M/MAX805L with no additional circuitry (see the *Typical Operating Circuit*). However, batteries with open-circuit voltages that are greater **cannot** be used for backup, as current is sourced into the substrate through the diode (D1 in Figure 3) when V_{CC} is close to the reset threshold.

Operation Without a Backup Power Source

If a backup power source is not used, ground V_{BATT} and connect V_{OUT} to V_{CC}. Since there is no need to switch over to any backup power source, V_{OUT} does not need to be switched. A direct connection to V_{CC} eliminates any voltage drops across the switch which may push V_{OUT} below V_{CC}.

Replacing the Backup Battery

The backup battery can be removed while V_{CC} remains valid, without danger of triggering RESET/$\overline{\text{RESET}}$. As long as V_{CC} stays above the reset threshold, battery-backup mode cannot be entered. In other switchover ICs where battery-backup mode is entered whenever V_{BATT} gets close to V_{CC}, an unconnected V_{BATT} pin accumulates leakage charge and triggers RESET/$\overline{\text{RESET}}$ in error.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when V_{IN} is close to its trip point. Figure 6 shows how to add hysteresis to the power-fail comparator. Select the ratio of R_1 and R_2 such that PFI sees 1.25V when V_{IN} falls to its trip point (V_{TRIP}). R_3 adds the hysteresis. It will typically be an order of magnitude greater than R_1 or R_2 (about 10 times either R_1 or R_2). The current through R_1 and R_2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R_3 should be larger than 10kΩ so it does not load down the $\overline{\text{PFO}}$ pin. Capacitor C1 adds additional noise rejection.

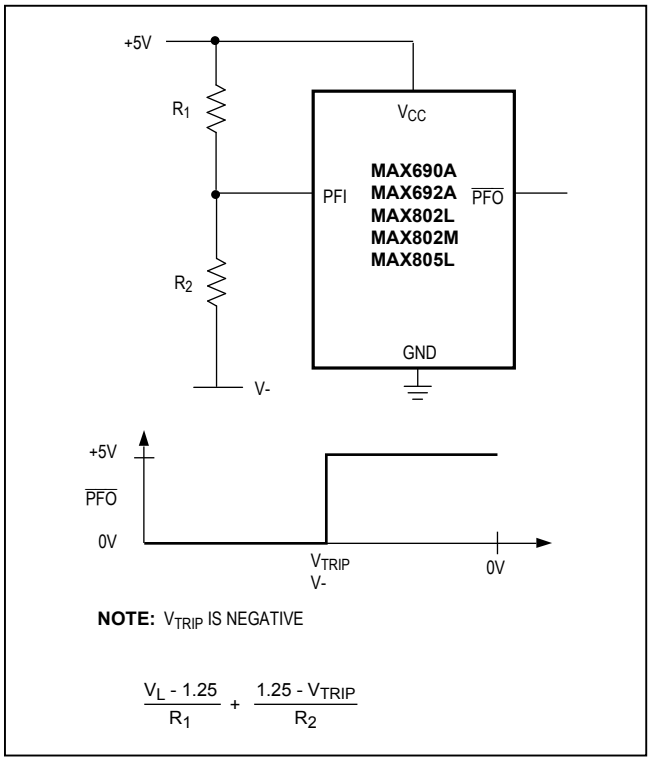


Figure 7. Monitoring a Negative Voltage

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply rail using the circuit of Figure 7. When the negative rail is good (a negative voltage of large magnitude), $\overline{\text{PFO}}$ is low. When the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{\text{PFO}}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} line, and the resistors.

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX690A/MAX692A/MAX802L/MAX802M $\overline{\text{RESET}}$ output. If, for example, the $\overline{\text{RESET}}$ output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{\text{RESET}}$ output and the µP reset I/O, as in Figure 8. Buffer the $\overline{\text{RESET}}$ output to other system components.

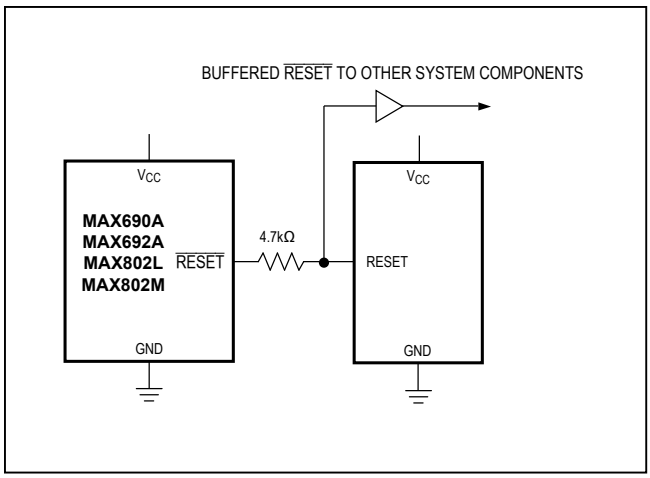


Figure 8. Interfacing to µPs with Bidirectional Reset I/O

µP Supervisory Circuits

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (s)	Backup-Battery Switch	$\overline{CE}$ - Write Protect	Power-Fail Comparator	Manual-Reset Input	Watch-dog Output	Low-Line Output	Active-High Reset	Battery-On Output
MAX690A/692A	4.65/4.40	140	1.6	✓		✓					
MAX691A/693A	4.65/4.40	140/adj.	1.6/adj.	✓	✓/10ns	✓		✓	✓	✓	✓
MAX696	Adj.	35/adj.	1.6/adj.	✓		✓		✓	✓	✓	✓
MAX697	Adj.	35/adj.	1.6/adj.		✓	✓		✓	✓	✓	
MAX700	4.65/adj.	200	–				✓			✓	
MAX703/704	4.65/4.40	140	–	✓		✓	✓				
MAX705/706	4.65/4.40	140	1.6			✓	✓	✓			
MAX706P	2.63	140	1.6			✓	✓	✓		✓	
MAX706R/S/T	2.63/2.93/ 3.08	140	1.6			✓	✓	✓			
MAX707/708	4.65/4.40	140	–			✓	✓			✓	
MAX708R/S/T	2.63/2.93/ 3.08	140	–			✓	✓			✓	
MAX709L/M/ R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	–								
MAX791	4.65	140	1	✓	✓/10ns	✓	✓	✓	✓	✓	✓
MAX792L/M/ R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	1		✓/10ns	✓	✓	✓	✓	✓	
MAX800L/M	4.60/4.40	140	1.6/adj.	✓	✓/10ns	✓/±2%		✓	✓	✓	✓
MAX802L/M	4.60/4.40	140	1.6	✓		✓/±2%					
MAX805L	4.65	140	1.6	✓		✓				✓	
MAX813L	4.65	140	1.6			✓	✓	✓		✓	
MAX820L/M/ R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	1		✓/10ns	✓/±2%	✓	✓	✓	✓	
MAX1232	4.37/4.62	250	0.15/0.60/1.2				✓			✓	
MAX1259	–	–	–	✓		✓					

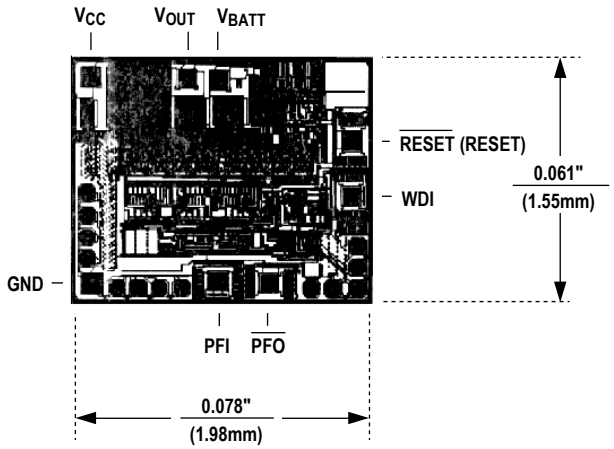
Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX692ACPA	0°C to +70°C	8 Plastic DIP
MAX692ACSA	0°C to +70°C	8 SO
MAX692AC/D	0°C to +70°C	Dice*
MAX692AEPA	-40°C to +85°C	8 Plastic DIP
MAX692AESA	-40°C to +85°C	8 SO
MAX692AMJA	-55°C to +125°C	8 CERDIP**
MAX802LCPA	0°C to +70°C	8 Plastic DIP
MAX802LCSA	0°C to +70°C	8 SO
MAX802LEPA	-40°C to +85°C	8 Plastic DIP
MAX802LESA	-40°C to +85°C	8 SO
MAX802MCPA	0°C to +70°C	8 Plastic DIP
MAX802MCSA	0°C to +70°C	8 SO
MAX802MEPA	-40°C to +85°C	8 Plastic DIP
MAX802MESA	-40°C to +85°C	8 SO
MAX805LCPA	0°C to +70°C	8 Plastic DIP
MAX805LCSA	0°C to +70°C	8 SO
MAX805LC/D	0°C to +70°C	Dice*
MAX805LEPA	-40°C to +85°C	8 Plastic DIP
MAX805LESA	-40°C to +85°C	8 SO
MAX805LMJA	-55°C to +125°C	8 CERDIP**

**Dice are specified at T_A = +25°C*

***Contact factory for availability and processing to MIL STD-883. Devices in PDIP and SO packages are available in both leaded and lead(Pb)-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering. Lead free not available for CERDIP package.*

Chip Topography



( ) ARE FOR MAX805L ONLY.

TRANSISTOR COUNT: 573;

SUBSTRATE MUST BE LEFT UNCONNECTED.

Package Information

For the latest package outline information and land patterns, go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE e CODE	OUTLINE NO.	LAND PATTERN NO.
8 PDIP	P8+1	21-0043	—
8 CDIP	J8+2	21-0045	—
8 SOIC	S8+2	21-0041	90-0096

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
5	4/15	No /V OPNs in *Ordering Information*; deleted Automotive Systems in *Applications Information* section; added *Package Information* and *Revision History* tables	1, 12, 13

