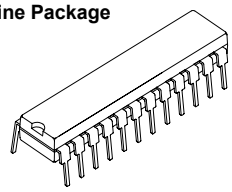
16-Bit Constant Current LED Sink Driver with Error Detection and Current Adjust

Features

- Compatible with MBI5026 in electrical characteristics and package
- Exploiting **Share-I-O™** technique to provide two operation modes:
  - Normal Mode with the same functionality as MBI5026
  - Special Mode to detect individual LED errors, like MBI5027 and program output current gain, like MBI5028
- 16 constant-current output channels
- Constant output current invariant to load voltage change
- Constant output current range: 5 -90 mA
- Excellent output current accuracy,
  between channels: < ±3% (max.), and
  between ICs: < ±6% (max.)
- Output current adjusted through an external resistor
- 128-step programmable output current gain for White Balance,
  low current band: gain = 1/9 ~ 95/288, linearly divided into 64 steps
  high current band: gain = 1/3 ~ 95/96, linearly divided into 64 steps
- Fast response of output current,
  $\overline{OE}$ (min.): 200 ns
- 25MHz clock frequency
- Schmitt trigger input
- 5V supply voltage
- Optional for “Pb-free & Green” Package

Dual In-Line Package



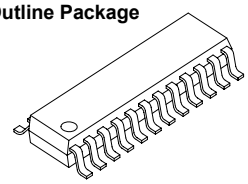
CN: P-DIP24-300-2.54

GN: P-DIP24-300-2.54

CNS: SP-DIP24-300-1.78

GNS: SP-DIP24-300-1.78

Small Outline Package



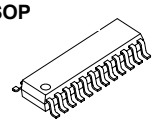
CD: SOP24-300-1.27

GD: SOP24-300-1.27

CF: SOP24-300-1.00

GF: SOP24-300-1.00

Shrink SOP



CP\CPA: SSOP24-150-0.64

GP\GPA: SSOP24-150-0.64

Current Accuracy		Conditions
Between Channels	Between ICs	
< ±3%	< ±6%	I_{OUT} = 10 ~ 60 mA

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Product Description

MBI5029 succeeds MBI5026 and also exploits **PrecisionDrive™** technology to enhance its output characteristics. Furthermore, MBI5029 uses the idea of **Share-I-O™** technology to make MBI5029 backward compatible with MBI5026 in both package and electrical characteristics and extend its functionality for LED load Error Detection and run-time LED current gain control in LED display systems, especially LED traffic sign applications.
MBI5029 contains a 16-bit Shift Register and a 16-bit Output Latch, which convert serial input data into parallel output format. At MBI5029 output stages, sixteen regulated current ports are designed to provide uniform and constant current sinks with small skew between ports for driving LED's within a wide range of forward voltage (Vf) variations. Users may adjust the output current from 5 mA to 90 mA with an external resistor R_{ext}, which gives users flexibility in controlling the light intensity of LED's. MBI5029 guarantees to endure maximum 17V at the output ports. Besides, the high clock frequency up to 25 MHz also satisfies the system requirements of high volume data transmission.

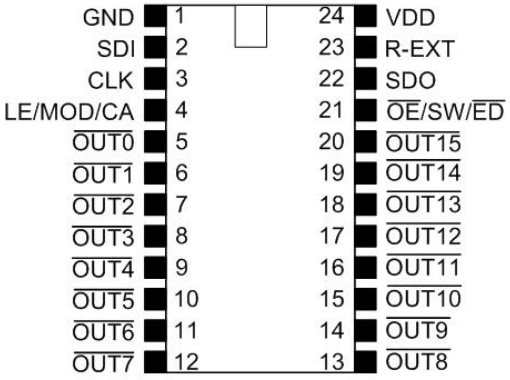
Besides Normal Mode, MBI5029 provide another mode, Special Mode, to extend its functionality by means of the **Share-I-O™** technique on pins LE and $\overline{OE}$, without any extra pins. In Special Mode two functions are included, Error Detection and Current Gain Control. Thus, MBI5029 could be a drop-in replacement of MBI5026. The printed circuit board originally designed for MBI5026 may be also applied to MBI5029. In MBI5029 there are two operation modes and three phases: Normal Mode phase, Mode Switching transition phase, and Special Mode phase. The signal on the multiple function pin $\overline{OE}$ / SW / $\overline{ED}$ would be monitored. Once an one-clock-wide short pulse appears on the pin $\overline{OE}$ / SW / $\overline{ED}$, MBI5029 would enter the Mode Switching phase. At this moment, the voltage level on the pin LE/MOD/CA is used to determine the next mode to which MBI5029 is going to switch.

In the Normal Mode phase, MBI5029 has exactly the same functionality with MBI5026. The serial data could be transferred into MBI5029 via the pin SDI, shifted in the Shift Register, and go out via the pin SDO. The LE/MOD/CA can latch the serial data in the Shift Register to the Output Latch. $\overline{OE}$ / SW / $\overline{ED}$ would enable the output drivers to sink current.

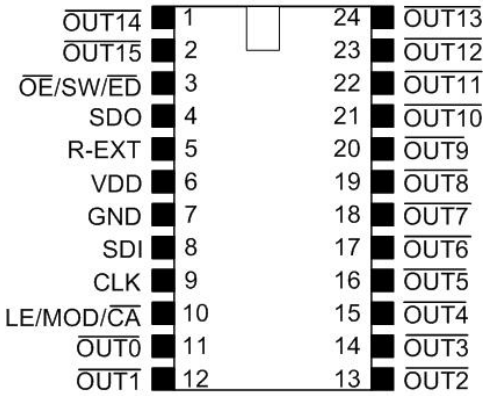
In the Special Mode phase, the low-voltage-level signal $\overline{OE}$ / SW / $\overline{ED}$ can enable output channels and detect the status of the output current to tell if the driving current level is enough or not. The detected error status would be loaded into the 16-bit Shift Register and be shifted out via the pin SDO along with the signal CLK. Then system controller could read the error status and know whether the LED's are properly lit or not.

On the other hand, in the Special Mode phase MBI5029 also allows users to adjust the output current level by setting a run-time programmable Configuration Code. The code is sent into MBI5029 via the pin SDI. The positive pulse of LE/MOD/CA would latch the code in the Shift Register into a built-in 16-bit Configuration Latch, instead of the Output Latch. The code would affect the voltage at the terminal R-EXT and control the output current regulator. The output current could be adjusted finely by a gain ranging from 1/9 to 95/96 in 128 steps. Hence, the current skew between IC's can be compensated within less than 1% and this feature is suitable for white balancing in LED color display panels.

Pin Configuration



MBI5029 CN\CNS\CD\CF\CP\ GN\GNS\GD\GF\GP



MBI5029 CPA\GPA

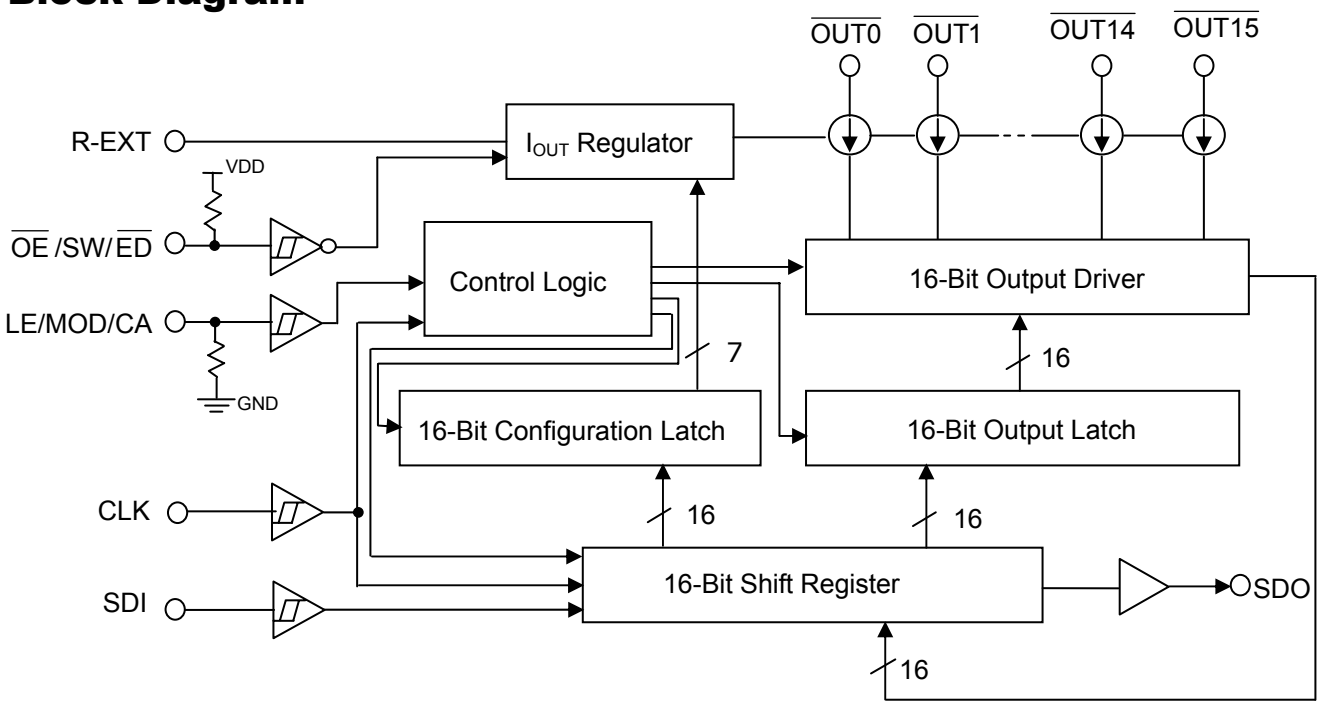
Terminal Description

Pin Name	Function
GND	Ground terminal for control logic and current sinks
SDI	Serial-data input to the Shift Register
CLK	Clock input terminal for data shift at the rising edge
LE/MOD/CA	**Output channel data strobe input terminal:** in the Normal Mode phase, serial data in the Shift Register is transferred to the respective Output Latch when LE/MOD/CA is high; the data is latched inside the Output Latch when LE/MOD/CA goes low. If the data in the Output Latch is "1" (High), the respective output channel will be enabled after $\overline{OE}$ / SW / $\overline{ED}$ is pulled down to low. **Mode selection input terminal:** in the Mode Switching phase, LE/MOD/CA couldn't strobe serial data but its level is used for determining the next mode to which MBI5029 is going to switch. When LE/MOD/CA is high, the next mode is the Special Mode; when low, the next mode is the Normal Mode. **Configuration data strobe input terminal:** in the Special Mode phase, serial data is latched into the Configuration Latch, instead of the Output Latch in the Normal Mode. The serial data here is regarded as the Configuration Code, which affect the output current level of all channels.
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
$\overline{OE}$ / SW / $\overline{ED}$	**Output enable terminal:** no matter in what phase MBI5029 operates, the signal $\overline{OE}$ / SW / $\overline{ED}$ can always enable output drivers to sink current. When its level is (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked). **Mode switching trigger terminal:** an one-clock-wide short pulse signal of $\overline{OE}$ / SW / $\overline{ED}$ could put MBI5029 into the Mode Switching phase. **Error detection enable terminal:** in the Special Mode phase, the active low signal $\overline{OE}$ / SW / $\overline{ED}$ can make MBI5029 not just enable output drivers but detect LED load error status. The detected error status would be stored into the Shift Register.
SDO	Serial-data output to the following SDI of the next driver IC
R-EXT	Input terminal used for connecting an external resistor in order to set up the current level of all output ports
VDD	5V supply voltage terminal

In MBI5029, the relationship between the functions of pins LE/MOD/CA and $\overline{OE}$ / SW / $\overline{ED}$ and the operation phases are listed below:

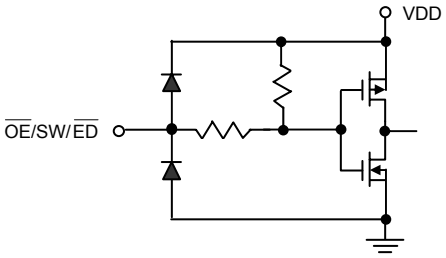
Pin Name	Function	Normal Mode	Mode Switching	Special Mode
LE/MOD/CA	LE: latching serial data into the Output Latch	Yes	No	No
	MOD: mode selection	No	Yes	No
	CA: latching serial data into the Configuration Latch	No	No	Yes
$\overline{OE}$ / SW / $\overline{ED}$	$\overline{OE}$: enabling the current output drivers	Yes	Yes	Yes
	SW: entering the Mode Switching phase	Yes	Yes	Yes
	$\overline{ED}$: enabling error detection and storing results into the Shift Register	No	No	Yes

Block Diagram

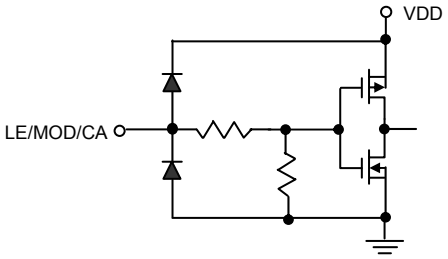


Equivalent Circuits of Inputs and Outputs

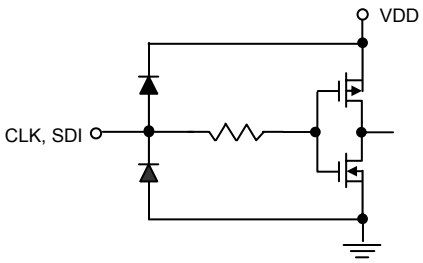
OE/SW/ED Terminal



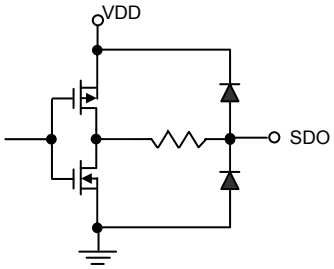
LE/MOD/CA Terminal



CLK, SDI Terminal

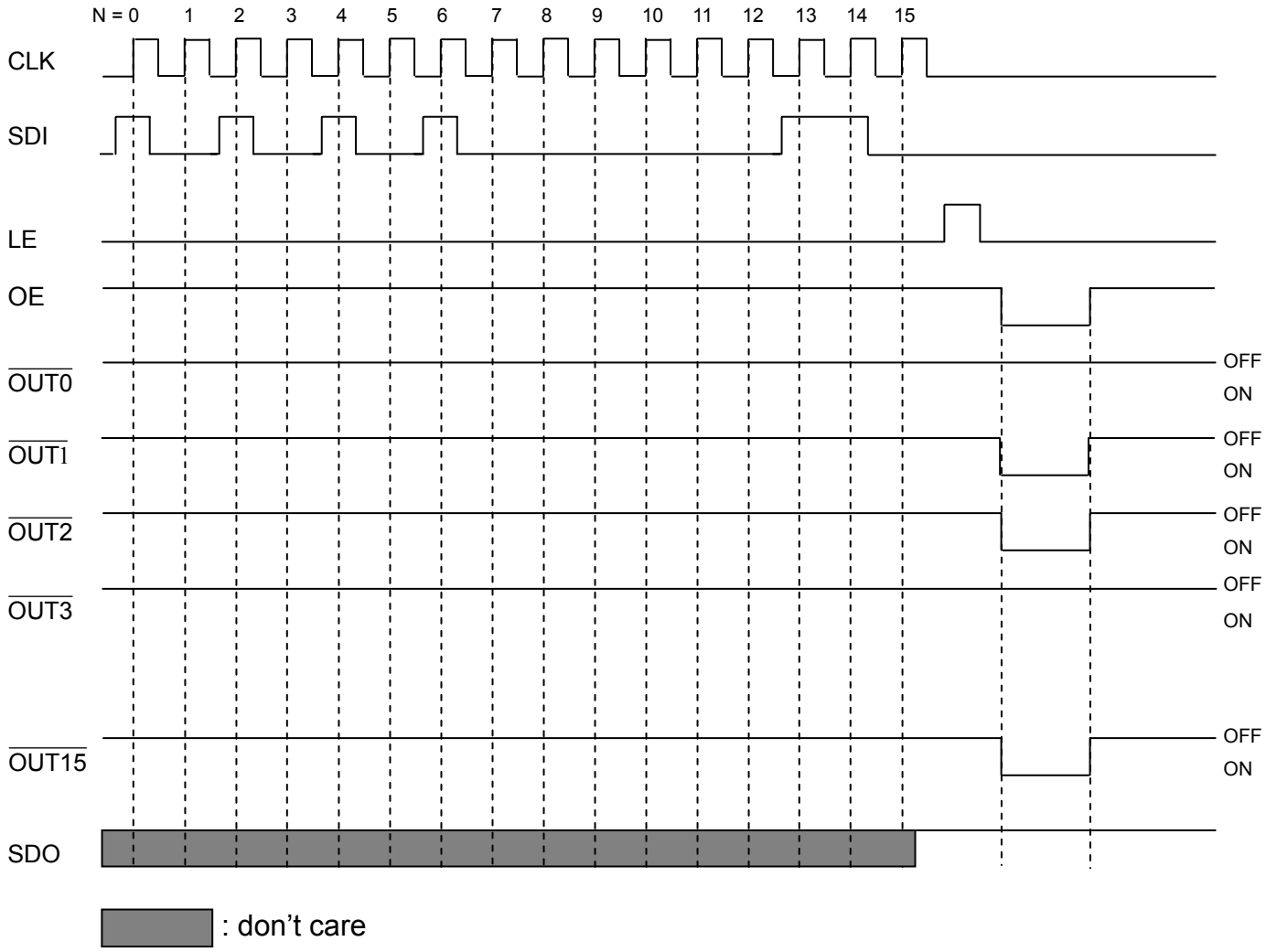


SDO Terminal



Timing Diagram

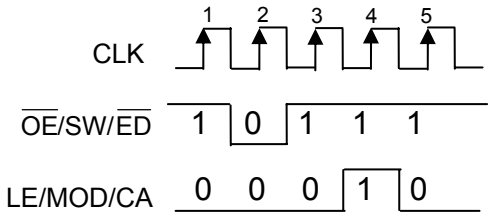
Normal Mode



Truth Table (In Normal Mode)

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ … $\overline{OUT7}$ … $\overline{OUT15}$	SDO
↑	H	L	D_n	$\overline{D_n}$ ….. $\overline{D_{n-7}}$ …. $\overline{D_{n-15}}$	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ …. $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ …. $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	H	D_{n+3}	Off	D_{n-13}

Switching to Special Mode

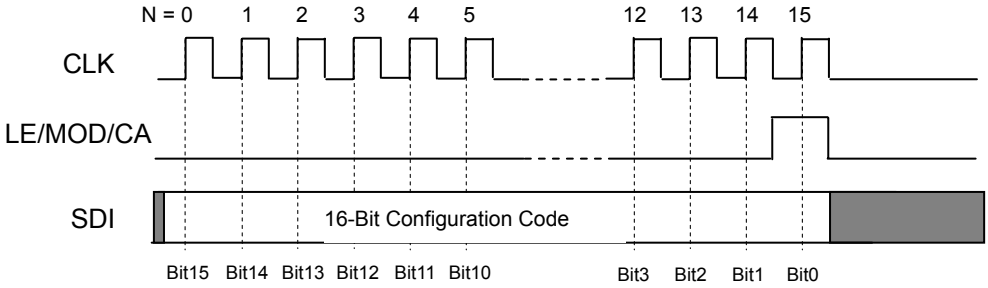


The above shows an example of the signal sequence that can set the next operation mode of MBI5029 to be the Special Mode. The LE/MOD/CA active pulse here would not latch any serial data.

Note:

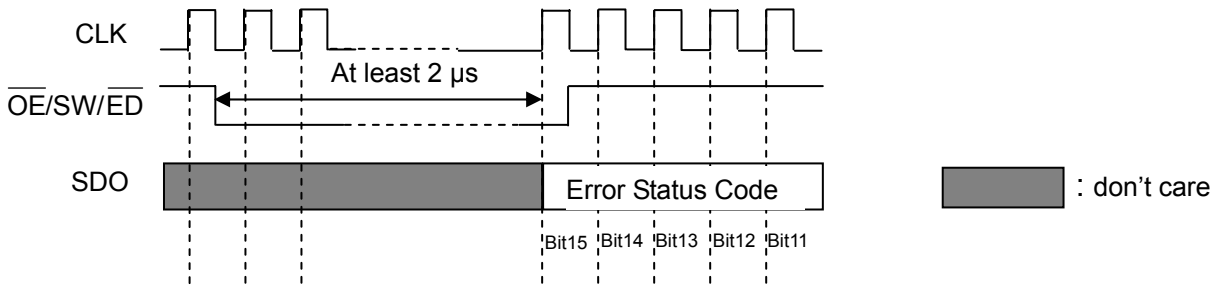
After entering the Special Mode, MBI5029 can detect LED error and adjust current gain.

Writing Configuration Code (In Special Mode)



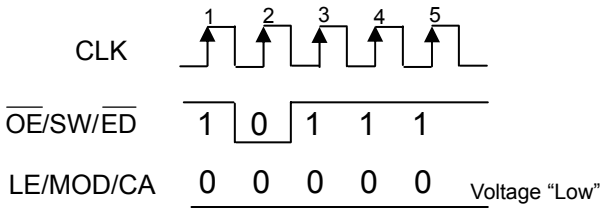
In the Special Mode, by sending the positive pulse of LE/MOD/CA, the content of the Shift Register with a Configuration Code will be written to the 16-bit Configuration Latch.

Reading Error Status Code (In Special Mode)



When MBI5029 is working in the Special Mode, the above signal sequence example can let a system controller read the Error Status codes via the pin SDO.

Switching to Normal Mode



The above signal sequence example can make MBI5029 operate in the Normal Mode.

Note:

If users want to know the detailed process for each of the above examples, please refer to the contents in **Operation Principle**.

Maximum Ratings

Characteristics			Symbol	Rating		Unit
Supply Voltage			V_{DD}	0 ~ 7.0		V
Input Voltage			V_{IN}	-0.4 ~ V_{DD} + 0.4		V
Output Current			I_{OUT}	+90		mA
Output Voltage			V_{DS}	-0.5 ~ +17		V
Clock Frequency			F_{CLK}	25		MHz
GND Terminal Current			I_{GND}	1440		mA
Power Dissipation (On PCB, Ta=25°C)	CN	GN	P_D	1.80	2.00	W
	CNS	GNS		1.50	1.61	
	CD	GD		2.01	2.19	
	CF	GF		1.69	1.91	
	CP	GP		1.38	1.46	
	CPA	GPA		1.38	1.46	
Thermal Resistance (On PCB, Ta=25°C)	CN	GN	$R_{th(j-a)}$	53.82	49.91	°C/W
	CNS	GNS		66.74	62.28	
	CD	GD		49.81	45.69	
	CF	GF		59.01	52.38	
	CP	GP		72.43	68.48	
	CPA	GPA		72.43	68.48	
Operating Temperature			T_{opr}	-40 ~ +85		°C
Storage Temperature			T_{stg}	-55 ~ +150		°C

Recommended Operating Conditions

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	-	4.5	5.0	5.5	V
Output Voltage	V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$	-	-	17.0	V
Output Current	I_{OUT}	$\overline{OUT0}$ ~ $\overline{OUT15}$	5	-	90	mA
	I_{OH}	SDO	-	-	-1.0	mA
	I_{OL}	SDO	-	-	1.0	mA
Input Voltage	V_{IH}	CLK, $\overline{OE}$/SW/$\overline{ED}$ LE/MOD/CA, and SDI	0.8*V_{DD}	-	V_{DD}	V
	V_{IL}	CLK, $\overline{OE}$/SW/$\overline{ED}$, LE/MOD/CA, and SDI	GND	-	0.3*V_{DD}	V
CLK Pulse Width	$t_{w(CLK)}$	-	20	-	-	ns
Setup Time for SDI	$t_{su(D)}$		5	-	-	ns
Hold Time for SDI	$t_{h(D)}$		10	-	-	ns
LE/MOD/CA Pulse Width	$t_{w(L)}$		20	-	-	ns
Setup Time for LE/MOD/CA	$t_{su(L)}$	For data strobe	5	-	-	ns
Hold Time for LE/MOD/CA	$t_{h(L)}$		10	-	-	ns
Setup Time for LE/MOD/CA	$t_{su(MOD)}$	In Mode Switching	5	-	-	ns
Hold Time for LE/MOD/CA	$t_{h(MOD)}$		10	-	-	ns
$\overline{OE}$/SW/$\overline{ED}$ Pulse Width	$t_{w(SW)}$	To trigger Mode Switching	20	-	-	ns
	$t_{w(OE)}$	I_{out} < 60mA	200	-	-	ns
	$t_{w(OE)}$	I_{out} = 60~100mA	400	-	-	ns
	$t_{w(ED)}$	When detecting LED error status	2010	-	-	ns
Setup Time for Correctly-Generated Error Status Code *	$t_{su(ER)}$	When detecting LED error status	2000	-	-	ns
Setup Time for $\overline{OE}$/SW/$\overline{ED}$	$t_{su(SW)}$	To trigger Mode Switching or when detecting LED error status	5	-	-	ns
Hold Time for $\overline{OE}$/SW/$\overline{ED}$	$t_{h(SW)}$		10	-	-	ns
Clock Frequency	F_{CLK}	Cascade Operation	-	-	25	MHz

* In the Error Detection mode, when $\overline{OE}$/SW/$\overline{ED}$ is pulled down to LOW for enabling output drivers and error detection, the output drivers must be enabled for at least 2us so that the error status code could be correctly generated. See **Operation Principle** and **Timing Waveform**.

Electrical Characteristics

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-	4.5	5.0	5.5	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$	-	-	17.0	V
Output Current		I_{OUT}	Test Circuit for Electrical Characteristics	5	-	90	mA
		I_{OH}	SDO	-	-	-1.0	mA
		I_{OL}	SDO	-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta = -40~85ºC	0.8*V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta = -40~85ºC	GND	-	0.3*V_{DD}	V
Output Leakage Current			V_{DS}=17.0V and channel off	-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA	-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA	4.6	-	-	V
Output Current 1		I_{OUT1}	V_{DS}=0.6V; R_{ext}=809 Ω; G**=0.9896	-	26.0	-	mA
Current Skew (between channels)		dI_{OUT1}	I_{OUT} = 26mA, V_{DS} = 0.6V, R_{ext}=809 Ω	-	±1	±3	%
Output Current 2		I_{OUT2}	V_{DS} = 0.8V; R_{ext} = 404Ω; G**=0.9896	-	52.1	-	mA
Current Skew (between channels)		dI_{OUT2}	I_{OUT} = 52.1mA, V_{DS} = 0.8V, R_{ext} = 404Ω	-	±1	±3	%
Output Current vs. Output Voltage Regulation		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V	-	±0.1	-	% / V
Output Current vs. Supply Voltage Regulation		$\%/dV_{DD}$	V_{DD} within 4.5V and 5.5V	-	±1	-	% / V
Pull-up Resistance		R_{IN}(up)	$\overline{OE}$/SW/$\overline{ED}$	250	500	800	KΩ
Pull-down Resistance		R_{IN}(down)	LE/MOD/CA	250	500	800	KΩ
Open Circuit Error*** Discrimination Voltage		$V_{DS, Th1}$	When all output ports sink $I_{out,target}$ =20mA simultaneously	1.0	-	-	V
		$V_{DS, Th2}$	When a single output port sinks $I_{out,target}$ =20mA	0.8	-	-	V
		$V_{DS, Th3}$	When all output ports sink $I_{out,target}$ =50mA simultaneously	1.2	-	-	V
		$V_{DS, Th4}$	When a single output port sinks $I_{out,target}$ =50mA	1.0	-	-	V
Supply Current	"OFF"	I_{DD}(off) 0	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off, G**=0.9896	-	7	12	mA
		I_{DD}(off) 1	R_{ext}=809 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off, G**=0.9896	-	10	12	
		I_{DD}(off) 2	R_{ext}=404 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off, G**=0.9896	-	12	15	
	"ON"	I_{DD}(on) 1	R_{ext}=809 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=On, G**=0.9896	-	10	18	
		I_{DD}(on) 2	R_{ext}=404 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=On, G**=0.9896	-	12	20	

** In the above table, G is the programmable output current gain. The detail description could be found in the section **Operation Principle**.

*** To effectively detect the open-circuit error occurring at the output port, MBI5029 has a built-in current detection circuit. The current detection circuit will detect the effective current $I_{OUT, effective}$ and compare the

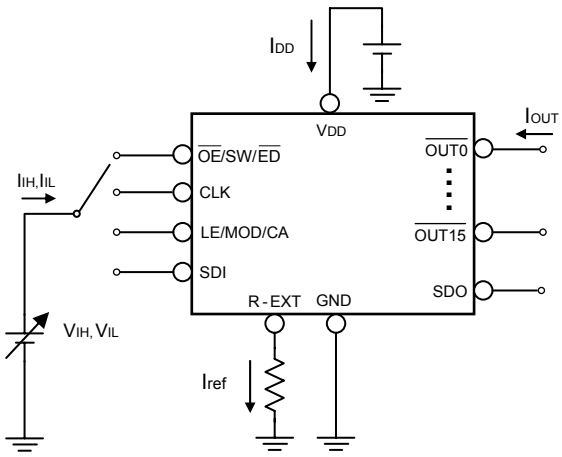
effective current $I_{OUT, effective}$ to the target current $I_{OUT, target}$ defined by R_{ext}. If $I_{OUT, effective}$ is less than the target current $I_{OUT, target}$, an error flag(Low) will be asserted and stored into the built-in Shift Register. The minimum voltage requirement for such current detection is $V_{DS, Th1}$, $V_{DS, Th2}$, $V_{DS, Th3}$ and $V_{DS, Th4}$.

Switching Characteristics

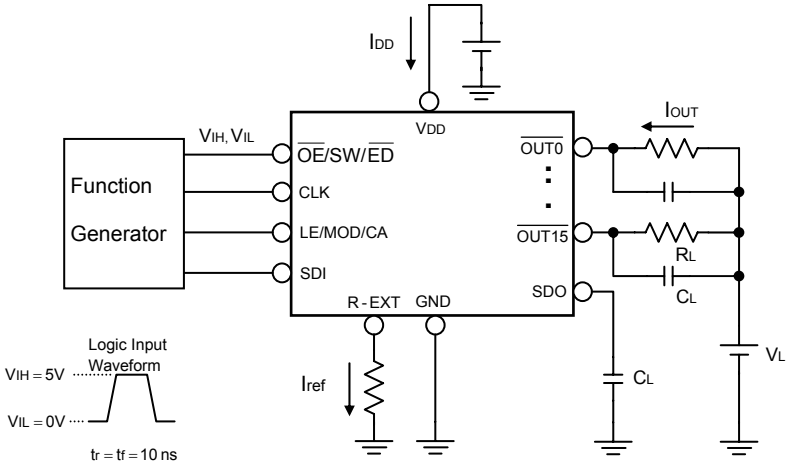
Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	CLK - $\overline{OUTn}$	t_{pLH1}	Test Circuit for Switching Characteristics V_{DD}=5.0 V V_{DS}=0.8 V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=372 Ω V_L=4.0 V R_L=64 Ω C_L=10 pF	-	100	150	ns
	LE/MOD/CA - $\overline{OUTn}$	t_{pLH2}		-	100	150	ns
	$\overline{OE}$/SW/$\overline{ED}$ - $\overline{OUTn}$	t_{pLH3}		-	50	150	ns
	CLK - SDO	t_{pLH}		15	20	-	ns
Propagation Delay Time ("H" to "L")	CLK - $\overline{OUTn}$	t_{pHL1}		-	50	100	ns
	LE/MOD/CA - $\overline{OUTn}$	t_{pHL2}		-	50	100	ns
	$\overline{OE}$/SW/$\overline{ED}$ - $\overline{OUTn}$	t_{pHL3}		-	20	100	ns
	CLK - SDO	t_{pHL}		15	20	-	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE/MOD/CA	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$/SW/$\overline{ED}$ (@ I_{out}< 60mA)	$t_{w(OE)}$		200	-	-	ns
Hold Time for LE/MOD/CA		$t_{h(L)}$		10	-	-	ns
Setup Time for LE/MOD/CA		$t_{su(L)}$		5	-	-	ns
Maximum CLK Rise Time		t_r***		-	-	500	ns
Maximum CLK Fall Time		t_f***		-	-	500	ns
Output Rise Time of Vout (turn off)		t_{or}		-	70	200	ns
Output Fall Time of Vout (turn on)		t_{of}		-	40	120	ns

*** If MBI5029 are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded LED drivers, MBI5029.

Test Circuit for Electrical Characteristics

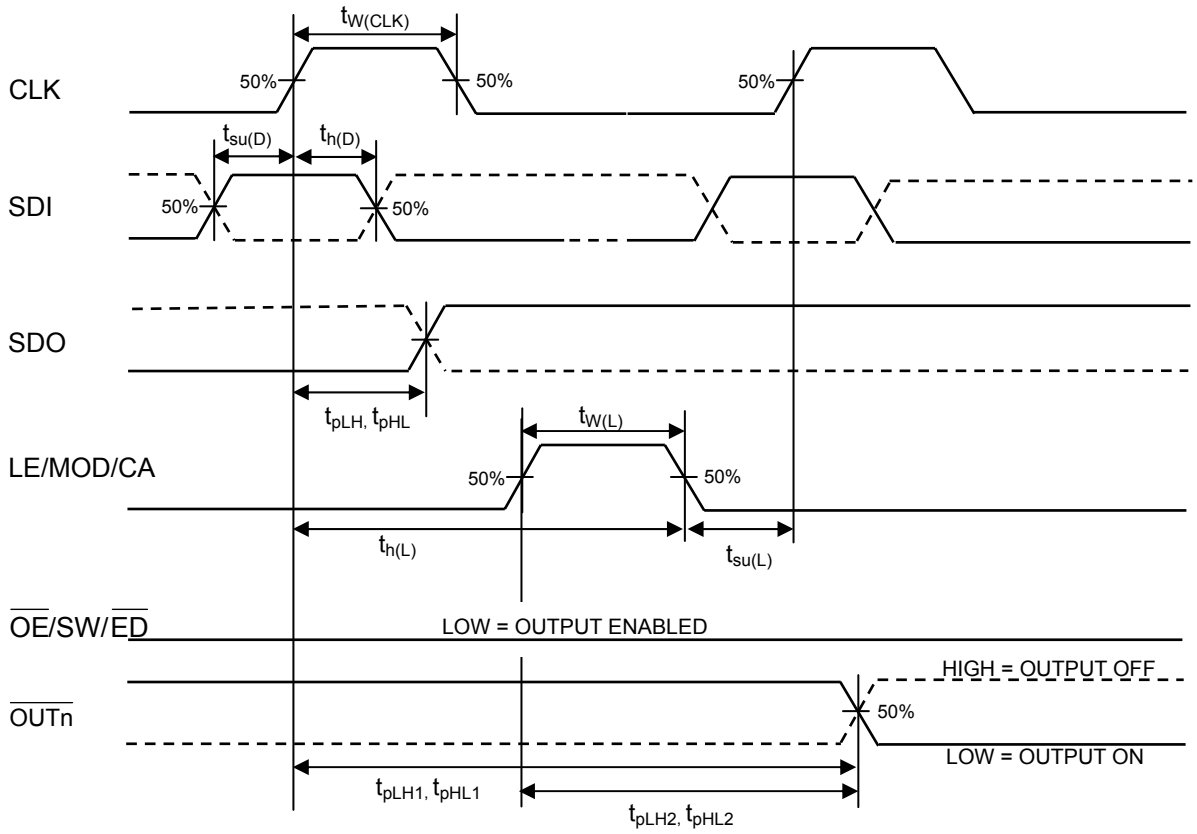


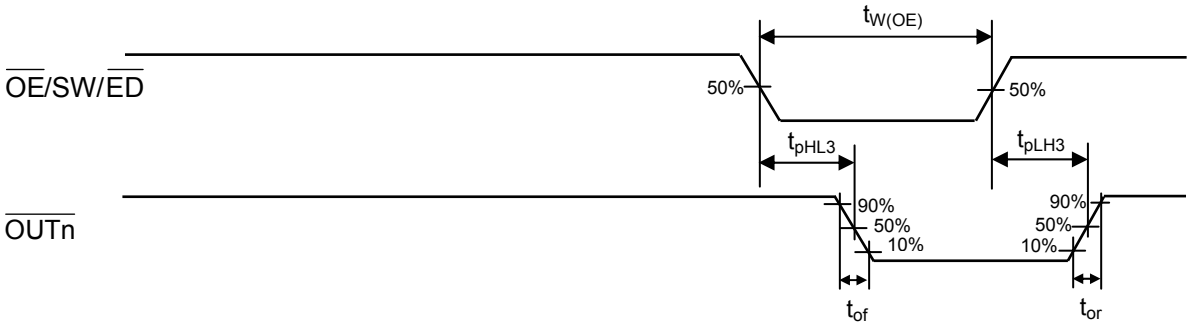
Test Circuit for Switching Characteristics



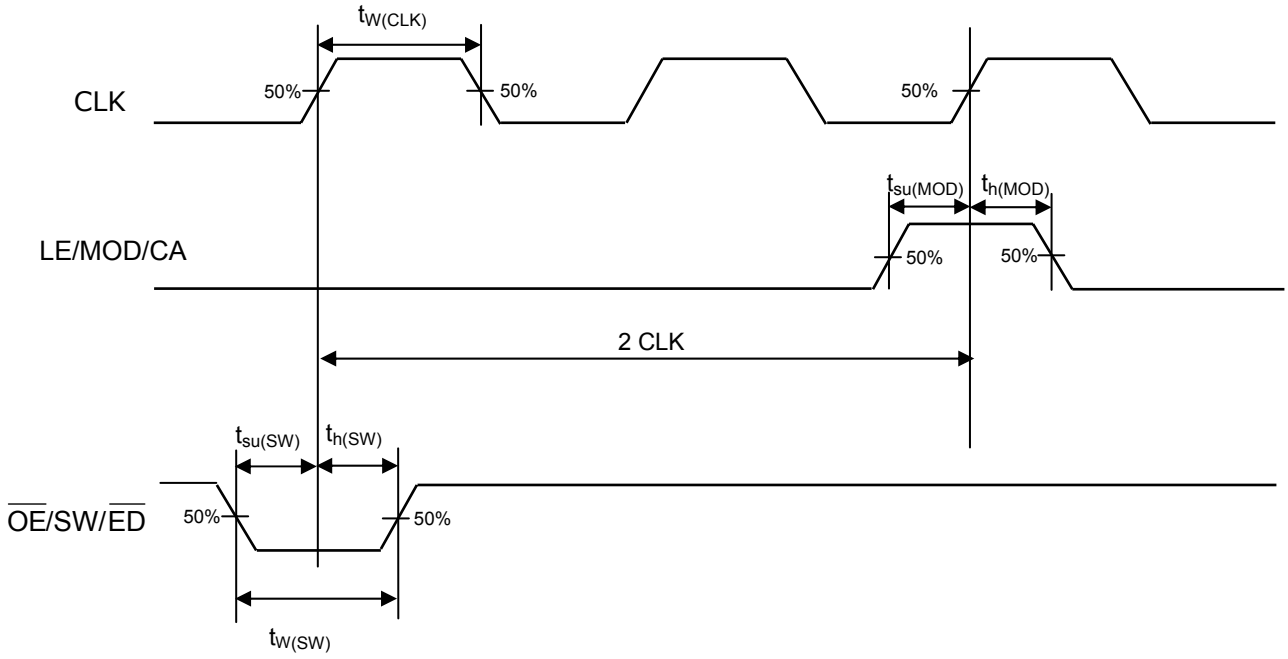
Timing Waveform

Normal Mode

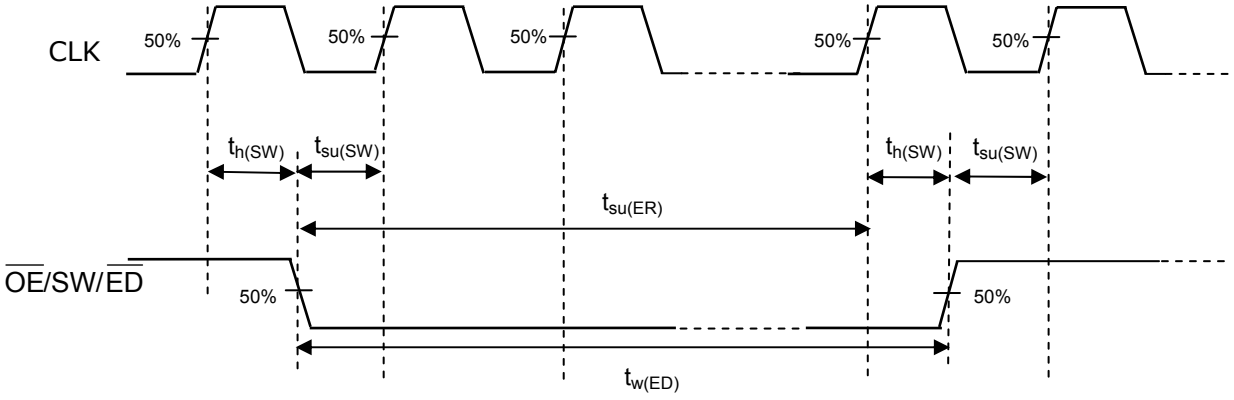




Switching to Special Mode



Reading Error Status Code



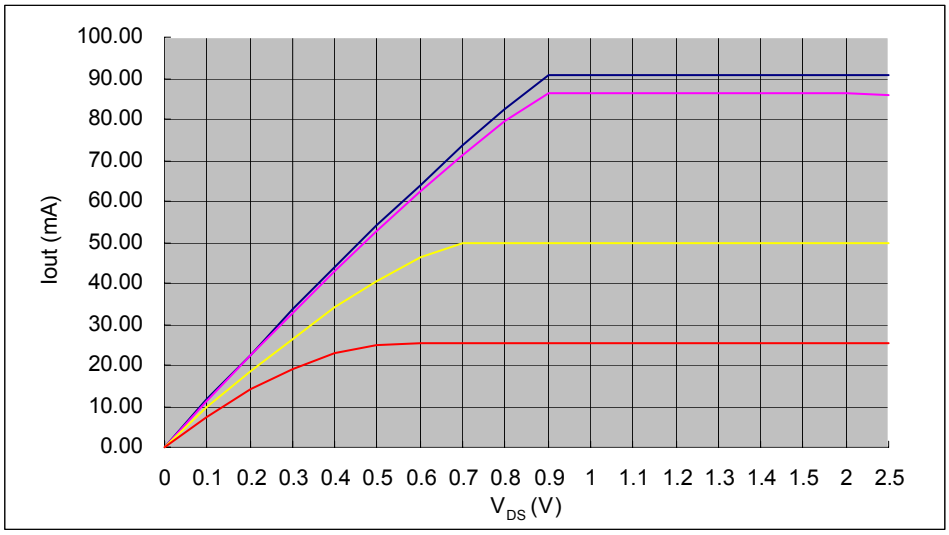
Operation Principle

Constant Current

In LED display applications, MBI5029 provides nearly no current variations from channel to channel and from IC to IC. This can be achieved by:

1) While $I_{OUT} \leqq 60mA$, the maximum current skew between channels is less than ±3% and that between ICs is less than ±6%.

2) In addition, the characteristics curve of output stage in the saturation region is flat and users can refer to the figure as shown below. Thus, the output current can be kept constant regardless of the variations of LED forward voltages (Vf). The output current level in the saturation region is defined as output target current $I_{out,target}$.



Adjusting Output Current

MBI5029 scales up the reference current I_{ref} set by the external resistor R_{ext} to sink a current I_{out} at each output port. Users can follow the below formulas to calculate the output current I_{out} in the saturation region:

$V_{R\text{-}EXT}$ = 1.4175Volt x G

$I_{ref} = V_{R\text{-}EXT} / R_{ext}$ if another end of the external resistor R_{ext} is connected to ground.

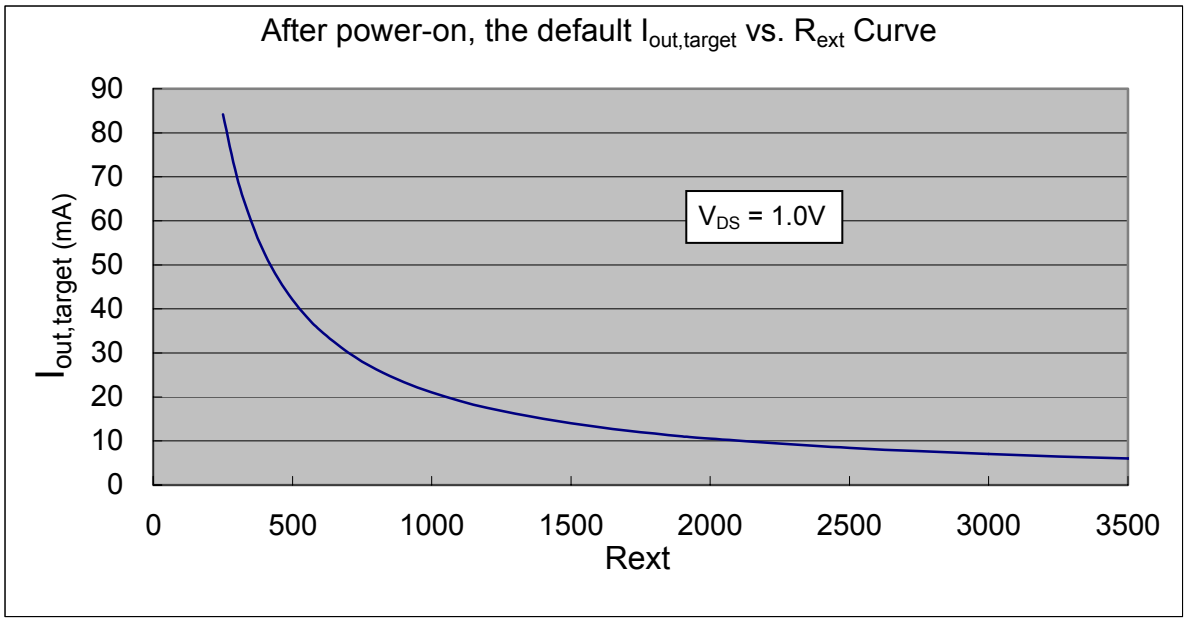
$I_{out,\ target} = I_{ref}$ x 15 = (1.4175Volt x G / R_{ext}) x 15

where R_{ext} is the resistance of the external resistor connected to the R-EXT terminal, and $V_{R\text{-}EXT}$ is the voltage of the R-EXT terminal and controlled by the programmable current gain G, which is defined by the Configuration Code. After power-on, the default value of G is 95/96 = 0.9896. Based on the default current gain,

$V_{R\text{-}EXT}$ = 1.4175Volt x 0.9896 = 1.40Volt

$I_{out,\ target}$ = (1.40Volt / R_{ext}) x 15

Hence, the default magnitude of current is around 52mA at 404Ω and 26mA at 809Ω. The default relationship after power-on between $I_{out,target}$ and R_{ext} is shown in the following figure.



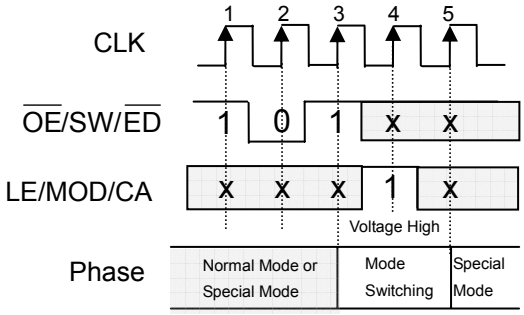
Resistance of the external resistor, R_{ext}, in Ω

Operation Phases

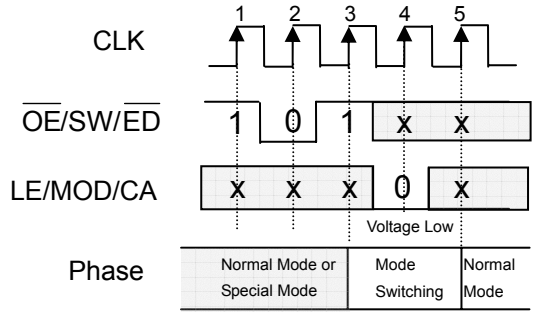
MBI5029 exploits the **Share-I-O™** technique to extend the functionality of pins in MBI5026 in order to provide LED load error detection and run-time programmable LED driving current in the Special Mode phase as well as the original function of MBI5026 in the Normal Mode phase. In order to switch between the two modes, MBI5029 monitors the signal $\overline{OE}$/SW/$\overline{ED}$. Once an one-clock-wide pulse of $\overline{OE}$/SW/$\overline{ED}$ appears, MBI5029 would enter the two-clock-period transition phase---the Mode Switching phase. After power-on, the default operation mode is the Normal Mode.

Operation Mode Switching

Switching to the Special Mode



Switching to the Normal Mode



As shown in the above figures, once a one-clock-wide short pulse "**101**" of $\overline{OE}$/SW/$\overline{ED}$ appears, MBI5029 would enter the Mode Switching phase. At the 4th rising edge of CLK, if LE/MOD/CA is sampled as "Voltage High", MBI5029 would switch to the Special Mode; otherwise, it would switch to the Normal Mode. Worthwhile noticing, the signal LE/MOD/CA between the 3rd and the 5th rising edges of CLK can not latch any data. Its level is just used for determining which mode to switch. However, the short pulse of $\overline{OE}$/SW/$\overline{ED}$ can still enable the output ports. During the mode switching, the serial data can still be transferred through the pin SDI and shifted out from the pin SDO.

Note:

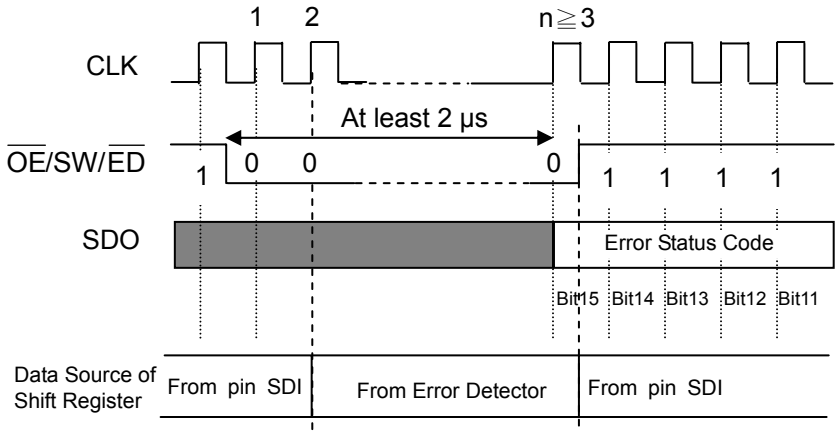
1. The signal sequence for the mode switching could be frequently used for making sure under which mode MBI5029 is working.
2. The aforementioned "1" and "0" are sampled at the rising edge of CLK. The "X" means its level would not affect the result of mode switching mechanism.

Normal Mode Phase

MBI5029 in the Normal Mode phase has similar functionality to MBI5026. The serial data could be transferred into MBI5029 via the pin SDI, shifted in the Shift Register, and go out via the pin SDO. The LE/MOD/CA can latch the serial data in the Shift Register to the Output Latch. $\overline{OE}$/SW/$\overline{ED}$ would enable the output drivers to sink current. The only difference is mentioned in the last paragraph about monitoring short pulse $\overline{OE}$/SW/$\overline{ED}$. The short pulse would trigger MBI5029 to switch the operation mode. However, as long as the signal LE/MOD/CA is not Voltage High in the Mode Switching phase, MBI5029 would still remain in the Normal Mode as if no mode switching occurs.

Special Mode Phase

In the Special Mode, as long as $\overline{OE}$/SW/$\overline{ED}$ is not at the Voltage Low, the serial data can still be shifted to the Shift Register via the pin SDI and shifted out via the SDO pin, as in the Normal Mode. But there are two differences between the Special Mode and the Normal Mode.

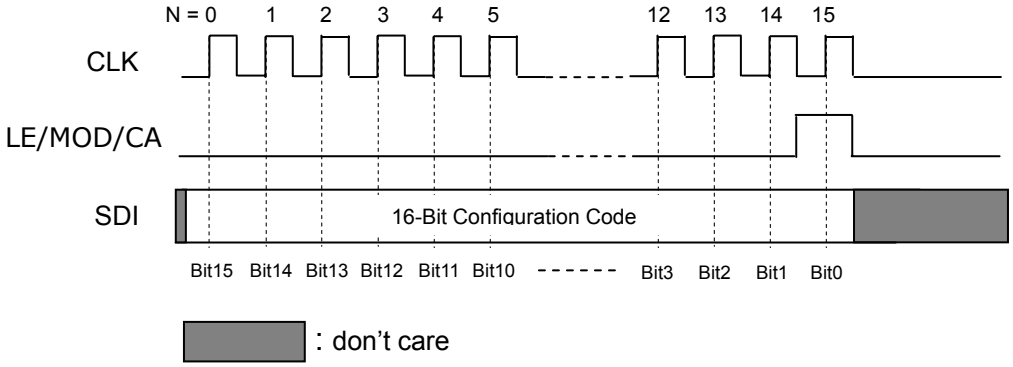


Reading Error Status Code (in Special Mode)

The first difference is that when the state of $\overline{OE}$/SW/$\overline{ED}$ is pulled down to Voltage Low, MBI5029 in the Special Mode would execute error detection and load error status codes into the Shift Register, as well as enabling output ports to sink current. The above figure shows the timing sequence for error detection. The shown "0" and "1" are sampled at the rising edge of each CLK. At least three "0" must be sampled at the Voltage Low signal $\overline{OE}$/SW/$\overline{ED}$. Just after the 2nd "0" is sampled, the data input source of the Shift Register would come from 16-bit parallel error status codes out of the circuit Error Detector, instead of serial data input via the pin SDI. Normally, the error status codes will be correctly generated at least 2µs after the falling edge of $\overline{OE}$/SW/$\overline{ED}$. The occurrence of the 3rd or later "0" results in the event that MBI5029 saves the detected error status codes into the Shift Register. Thus, when $\overline{OE}$/SW/$\overline{ED}$ is at the Voltage Low state, the serial data cannot be shifted into MBI5029 via the pin SDI. But when the state of $\overline{OE}$/SW/$\overline{ED}$ is pulled up to Voltage High from Voltage Low, the data input source of the Shift Register would again come from the pin SDI. At the same time, the output ports are disabled and the error detection is completed. Then, the error status codes saved in the Shift Register could be shifted out via the pin SDO bit by bit along with CLK, as well as the new serial data can be shifted into MBI5029 via the pin SDI.

The limitation is that in the Special Mode, it couldn't be allowed to **simultaneously** transfer serial data and detect LED load error status.

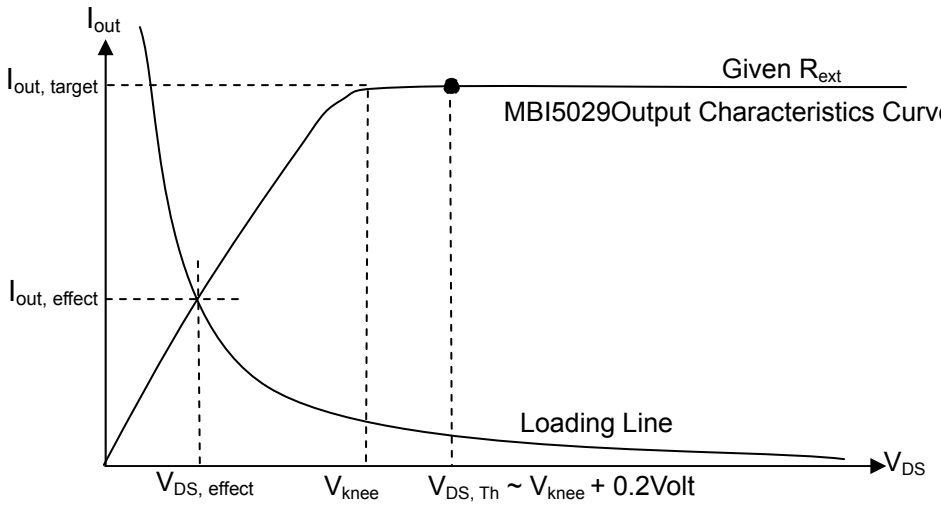
Writing Configuration Code



The second difference is that the active high signal LE/MOD/CA latches the serial data in the Shift Register to the Configuration Latch, instead of the Output Latch. The latched serial data is regarded as the Configuration Code. The code would be memorized until power off or the Configuration Latch is re-written. As shown above, the timing for writing the Configuration Code is the same as that in the Normal Mode for latching output channel data.

As aforementioned descriptions, both of Configuration Code and Error Status Code are transferred in common 16-bit Shift Register. Users must pay attention to the sequence of error detection and current adjustment to avoid the Configuration Code being overwritten by Error Status Code.

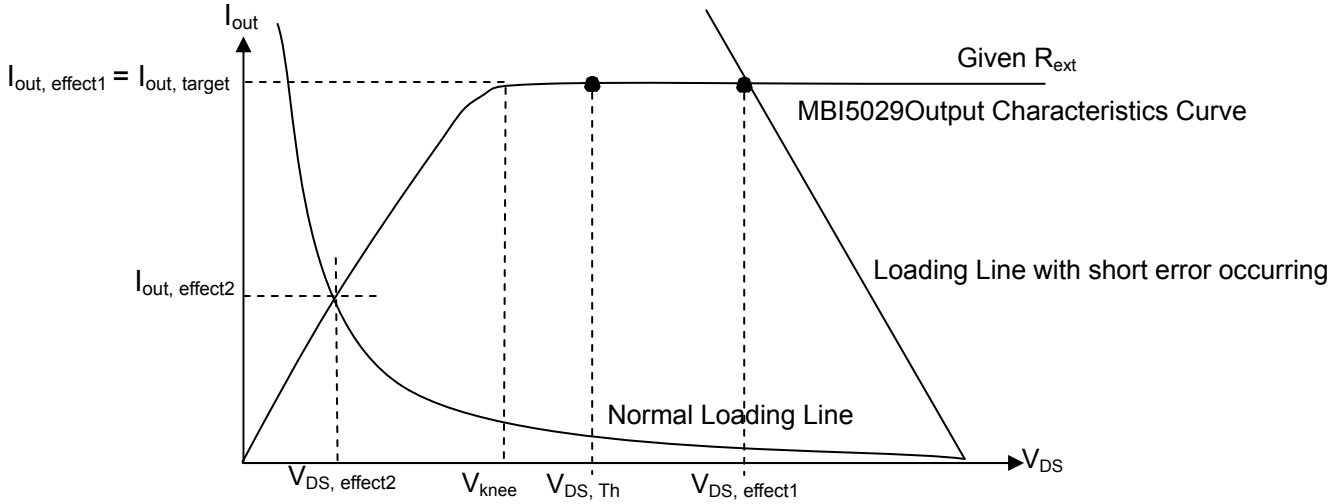
Open-Circuit Detection Principle



The principle of MBI5029 LED Open-Circuit Detection is based on the fact that the LED loading status is judged by comparing the effective current value($I_{out, effect}$) of each output port with the target current($I_{out, target}$) set by R_{ext}. As shown in the above figure, the knee voltage (V_{knee}) is the one between triode region and saturation region. The cross point between the loading line and MBI5029 output characteristics curve is the effective output point ($V_{DS, effect}$, $I_{out, effect}$).Thus, to detect the status of LED correctly, the output ports of MBI5029 must be enabled. The relationship between the Error Status code and the effective output point is shown below:

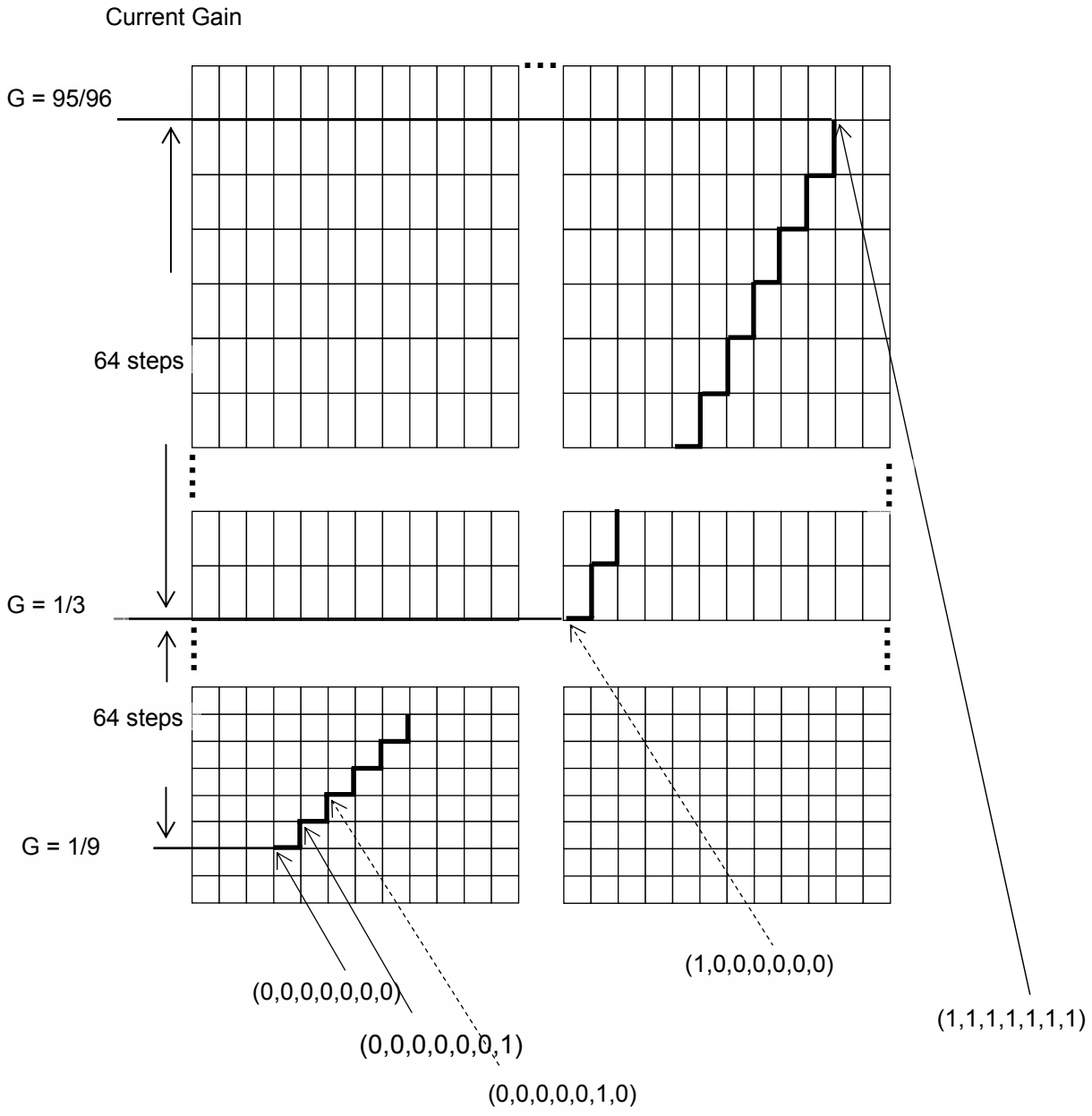
State of Output Port	Condition of Effective Output Point	Detected Open-Circuit Error Status Code	Meaning
OFF	$I_{out, effect} = 0$	"0"	-
ON	$I_{out, effect} \leqq I_{out, target}$ and $V_{out, effect} < V_{DS, Th}$	"0"	Open Circuit
	$I_{out, effect} = I_{out, target}$ and $V_{out, effect} \geqq V_{DS, Th}$	"1"	Normal
Note：the threshold voltage $V_{DS, Th}$ is around V_{knee} + 0.2Volt			

Short-Circuit Detection Principle



When LED is damaged, a short-circuit error may occur. To effectively detect the short-circuit error, LEDs need insufficiently biasing. The principle of MBI5029 LED Short Circuit Detection is based on the fact that the LED loading status is judged by comparing the effective current value($I_{out, effect}$) of each output port with the target current($I_{out, target}$) set by R_{ext}. When normal LED is insufficiently biased, its effective output point would be located at the ramp segment ($V_{DS} < V_{DS,Th}$) of MBI5029 Output Characteristics Curve, compared with LED with a short error falling within the flat zone ($V_{DS} \geqq V_{DS,Th}$). The relationship between the Error Status code and the effective output point is shown below:

State of Output Port	Condition of Effective Output Point	Detected Short-Circuit Error Status Code	Meaning
OFF	$I_{out, effect} = 0$	"0"	-
ON	$I_{out, effect} \leqq I_{out, target}$ and $V_{out, effect} < V_{DS, Th}$	"0"	Normal
	$I_{out, effect} = I_{out, target}$ and $V_{out, effect} \geqq V_{DS, Th}$	"1"	Short Circuit
Note：the threshold voltage $V_{DS, Th}$ is around V_{knee} + 0.2Volt			



16-Bit Configuration Code

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
Meaning	-	HC	CC0	CC1	CC2	CC3	CC4	CC5	-	-	-	-	-	-	-	-
Default Value	-	1	1	1	1	1	1	1	-	-	-	-	-	-	-	-

← 7-bit Current Adjust Code →

Note: "-" means "reserved and not used now"

After entering the Current Adjust mode, the system controller can sends 7-bit Current Adjust code to 16-bit Shift Register through MBI5029 SDI pin. Then sending LE/MOD/CA active pulse will transfer the contents in the Shift Register to a 16-bit Configuration Latch rather than the 16-bit Output Latch in a Normal mode. The 7-bit Current Adjust code in the Configuration Latch will directly affect the voltage at R-EXT terminal and output current $I_{out,target}$ by the current gain, G. The relationship between the Current Adjust Code {HC, CC〔0:5〕} and current gain G is shown below:

$$G = [(1 + 2 \times HC)/3] \times [(1 + D/32)/3]$$

where HC is 1 or 0 (HC=0 : Low current band; HC=1 : High current band) and

D = CC0 x 25+ CC1 x 24+ CC2 x 23+ CC3 x 22+ CC4 x 21+ CC5 x 20;

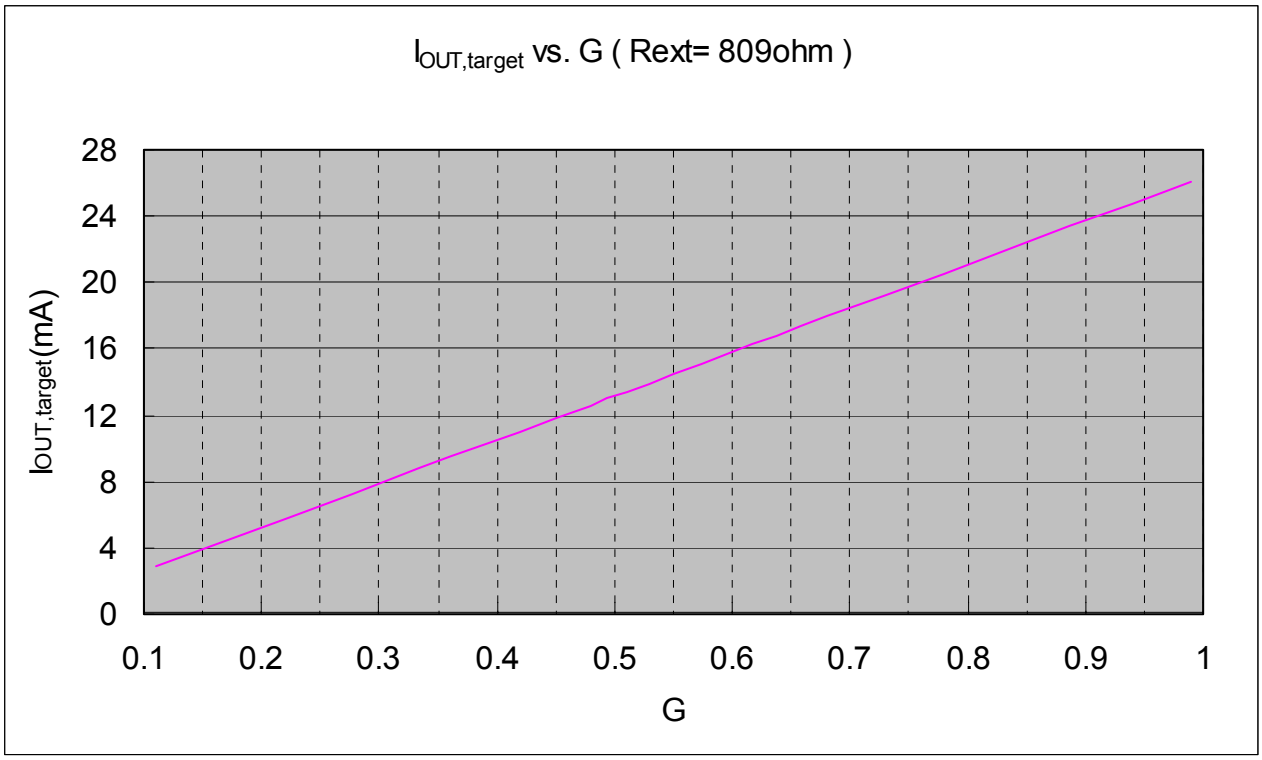
So, the Current Adjust Code is a floating number with one bit exponent HC and 6-bit mantissa.

For example,
when the Current Adjust Code is (1,1,1,1,1,1,1)
Gain, G = [(1 + 2 x 1)/3] x [(1 + 63/32)/3]= 0.9896

when the Current Adjust Code is (1,0,0,0,0,0,0)
Gain, G = [(1 + 2 x 1)/3] x [(1 + 0/32)/3]= 1/3

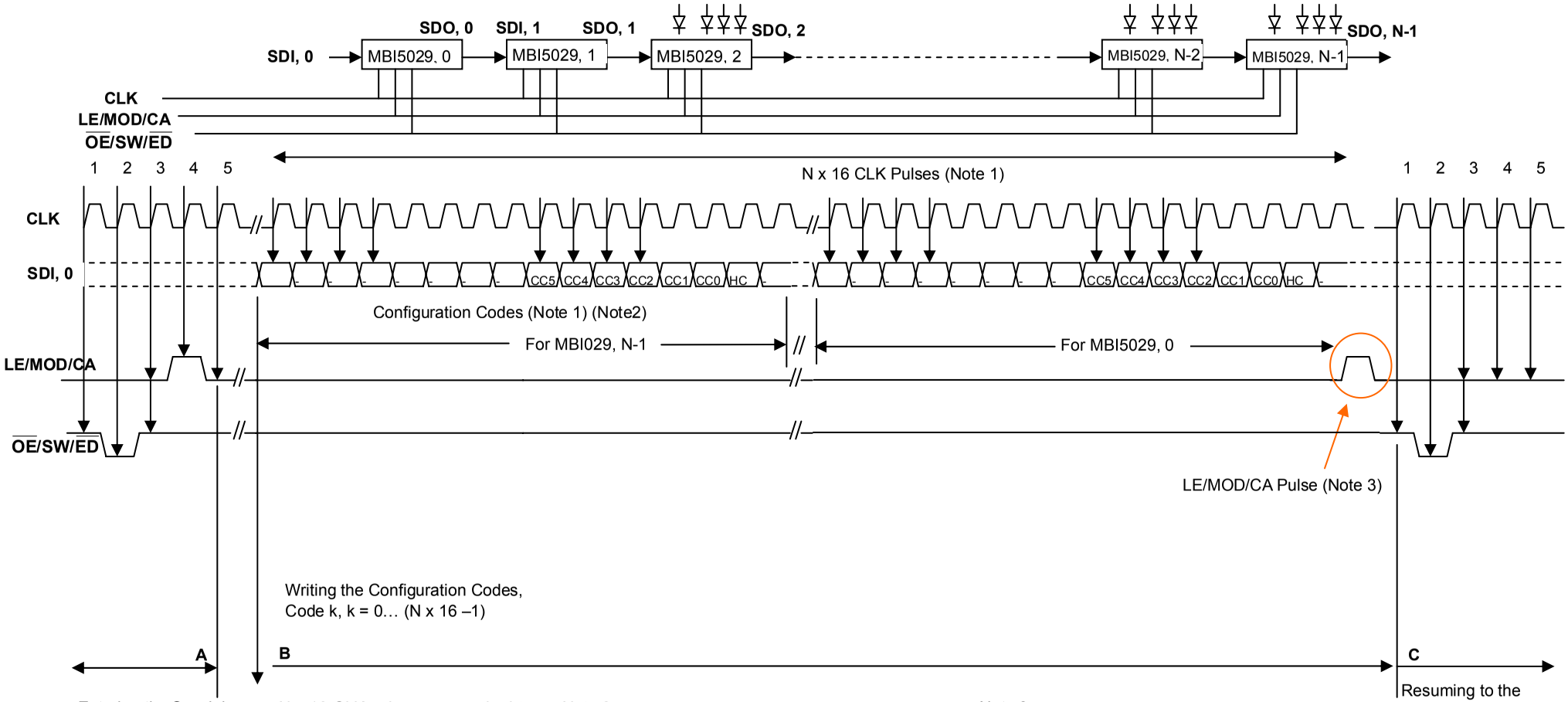
when the Current Adjust Code is (0,0,0,0,0,0,0)
Gain, G = [(1 + 2 x 0)/3] x [(1 + 0/32)/3]= 1/9

After power on, the default value of Current Adjust Code is (1,1,1,1,1,1,1). Thus, G is 0.9896.
Typically, the output current resulted by the digital current gain, G, is shown as the figure below.



Timing Chart for Current Adjust Mode (An Example)

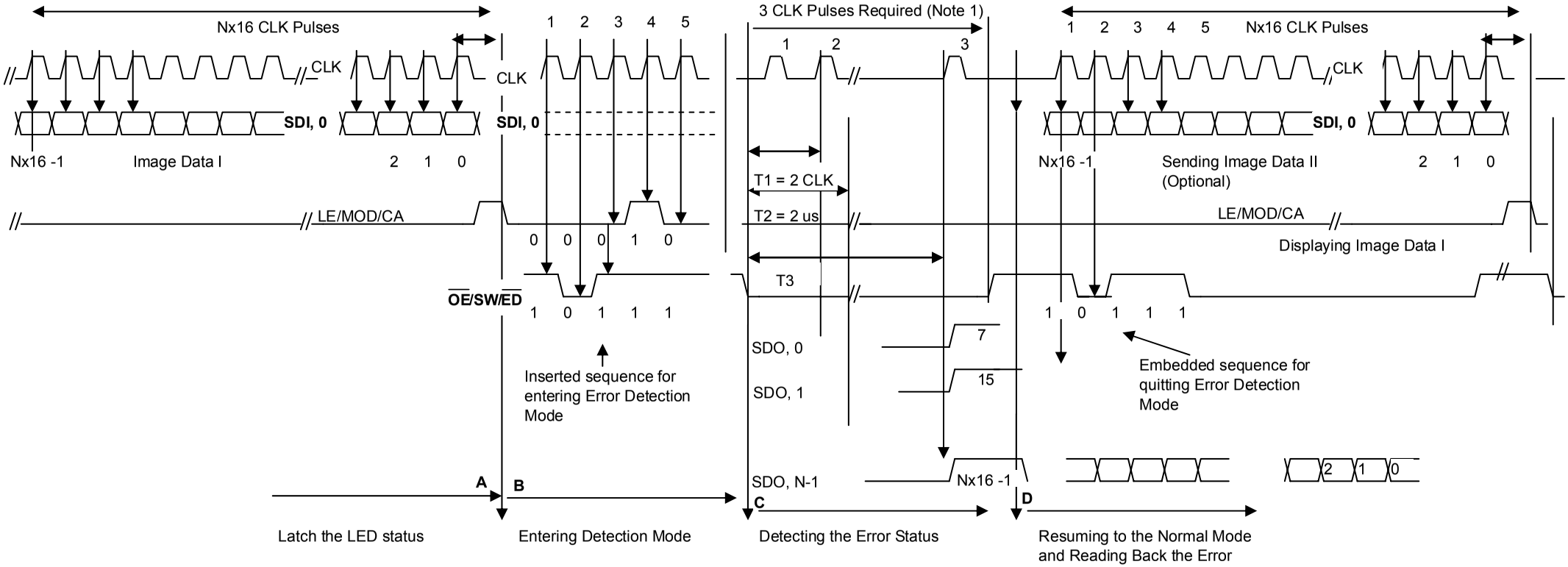
N of MBI5029 are connected in cascade, i.e., SDO, k --> SDI, k+1.
And, all MBI5029 are connected to the same signal bus CLK, LE/MOD/CA and $\overline{OE}$/SW/$\overline{ED}$.



Note 2:
Gain G = 〔(1+ 2 X HC)/3〕x (1 + D/32)/ 3
D = CC0 x 2^5+ CC1 x 2^4 + CC2 x 2^3 + CC3 x 2^2 + CC4 x 2^1 + CC5 x 2^0 .

Note 3:
The LE/MOD/CA pulse writes the Configuration Codes to each MBI5029.

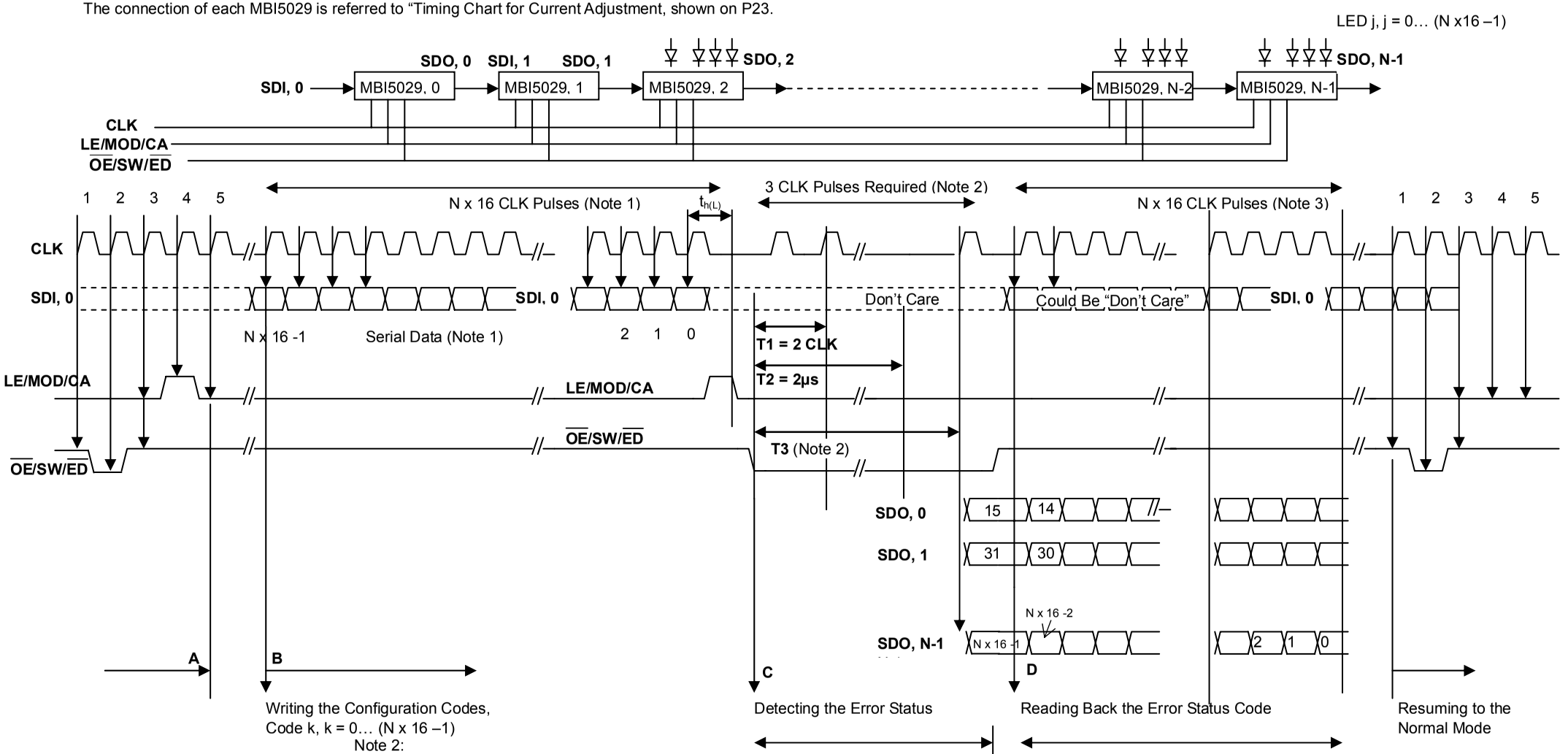
Timing Chart for Open-/Short- Circuit Detection Mode (An Example)



Note 1:
T1 = 2 CLK pluses is required to start the error detection. When Short-Circuit Detection is executed, LEDs should be insufficiently biased during this period.
T2 = 2 µs is required to obtain the stable error status result.
T3 = the third CLK pulses is required before **$\overline{OE}$/SW/$\overline{ED}$** goes voltage high. The rising edge of CLK writes the error status code back to the MBI5029 built-in shift register.

Timing Chart for Current Adjust Mode Plus Open-/Short- Circuit Detection Mode (An Example)

The connection of each MBI5029 is referred to "Timing Chart for Current Adjustment, shown on P23.



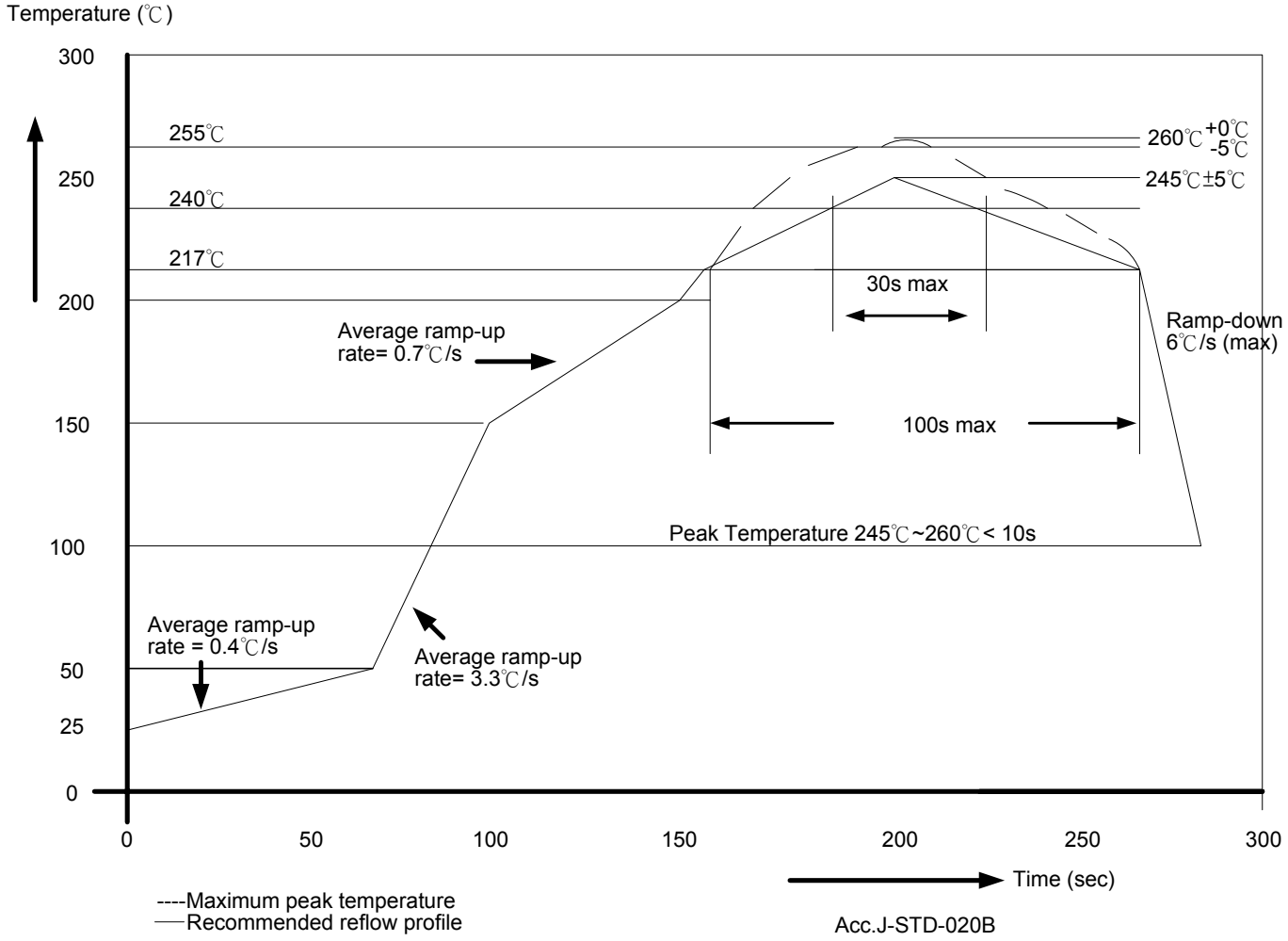
Note 1: N x 16 CLK pulses are required to shift the 8-bit Configuration Codes needed by N of MBI5029

Note 2:
T1 = 2 CLK pluses is required to start the error detection. When Short-Circuit Detection is executed, LEDs should be insufficiently biased during this period.
T2 = 2 µs is required to obtain the stable error status result.
T3 = the third CLK pulses is required before **OE/SW/ED** goes voltage high. The rising edge of CLK writes the error status code back to the MBI5029 built-in shift register.

Note 3:
The first rising edge of CLK after the rising edge of **OE/SW/ED** starts shifting the Image Data with LED Error. An LED error will be represented by a "0", to over write the original image data "1". Image Data k, k = 0… (N x 16 –1), = all "1" is suggested.
N x 16 CLK pulses shift all N x 16 error results (Error Status Code) via Node SDO, N-1.

Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defines "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected **100% pure tin** (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to standard 215ºC to 240ºC reflow processes which adopt tin/lead (SnPb) solder paste. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn), will all require up to 260°C for proper soldering on boards, referring to J-STD-020B as shown below.

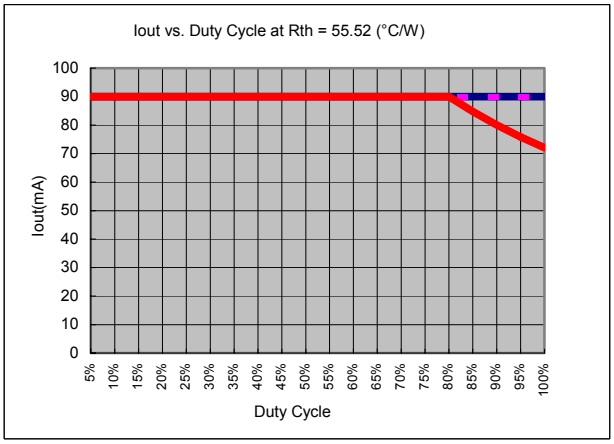


*Note1: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

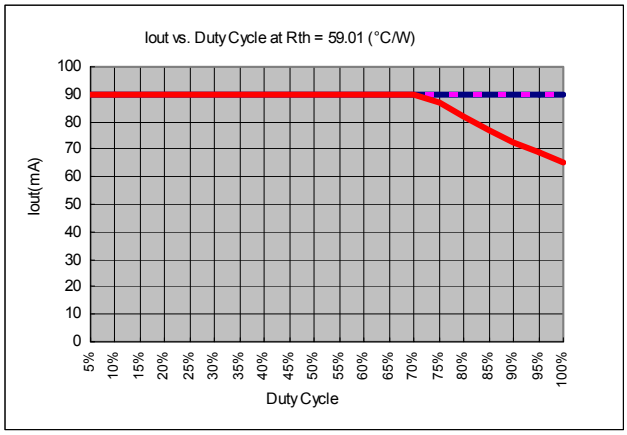
Package Power Dissipation (P_D)

The maximum allowable package power dissipation is determined as $P_D(max) = (Tj – Ta) / R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act) = (I_{DD} \times V_{DD}) + (I_{OUT} \times Duty \times V_{DS} \times 16)$. Therefore, to keep $P_D(act) \leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

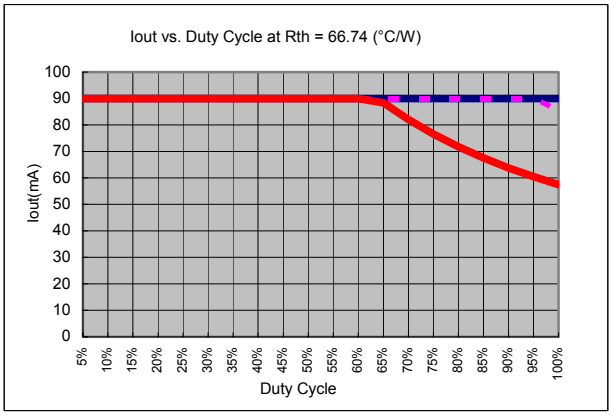
$I_{OUT} = \{ [(Tj – Ta) / R_{th(j-a)}] – (I_{DD} \times V_{DD}) \} / V_{DS} / Duty / 16,$
where Tj = 150°C.



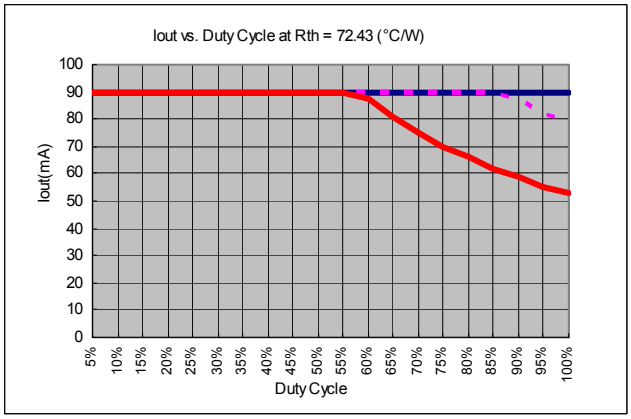
CN\GN type package



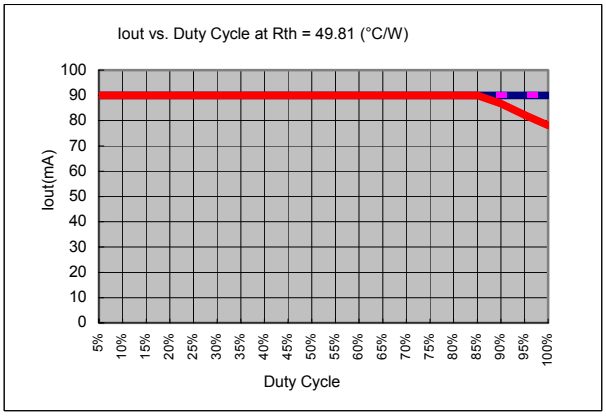
CF\GF type package



CNS\GNS type package



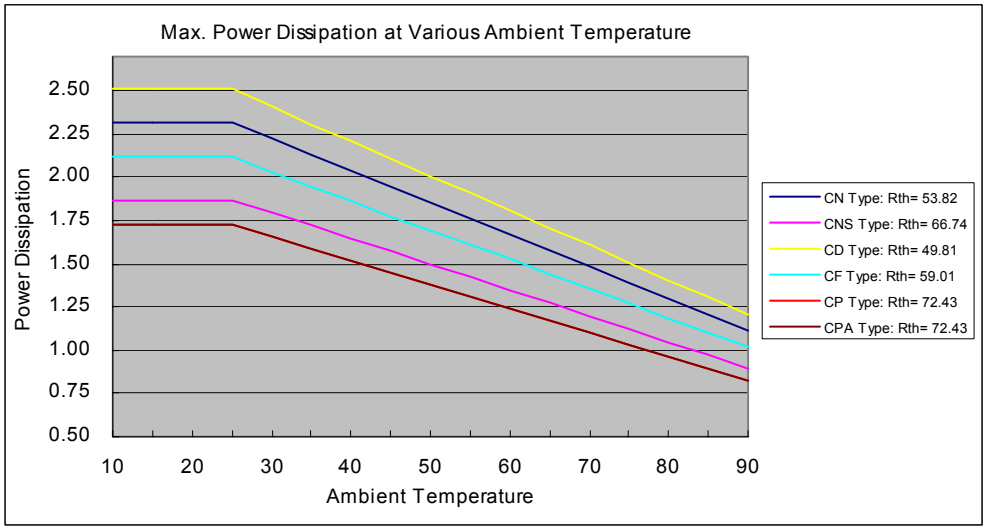
CP\CPA\GP\GPA type package



CD\GD type package

Condition : I_{out} = 90mA , V_{DS} = 1.0V , 16 output channels active				
Device Type		$R_{th(j-a)}$(°C/W)		Note
CN	GN	55.52	49.90	Ta = 25℃ Ta = 55℃ Ta = 85℃
CNS	GNS	66.74	62.28	
CD	GD	49.81	45.69	
CF	GF	59.01	52.38	
CP\CPA	GP\GPA	72.43	68.48	

The maximum power dissipation, $P_D(max) = (Tj – Ta) / R_{th(j-a)}$, decreases as the ambient temperature increases.

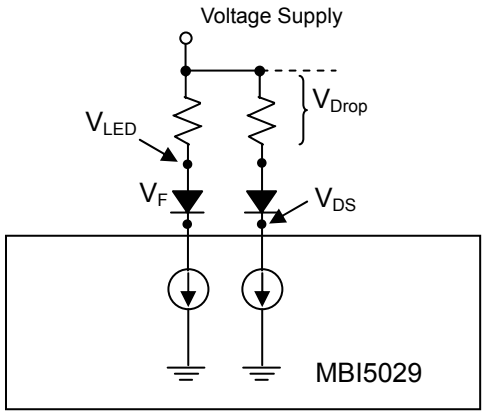


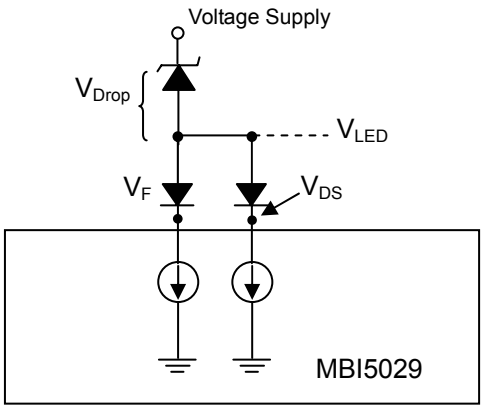
Load Supply Voltage (V_{LED})

MBI5029 are designed to operate with V_{DS} ranging from 0.4V to 1.0V considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D(act)} > P_{D(max)}$ when V_{LED} = 5V and $V_{DS} = V_{LED} – Vf$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer (V_{DROP}).

A voltage reducer lets $V_{DS} = (V_{LED} – Vf) – V_{DROP}$.

Resisters, or Zener diode can be used in the applications as the following figures.

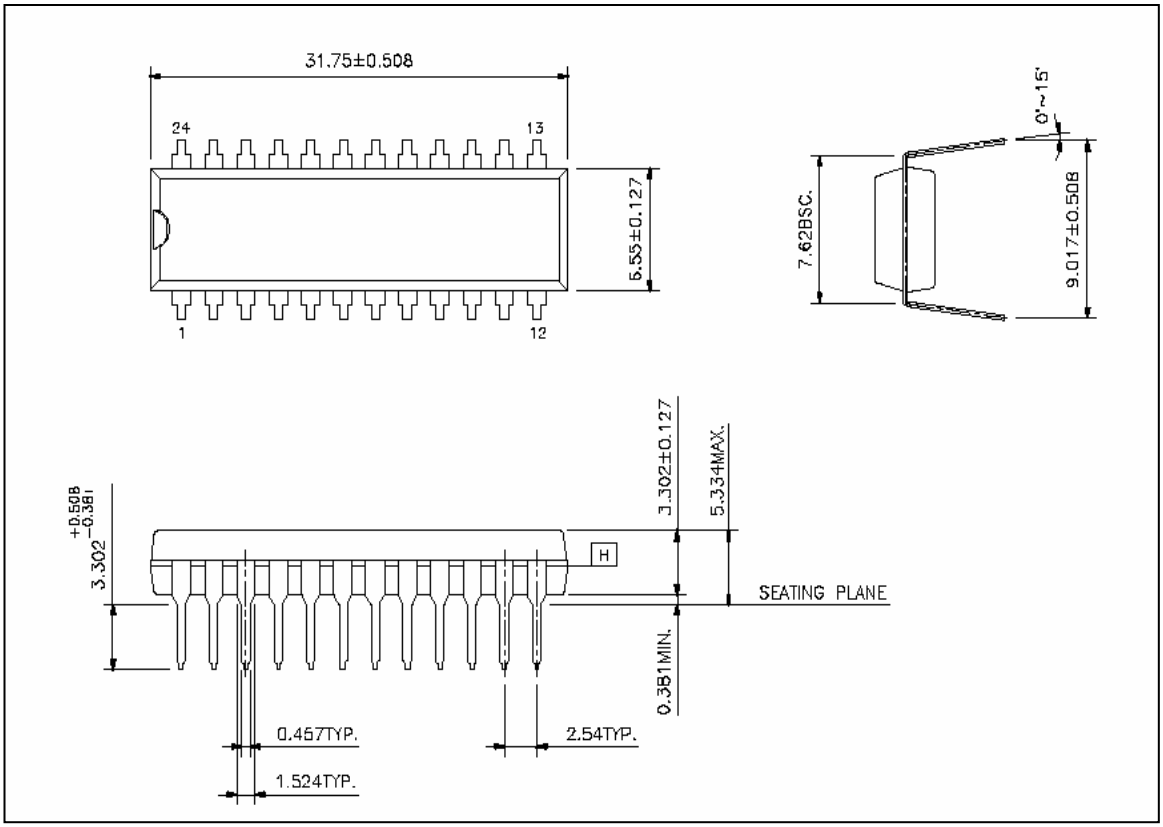




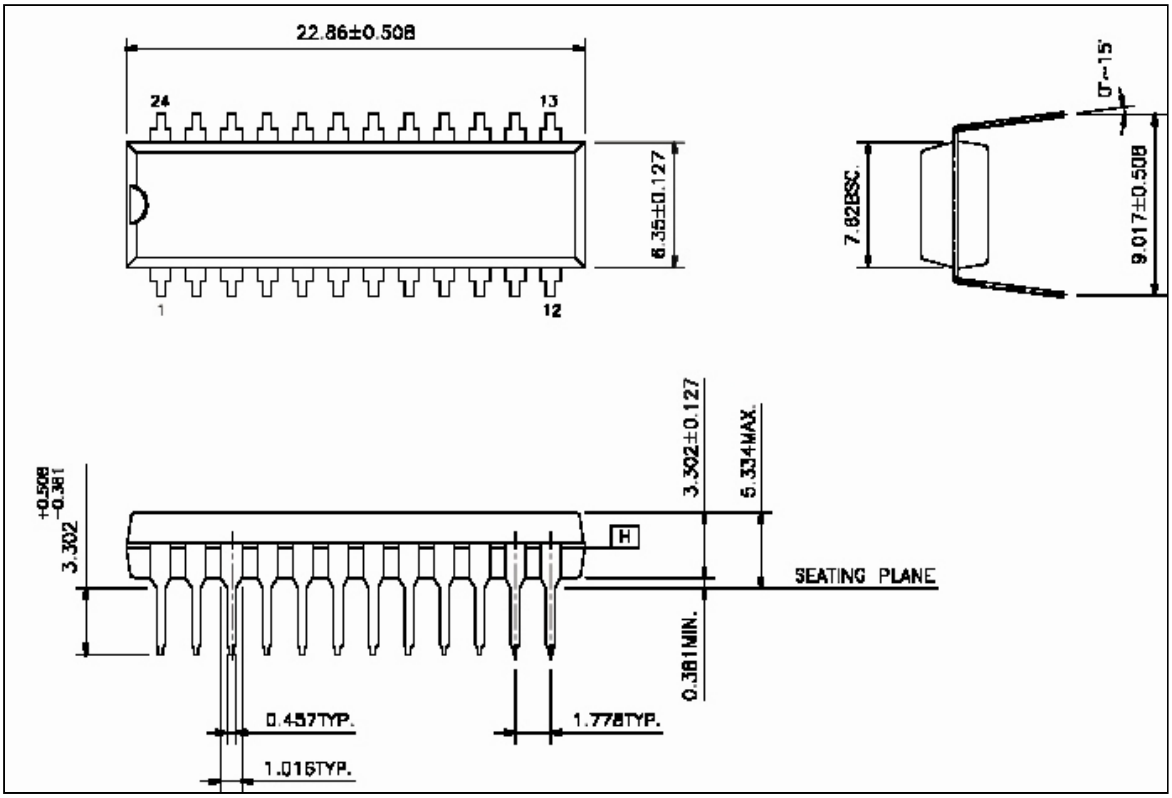
Switching Noise Reduction

LED Driver ICs are frequently used in switch-mode applications which always behave with switching noise due to parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

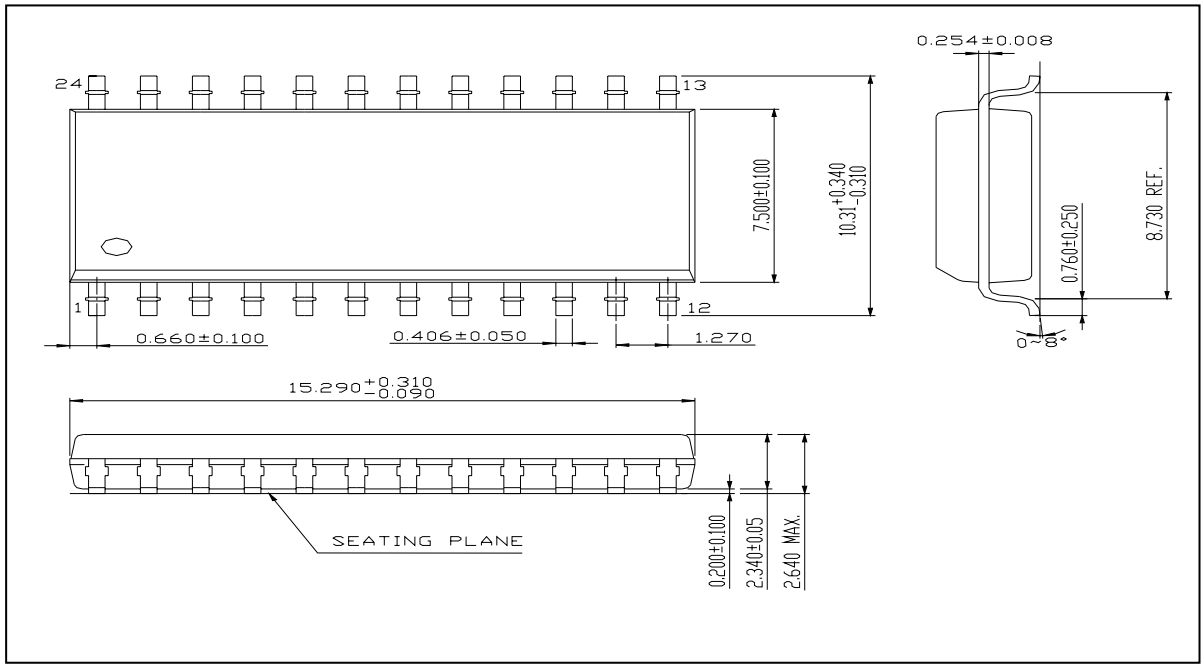
Package Outline



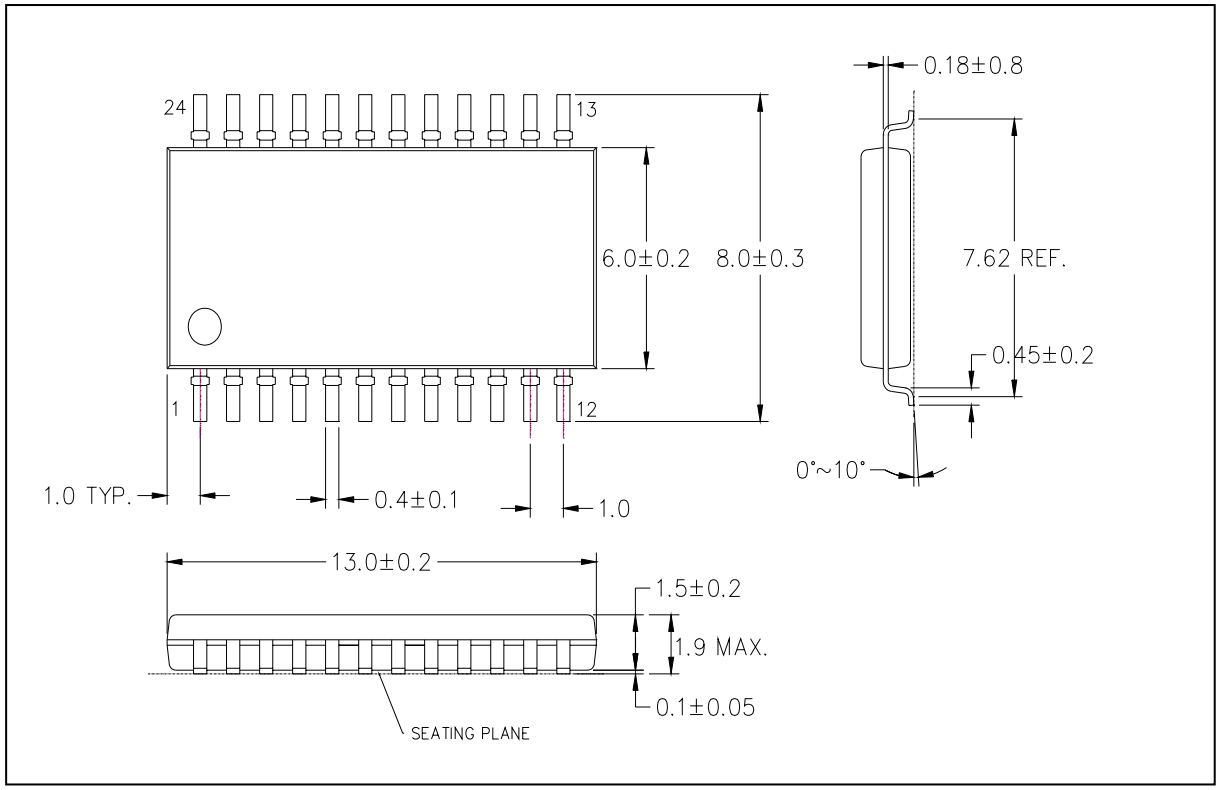
MBI5029CN\GN Outline Drawing



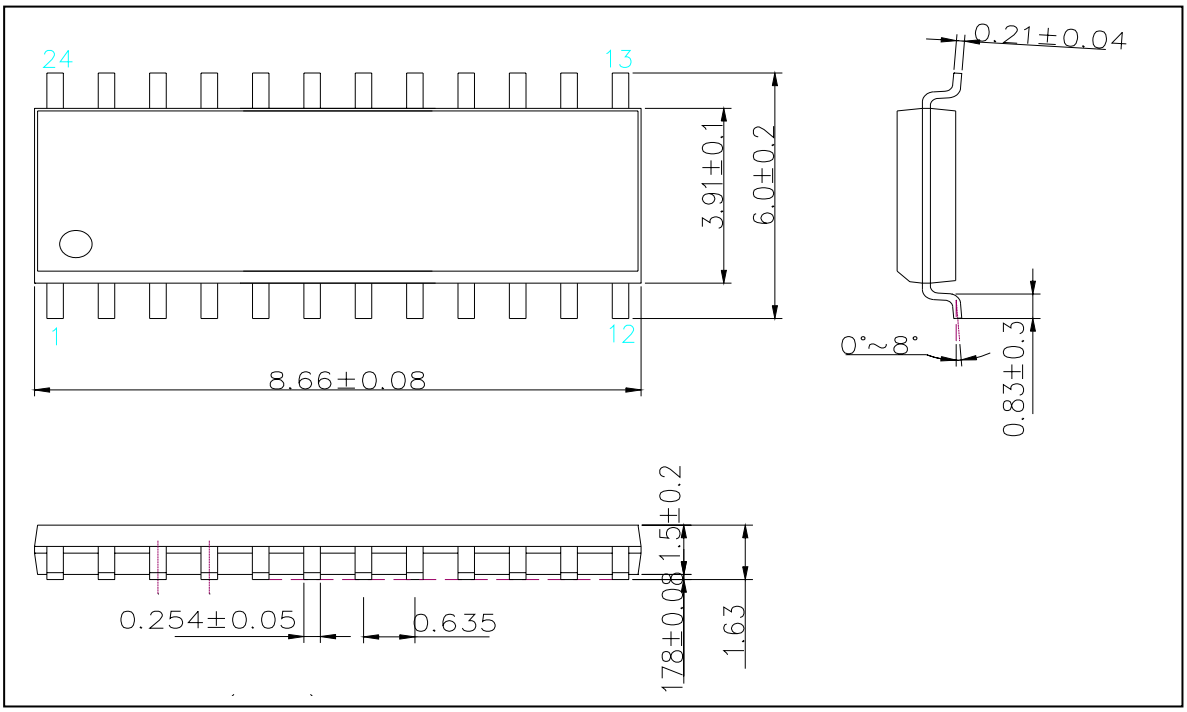
MBI5029CNS\GNS Outline Drawing



MBI5029CD\GD Outline Drawing



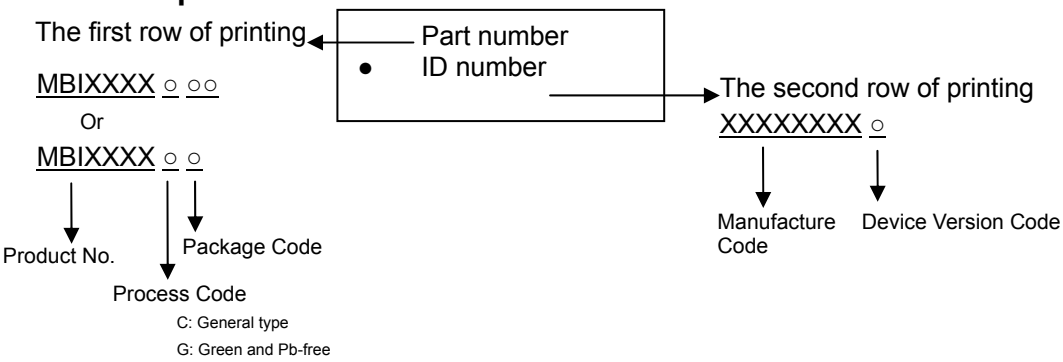
MBI5029CF\GF Outline Drawing



MBI5029CP\CPA\GP\GPA Outline Drawing

Note: The unit for the outline drawing is mm.

Product Top-mark Information



Product Revision History

Datasheet version	Device version code
VA.00	*Not defined*
VA.01	A
VA.02	A

Product Ordering Information

Part Number	Package Type	Weight (g)
MBI5029CN	P-DIP24-300-2.54	1.628
MBI5029CNS	SP-DIP24-300-1.78	1.11
MBI5029CD	SOP24-300-1.27	0.617
MBI5029CF	SOP24-300-1.00	0.28
MBI5029CP	SSOP24-150-0.64	0.11
MBI5029CPA	SSOP24-150-0.64	0.11

Part Number	"Pb-free & Green" Package Type	Weight (g)
MBI5029GN	P-DIP24-300-2.54	1.628
MBI5029GNS	SP-DIP24-300-1.78	1.11
MBI5029GD	SOP24-300-1.27	0.617
MBI5029GF	SOP24-300-1.00	0.28
MBI5029GP	SSOP24-150-0.64	0.11
MBI5029GPA	SSOP24-150-0.64	0.11