8-bit Parallel-In/Parallel-Out Constant Current Driver

Features

. Fast output current control, the minimum output enable pulse width = 80ns
. Current regulated output channels, constant current range: 5 – 100mA
. Built-in data latches and output enable function
. Excellent output current matching:

Current Skew		Conditions
Bit Skew	Chip Skew	
< ±3%	< ±6%	OE/ pulse width > 100ns , 30mA < Iout < 100mA
< ±4%	< ±8%	OE/ pulse width > 80ns , 5mA < Iout < 30mA

. All output current are adjusted through one external resistor
. Programmable interface:
(1) 5V CMOS level Schmitt triggered interface
(2) Discrete 3V input interface
. 5V supply voltage
. Packages: SOP24 and SSOP24

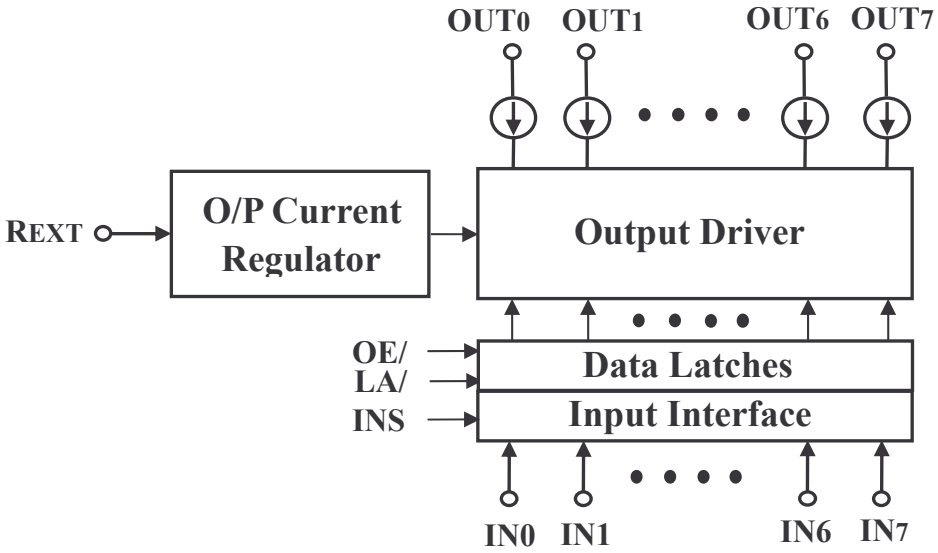
Product Description

The SCT2180 is designed to be a simple but effective solution for lighting LED. It drives up to eight LED clusters with regulate constant current for uniform intensity.

In applications, an external resistor is used to set the full-scale LED current from 5mA to 100mA. The SCT2180 guarantees each output can endure maximum 7V DC voltage stress. The on/off state of outputs are controlled by each input data bit (IN0~IN7), signals of latch (LA/) and output enable (OE/). Combing schemes of parallel data inputs and the finest output current pulse, the SCT2180 can easily realize high quality LED displays which are used to display true color motion pictures.

StarChips **Technology, Inc.**
4F, No.5, Technology Rd., Science-Based Industrial Park, Hsin-Chu, Taiwan, R.O.C
TEL: 03-577-5767 FAX: 03-577-6575 E-mail: contact@starchips.com.tw

Block Diagram



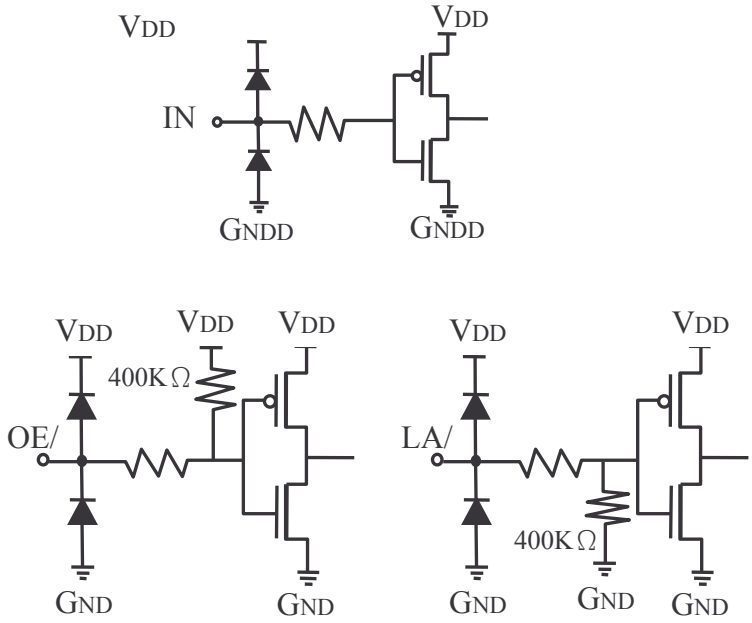
Terminal Description

Pin No.	Pin Name	Function
1	OE/	Output enable input signal, low active.
2, 15	GNDD	Digital ground terminals.
4	GNDA	Analog ground terminal.
3, 5, 11, 12, 13, 14 20, 22	IN0~IN7	Digital data inputs.
6, 7, 8, 9, 16, 17, 18, 19	OUT0~OUT7	Output terminals.
10	INS	Interface select input signal. When INS='L' select 5V Schmitt trigger interface. Let INS='H' select 3V discrete input.
21	LA/	Latch input signal. LA/='H' input data transparent to output. When LA/='L', input data are latched.
23	REXT	Full-scale output current set input. Connect a resistor from REXT to GND set the output current.
24	VDD	5V supply voltage terminal.

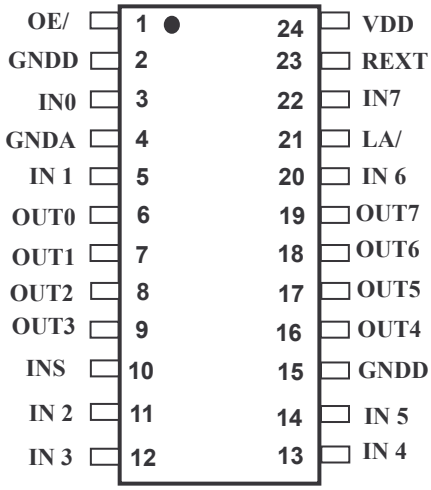
Truth Table

DIN	LA/	OE/	OUTPUT Function
X	L	L	Q_N ; previous state
L	H	L	OFF ; LED off
H	H	L	ON ; LED on
X	X	H	OFF ; LED off

Equivalent Circuits of Inputs



Pin Configuration



Ordering information

Part Number	Marking	Package
SCT2180ASON	SCT2180ASON	Normal SOP24
SCT2180ASSN	SCT2180ASSN	Normal SSOP24
SCT2180ASOG	SCT2180ASOG	Pb free SOP24
SCT2180ASSG	SCT2180ASSG	Pb free SSOP24

Maximum Ratings

Characteristic	Symbol	Rating	Unit
Supply voltage	V_{DD}	4.0 ~ 7.0	V
Input voltage	V_{IN}	-0.2 ~ V_{DD}+0.2	V
Output current	I_{OUT}	+120	mA
Output voltage	V_{OUT}	0.8~7.0	V
Data switching rate	F_{IN}	8	MHz
Total GND terminals current	I_{GND}	1000	mA
Operating temperature	T_{OPR}	-40~+85	°C
Storage temperature	T_{STG}	-55~+150	°C

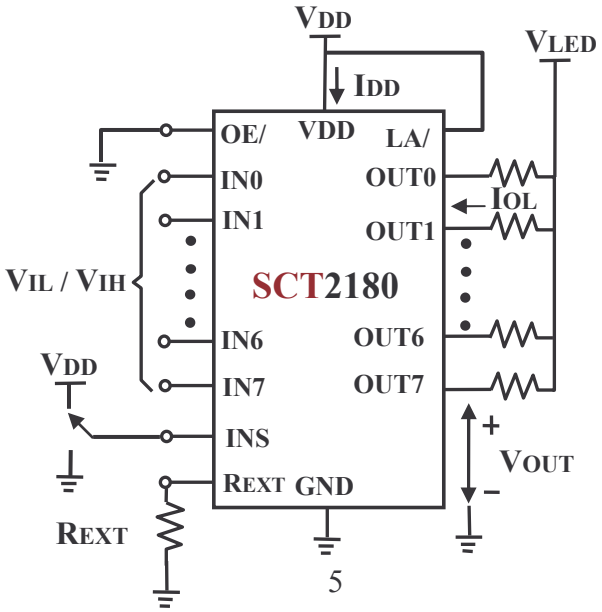
Recommended Operating Conditions (Ta=-40 to 85 °C unless otherwise noted)

Characteristic	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Supply voltage	V_{DD}	-	4.5	5.0	5.5	V
Output voltage	V_{OUT}	OUT0 ~ OUT15	1.0	-	V_{DD}	V
Output current	I_{OUT}	DC test circuit	5	-	100	mA
Input voltage (INS=L)	V_{IH}	-	0.8V_{DD}	-	V_{DD}	V
	V_{IL}	-	0	-	0.2V_{DD}	V
Input voltage (INS=H)	V_{IH}	-	2.0	-	V_{DD}	V
	V_{IL}	-	0	-	0.4	V
OE/ pulse width	t_{w2}	V_{DD}=4.5~5.5V	80	-	-	ns
Data rate	F_{IN}	-	-	-	5	MHz

Electrical Characteristics

Characteristic		Symbol	Condition		Min.	Typ.	Max.	Unit
Input voltage (INS=L)		V_{IH}			$0.8V_{DD}$	-	V_{DD}	V
		V_{IL}			0	-	$0.2V_{DD}$	V
Input voltage (INS=H)		V_{IH}			2	-	V_{DD}	V
		V_{IL}			0	-	0.4	V
Output leakage current		I_{OL}	V_{OH} = VDD = 7V		-	-	0.5	μA
Output current		I_{OUT}	V_{OUT}=1.0V	R_{EXT}=900 Ω	-	40	-	mA
Current bit skew		dI_{OUT}	I_{OL}=40mA V_{OUT}=1.0V F_{IN}<5MHz	R_{EXT}=900 Ω	-	±1	±3	%
Iout vs. supply voltage regulation		%/dV_{DD}	4.5V <V_{DD} < 5.5V V_{OUT} > 1.0 V		-	-	±1	%/V
Iout vs. output voltage regulation		%/dV_{OUT}	1.0V < V_{OUT} < 4.0V I_{OL}=50mA, V_{DD} = 5V		-	-	±1	%/V
Supply current	OFF	$I_{DD(off)\ 1}$	R_{EXT} = Open ,V_{DD} = 5V OUT0~OUT7=Off		-	12	15	mA
	OFF	$I_{DD(off)\ 2}$	R_{EXT} = 900 Ω,V_{DD} = 5V OUT0~OUT7=Off		-	13	15	
	ON	$I_{DD(on)}$	R_{EXT} = 900 Ω,V_{DD} = 5V OUT0~OUT7=On		-	13	15	

Test Circuit for Electrical Characteristics

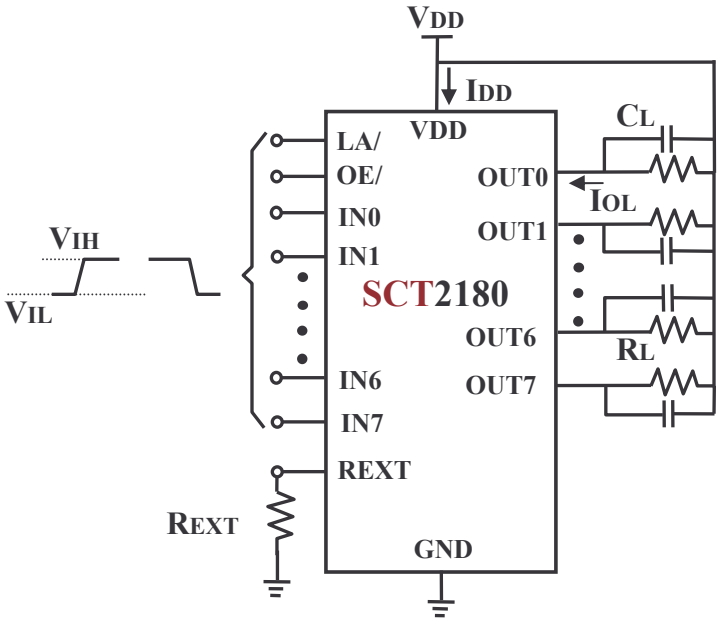


Switching Characteristics

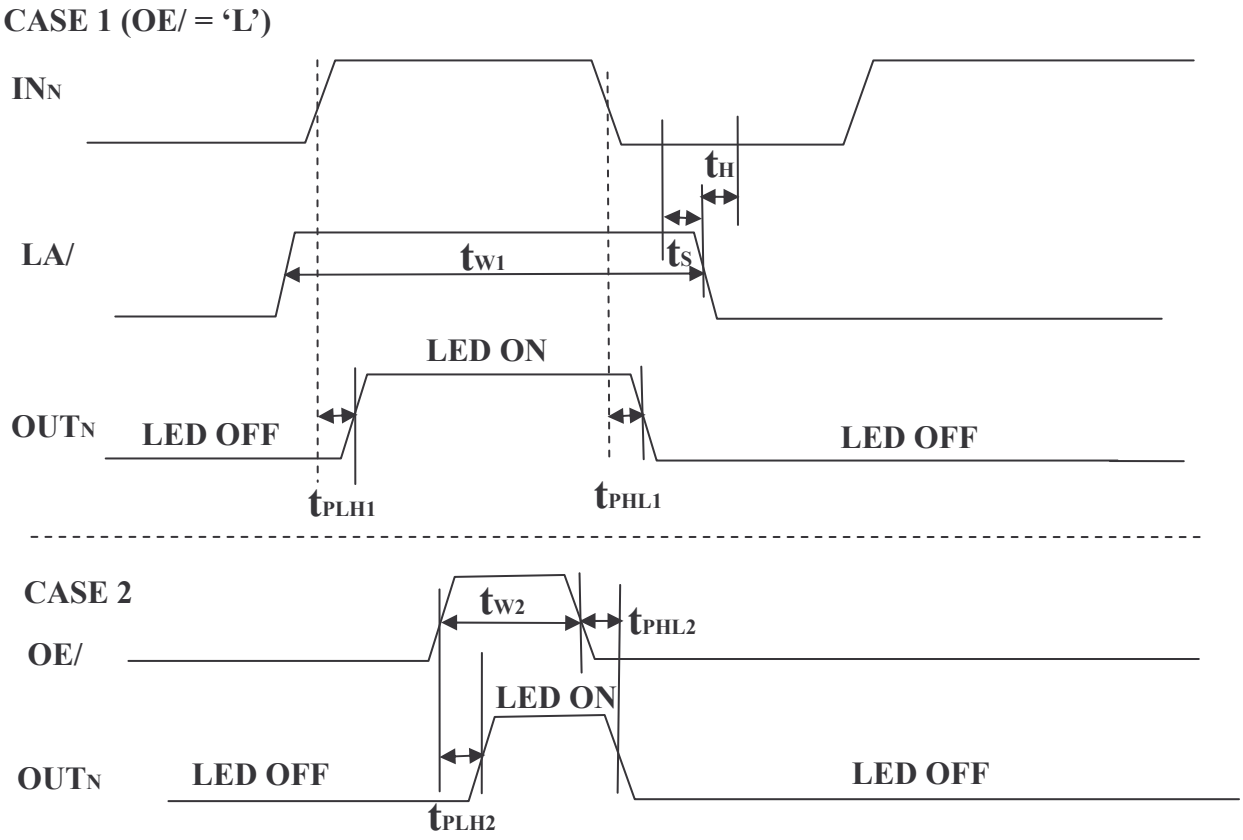
(VDD=5.0V, Ta=25ºC unless otherwise noted)

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	LA/ - OUTn	t_{PLH1}	V_{DD} = 5.0 V V_{LED} = V_{DD} V_{IH} = V_{DD} V_{IL} = GND R_{EXT} = 900 Ω R_L = 75 Ω C_L = 10 pF	-	50	100	ns
	OE/ - OUTn	t_{PLH2}		-	30	60	ns
Propagation Delay Time ("H" to "L")	LA/ - OUTn	t_{PHL1}		-	50	100	ns
	OE/ - OUTn	t_{PHL2}		-	30	60	ns
Pulse Width	LA/	t_{w1}		20	-	-	ns
	OE/	t_{w2}		100			ns
Hold Time for LA/		t_H		5	-	-	ns
Setup Time for LA/		t_S		5	-	-	ns
Output Rise Time of Iout				-	10	25	ns
Output Fall Time of Iout				-	10	25	ns

Test Circuit for Switching Characteristics

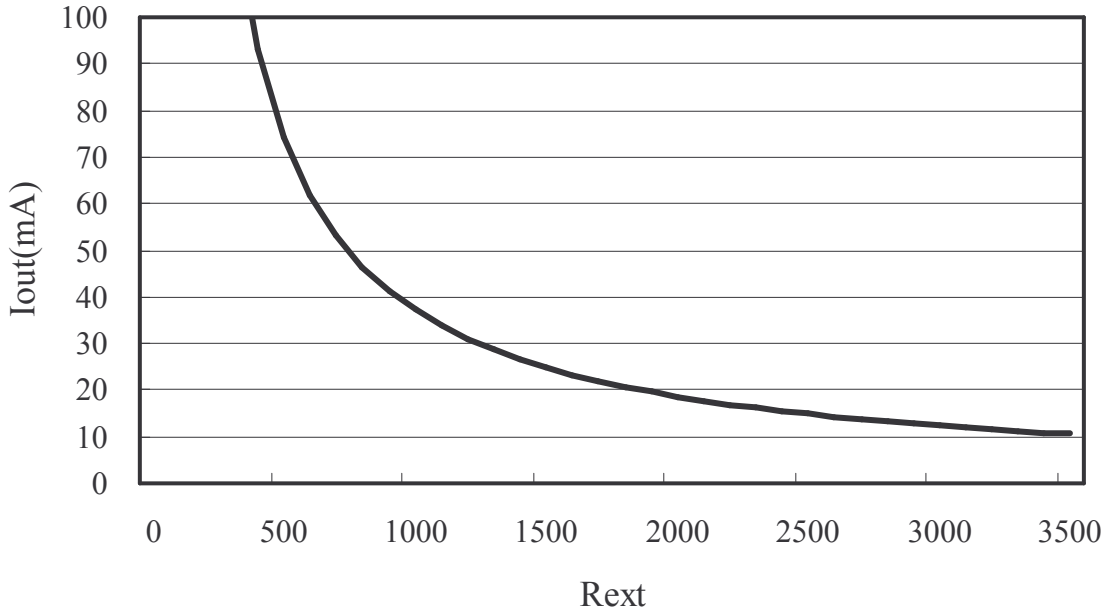


Timing Waveform



Adjusting Output Current

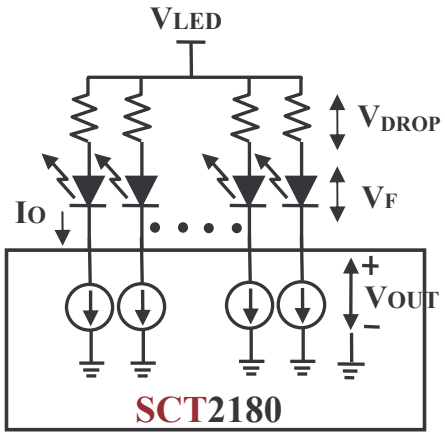
All SCT2180's output current (I_{OUT}) are set by one external resistor at pin REXT. The relationship between I_{OUT} and resistance R_{EXT} is shown as the following figure.

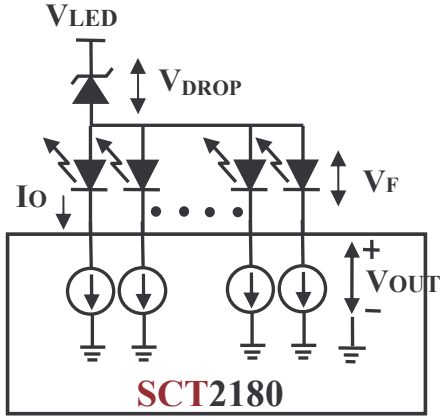


Also, when SCT2180's output voltage is set between 1.0 Volt and 4.0 Volt, the output current can be estimated approximately by : $I_{OUT} = 60(620 / R_{EXT})$ (mA)
Thus the output current are all set to be about 41mA at $R_{EXT} = 900\Omega$.

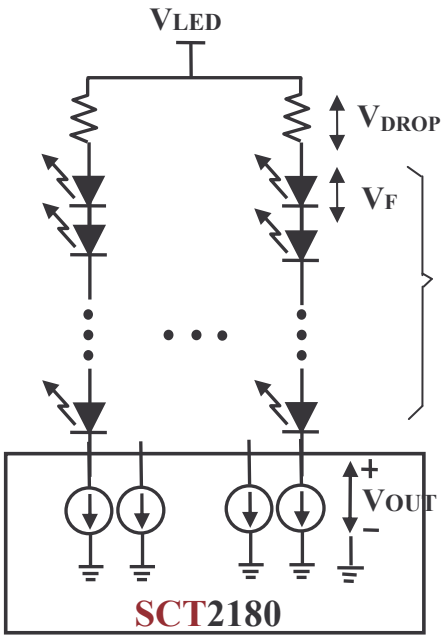
Load Supply Voltage (V_{LED})

SCT2180 can operate very well only when V_{OUT} ranging from 1.0V to 4.0V. So it is recommended to use the lowest possible supply voltage or set a voltage reducer to reduce the V_{OUT} voltage. A voltage reducer lets $V_{OUT} = V_{LED} - V_{DROP} - V_F$. Resistors or Zener diode can be used in the applications as shown in the following figures.





VLED'S LIMITATION



N • (VF-0.7) + 7 > VLED = N • VF +VOUT
and N < (7-VOUT)/0.7

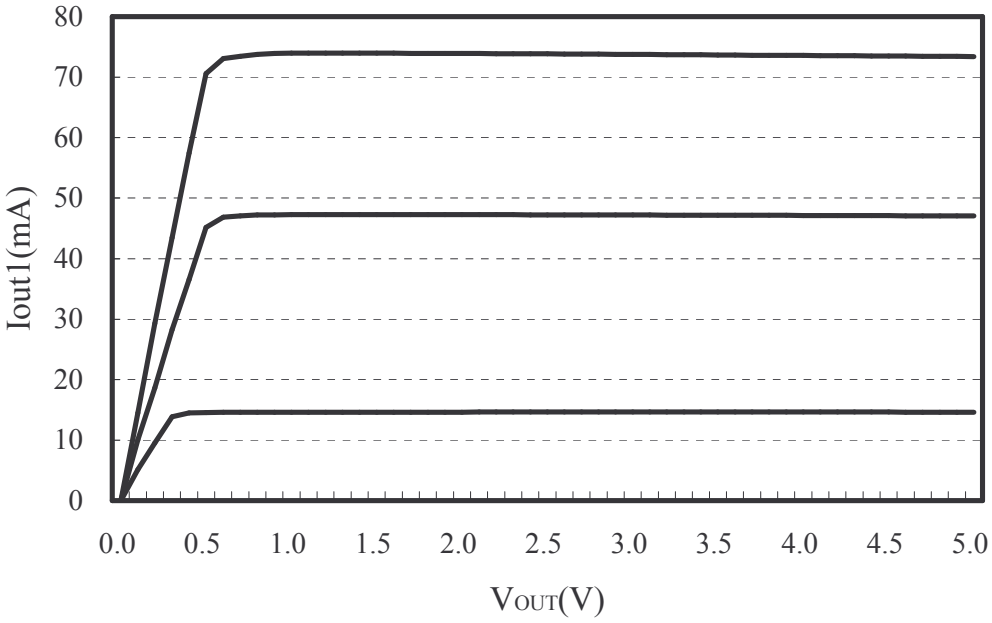
VF=LED's forward voltage

For example :
Let VF= 2.1V , VCC=5V and VOUT > 1V
N < (7-1)/0.7= 8, thus we can use 6 LED
And we have 6 • (2.1-0.7)+7 > VLED > 6 • 2.1 + 1

That is 15.4V > VLED > 13.6V

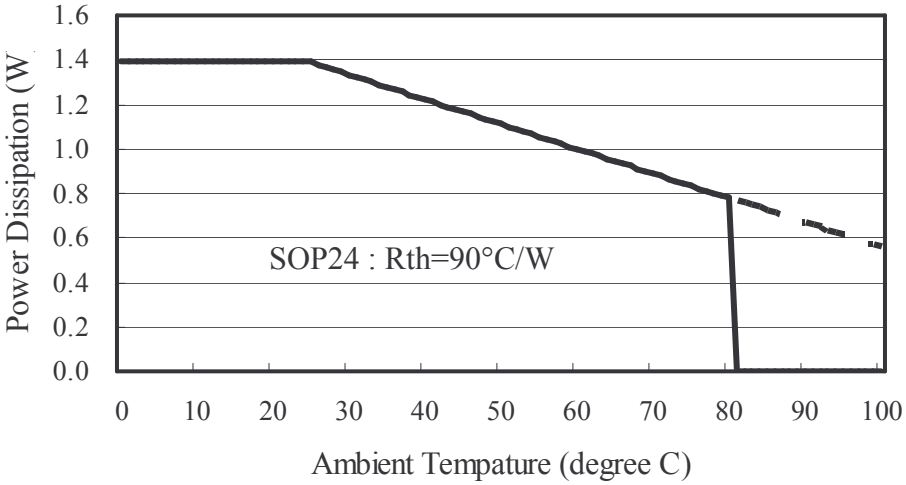
Constant Current

The current characteristic of output stage is flat. The output current can kept constant regardless of the variations of LED forward voltage when V_{OUT} > 1.0V. The relationship between I_{OUT} and V_{OUT} is shown as :



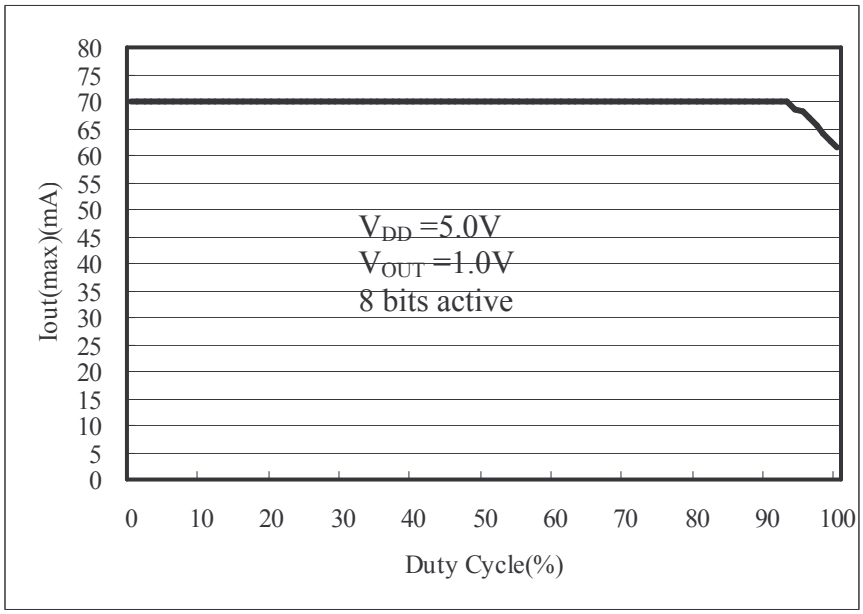
Power Dissipation

The power dissipation (P_D) of a semiconductor chip is limited by its package and ambient temperature. The maximum allowable power dissipation (P_D) is determined as P_D (max)=(Tj –Ta)/$R_{th(j-a)}$ where Tj : the chip junction temperature, Ta: ambient temperature, $R_{th(j-a)}$: thermal resistance. For SOP packages, the relationship between P_D and Ta is shown as the following figure.



Maximum Output Current

In practical case, the SCT2180 turn on the output in partial period. So the actual package power dissipation is P_D(act)=(I_{DD} • V_{DD}) + (# outputs • I_{OUT} • V_{OUT} • Duty). Therefore, to keep P_D(act) ≦ P_D(max), the allowed maximum output current be calculated from the equation: I_{OUT} = (P_D - I_{DD} • V_{DD})/(# outputs • V_{OUT} • Duty)
So the relationship between I_{OUT} (max) and Ta is shown as the following figure:



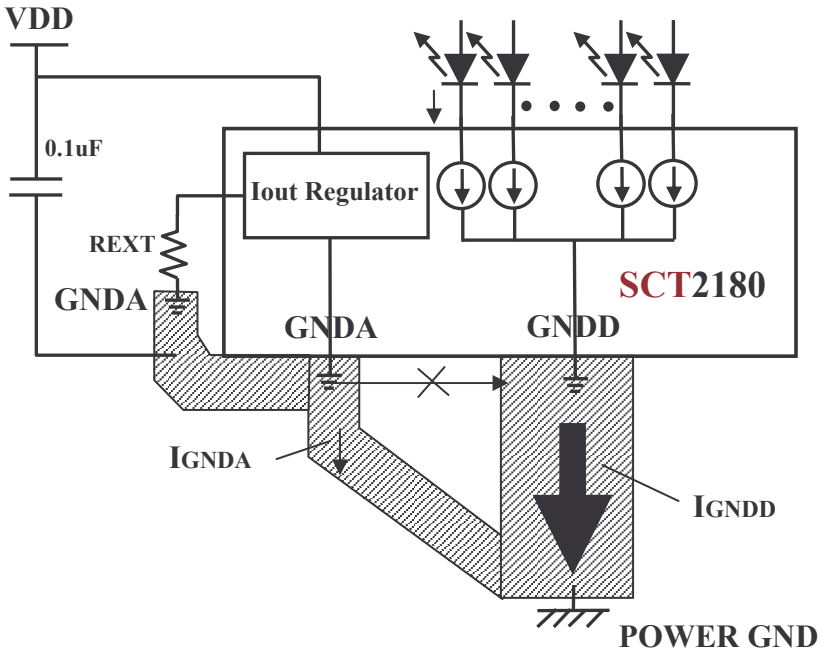
Layout Guide

For best circuit performance, use the following general guide-line when designing printed circuit boards (PCB**):**

Decoupling Capacitor
Place a 0.1uF decoupling capacitor between VDD and GND pins of SCT2180. Locate the capacitor as close to the SCT2180 as possible.

External Resistor (REXT)
Locate the external resistor as close to the REXT pin as possible to avoid the noise influence.

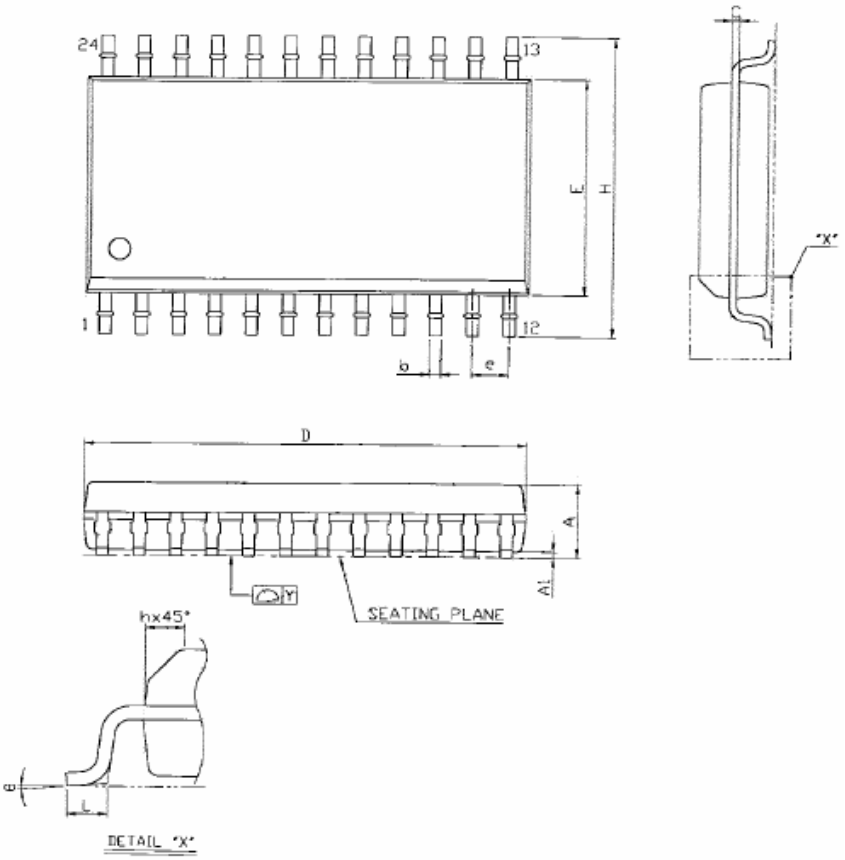
Ground
Split the ground connection. Use separate traces or planes for the analog, digital grounds (GNDA, GNDD pins of SCT2180) and tie them together at a single point, preferably close to the system power return. The GNDA pin of SCT2180 has little current flow through it and is likely to be treated as a clean ground in SCT2180. The GNDD pins have to accept all the output current and hence to be named "dirty ground".



When split the ground connections, note that GNDD traces should be made shorter and wider. Maximizing the width and minimizing the length improves efficiency and ground bouncing by reducing both ground parasitic resistance and inductance. GNDA trace can be relatively narrow in application of SCT2180.

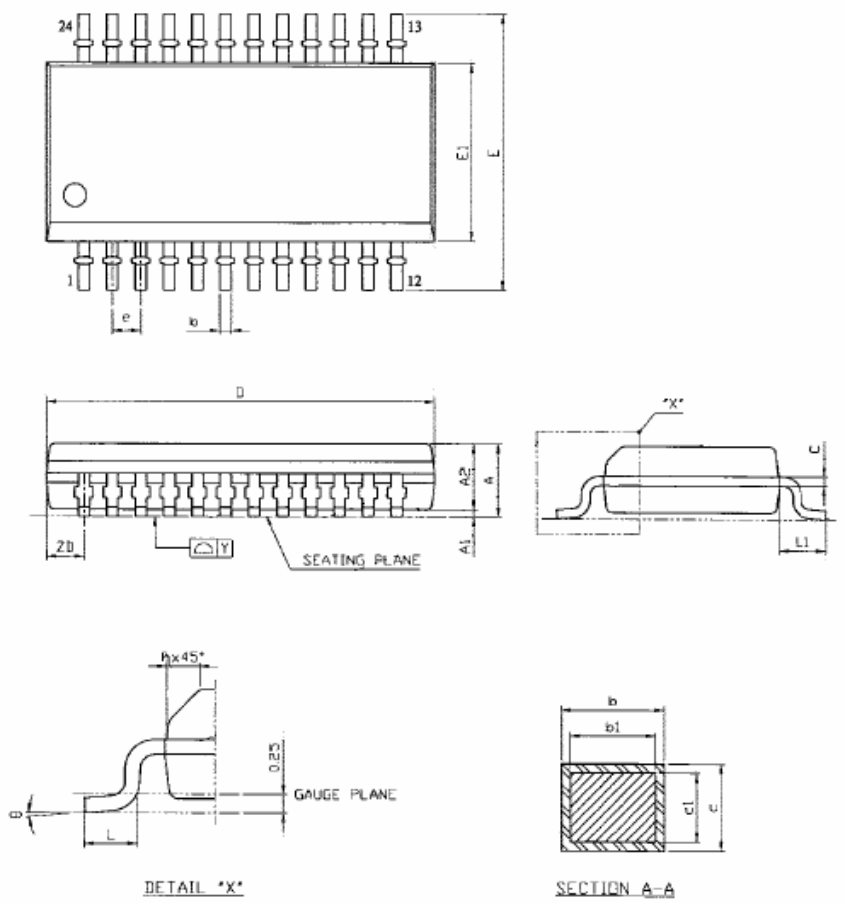
Package Dimension

SOP24



SYMBOL	DIMENSION (mm)			DIMENSION (mil)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.36	2.54	2.64	93	100	104
A1	0.10	0.20	0.30	4	8	12
b	0.35	0.406	0.48	14	16	19
c	0.23	0.254	0.31	9	10	12
D	15.20	15.29	15.60	598	602	614
E	7.40	7.50	7.60	291	295	299
e		1.27 BSC			50 BSC	
H	10.00	10.31	10.65	394	406	419
h	0.25	0.66	0.75	10	26	30
L	0.51	0.76	1.02	20	30	40
Y			0.075			3
θ	0°		8°	0°		8°

SSOP24



SYMBOL	DIMENSION (mm)			DIMENSION (mil)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	53	63	69
A1	0.10	0.15	0.25	4	6	10
A2			1.50			59
b	0.20		0.30	8		12
b1	0.20	0.254	0.28	8	10	11
c	0.18		0.25	7		10
c1	0.18	0.203	0.23	7	8	9
D	8.56	8.66	8.74	337	341	344
E	5.80	6.00	6.20	228	236	244
E1	3.80	3.90	4.00	150	154	157
e	0.635 BSC			25 BSC		
h	0.25	0.42	0.50	10	17	20
L	0.40	0.635	1.27	16	25	50
L1	1.00	1.05	1.10	39	41	43
ZD	0.838 REF			33 REF		
Y			0.10			4
θ	0°		8°	0°		8°