VIPER16

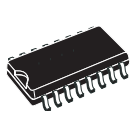
Fixed frequency VIPer™ plus family

Features

- 800 V avalanche rugged power section
- PWM operation with frequency jittering for low EMI
- Operating frequency:
  - 60 kHz for L type
  - 115 kHz for H type
- No need of auxiliary winding for low power application
- Standby power < 50 mW at 265 V_{AC}
- Limiting current with adjustable set point
- On-board soft-start
- Safe auto-restart after a fault condition
- Hysteretic thermal shutdown

Application

- Replacement of capacitive power supply
- Auxiliary power supply for appliances,
- Power metering
- LED drivers



SO16 narrow

DIP-7

Description

The device is an off-line converter with an 800 V, avalanche ruggedness power section, a PWM controller, user defined over current limit, protection against feedback network disconnection, hysteretic thermal protection, soft start up and safe auto restart after any fault condition. It is able to power itself directly from the rectified mains, eliminating the need for an auxiliary bias winding.

Advance frequency jittering reduces EMI filter cost. Burst mode operation and device very low consumption helps to meet the stand by energy saving regulation.

Figure 1. Typical buck converter application

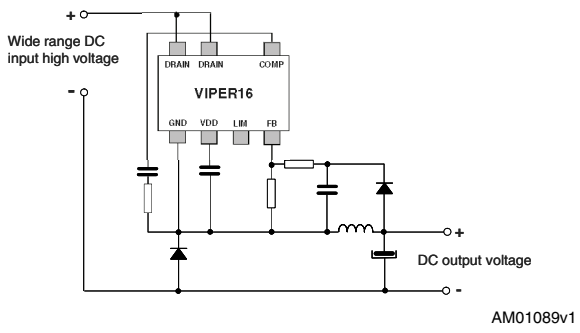


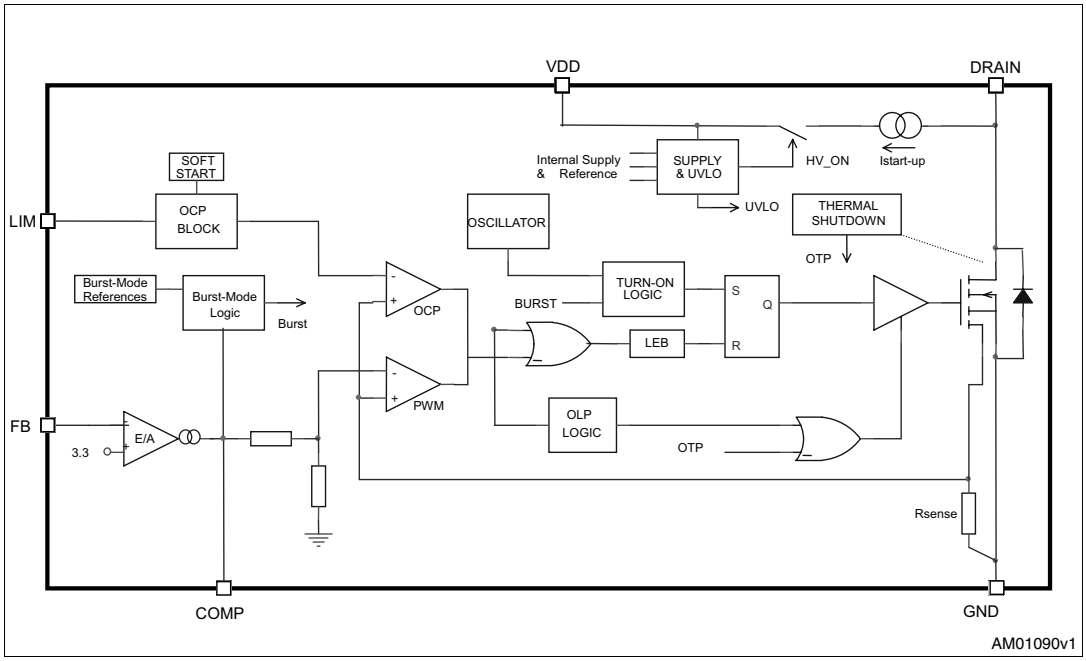
Table 1. Device summary

Order codes	Package	Packaging
VIPER16LN	DIP-7	Tube
VIPER16HN		
VIPER16HD	SO16 narrow	Tube
VIPER16HDTR		Tape and reel
VIPER16LD		Tube
VIPER16LDTR		Tape and reel

Contents

1 Block diagram

Figure 2. Block diagram



2 Typical power

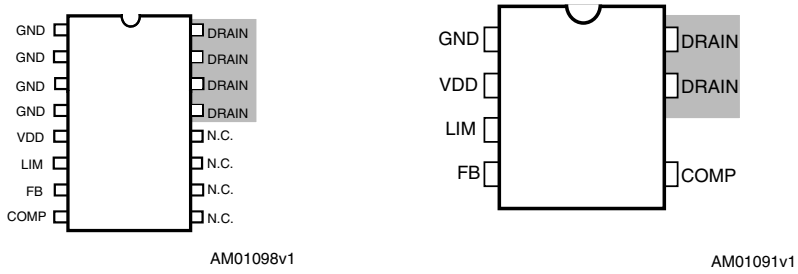
Table 2. Typical power

Part number	230 V_{AC}		85-265 V_{AC}	
	Adapter(1)	Open frame(2)	Adapter(1)	Open frame(2)
VIPER16	9 W	12 W	5 W	7 W

1. Typical continuous power in non ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat sinking.

3 Pin settings

Figure 3. Connection diagram (top view)



Note: The copper area for heat dissipation has to be designed under the DRAIN pins.

Table 3. Pin description

Pin N.		Name	Function
DIP-7	SO16		
1	1-4	GND	Connected to the source of the internal power MOSFET and controller ground reference.
2	5	VDD	Supply voltage of the control section. This pin provides the charging current of the external capacitor.
3	6	LIM	This pin allows setting the drain current limitation. The limit can be reduced by connecting an external resistor between this pin and GND. Pin left open if default drain current limitation is used.
4	7	FB	Inverting input of the internal trans conductance error amplifier. Connecting the converter output to this pin through a single resistor results in an output voltage equal to the error amplifier reference voltage (3.3 V typ. see V_{FB_REF} on *Table 7*). An external resistors divider is required for higher output voltages.
5	8	COMP	Output of the internal trans conductance error amplifier. The compensation network have to be placed between this pin and GND to achieve stability and good dynamic performance of the voltage control loop. The pin is used also to directly control the PWM with an optocoupler. The linear voltage range extends from V_{COMPL} to V_{COMPH} (*Table 7*).
7,8	13-16	DRAIN	High voltage drain pin. The built-in high voltage switched start-up bias current is drawn from this pin too. Pins connected to the metal frame to facilitate heat dissipation.

4 Electrical data

4.1 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Pin (DIP-7)	Parameter	Value		Unit
			Min	Max	
V_{DRAIN}	7, 8	Drain-to-source (ground) voltage		800	V
E_{AV}	7, 8	Repetitive avalanche energy (limited by T_J = 150 °C)		2	mJ
I_{AR}	7, 8	Repetitive avalanche current (limited by T_J = 150 °C)		1	A
I_{DRAIN}	7, 8	Pulse drain current		2.5	A
V_{COMP}	5	Input pin voltage	-0.3	3.5	V
V_{FB}	4	Input pin voltage	-0.3	4.8	V
V_{LIM}	3	Input pin voltage	-0.3	2.4	V
V_{DD}	2	Supply voltage	-0.3	Self limited	V
I_{DD}	2	Input current		20	mA
P_{TOT}		Power dissipation at T_A < 40 °C (DIP-7)		1	W
		Power dissipation at T_A < 60 °C (SO16N)		1	W
T_J		Operating junction temperature range	-40	150	°C
T_{STG}		Storage temperature	-55	150	°C

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max value SO16N	Max value DIP-7	Unit
R_{thJP}	Thermal resistance junction pin (Dissipated power = 1 W)	35	40	°C/W
R_{thJA}	Thermal resistance junction ambient (Dissipated power = 1 W)	90	110	°C/W
R_{thJA}	Thermal resistance junction ambient (1) (Dissipated power = 1 W)	80	90	°C/W

1. When mounted on a standard single side FR4 board with 100 mm^2 (0.155 sq in) of Cu (35 µm thick)

4.3 Electrical characteristics

(T_J = -25 to 125 °C, V_{DD} = 14 V; unless otherwise specified)

Table 6. Power section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{BVDSS}	Break-down voltage	I_{DRAIN} = 1 mA, V_{COMP} = GND, T_J = 25 °C	800			V
I_{OFF}	OFF state drain current	V_{DRAIN} = max rating, V_{COMP} = GND			60	µA
$R_{DS(on)}$	Drain-source on state resistance	I_{DRAIN} = 0.2 A, T_J = 25 °C		20	24	Ω
		I_{DRAIN} = 0.2 A, T_J = 125 °C		40	48	Ω
C_{OSS}	Effective (energy related) output capacitance	V_{DRAIN} = 0 to 640 V		10		pF

Table 7. Supply section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Voltage						
V_{DRAIN_START}	Drain-source start voltage		40	50	60	V
I_{DDch1}	Start up charging current	V_{DRAIN} = 100 V to 640 V, V_{DD} = 4 V	-0.6		-1.8	mA
I_{DDch2}	Charging current during operation	V_{DRAIN} = 100 V to 640 V, V_{DD} = 9 V falling edge	-7		-13	mA
V_{DD}	Operating voltage range		11.5		23.5	V
$V_{DDclamp}$	V_{DD} clamp voltage	I_{DD} = 15 mA	23.5			V
V_{DDon}	V_{DD} start up threshold		12	13	14	V
V_{DDCSon}	VDD on internal high voltage current generator threshold		9.5	10.5	11.5	V
V_{DDoff}	V_{DD} under voltage shutdown threshold				7	V
Current						
I_{DD0}	Operating supply current, not switching	F_{OSC} = 0 kHz, V_{COMP} = GND			0.6	mA
I_{DD1}	Operating supply current, switching	V_{DRAIN} = 120 V, F_{SW} = 60 kHz			1.3	mA
		V_{DRAIN} = 120 V, F_{SW} = 115 kHz			1.5	mA
I_{DDoff}	Operating supply current with $V_{DD} < V_{DDoff}$	$V_{DD} < V_{DDoff}$			0.35	mA
I_{DDol}	Open loop failure current threshold	$V_{DD} = V_{DDclamp}$ V_{COMP} = 3.3 V,	4			mA

Table 7. Controller section
(T_J = -25 to 125 °C, V_{DD} = 14 V; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Error amplifier						
V_{REF_FB}	FB reference voltage		3.2	3.3	3.4	V
$I_{FB\_PULL\ UP}$	Current pull up			-1		µA
G_M	Trans conductance			2		mA/V
Current setting (LIM) pin						
V_{LIM_LOW}	Low level clamp voltage	I_{LIM} = -100 µA		0.5		V
Compensation (COMP) pin						
V_{COMPH}	Upper saturation limit	T_J = 25 °C		3		V
V_{COMPL}	Burst mode threshold	T_J = 25 °C	1	1.1	1.2	V
V_{COMPL_HYS}	Burst mode hysteresis	T_J = 25 °C		40		mV
H_{COMP}	ΔV_{COMP} / ΔI_{DRAIN}		4		9	V/A
$R_{COMP(DYN)}$	Dynamic resistance	V_{FB} = GND		15		kΩ
I_{COMP}	Source / sink current	V_{FB} > 100 mV		150		µA
	Max source current	V_{COMP} = GND, V_{FB} = GND		220		µA
Current limitation						
I_{Dlim}	Drain current limitation	I_{LIM} = -10 µA V_{COMP} = 3.3 V T_J = 25 °C	0.38	0.4	0.42	A
t_{SS}	Soft-start time			8.5		ms
T_{ON_MIN}	Minimum turn ON time				450	ns
I_{Dlim_bm}	Burst mode current limitation	V_{COMP} = V_{COMPL}		85		mA
Overload						
t_{OVL}	Overload time			50		ms
$t_{RESTART}$	Restart time after fault			1		s
Oscillator section						
F_{OSC}	Switching frequency VIPer16LN		54	60	66	kHz
	Switching frequency VIPer16HN		103	115	127	kHz
F_D	Modulation depth	F_{OSC} = 60 kHz		±4		kHz
		F_{OSC} = 115 kHz		±8		kHz
F_M	Modulation frequency			230		Hz

Table 7. Controller section (continued)
(T_J = -25 to 125 °C, V_{DD} = 14 V; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
D_{MAX}	Maximum duty cycle		70		80	%
Thermal shutdown						
T_{SD}	Thermal shutdown temperature		150	160		°C
T_{HYST}	Thermal shutdown hysteresis			30		°C

5 Typical electrical characteristics

Figure 4. IDlim vs T_J

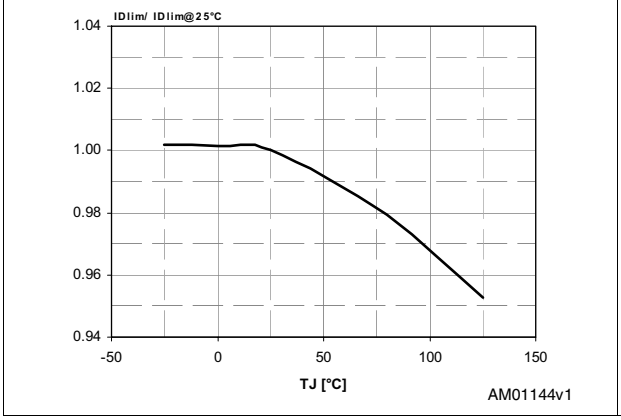


Figure 5. F_{OSC} vs T_J

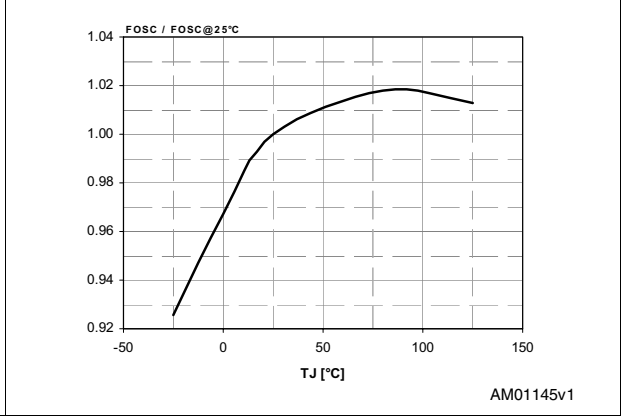


Figure 6. V_{DRAIN_START} vs T_J

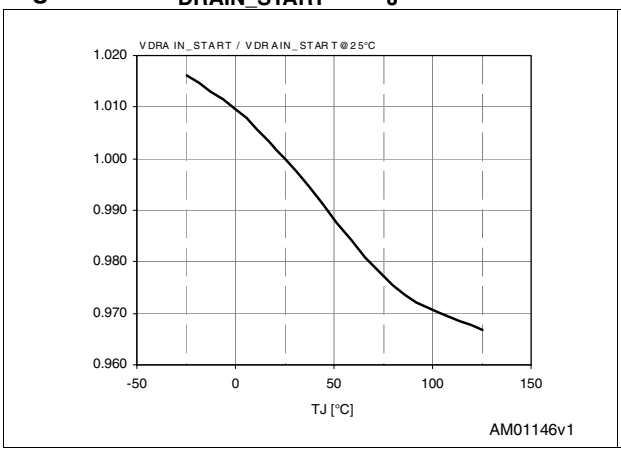


Figure 7. H_{COMP} vs T_J

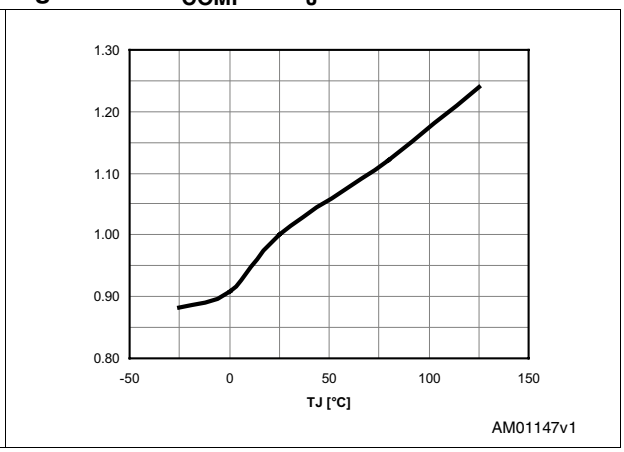


Figure 8. G_M vs T_J

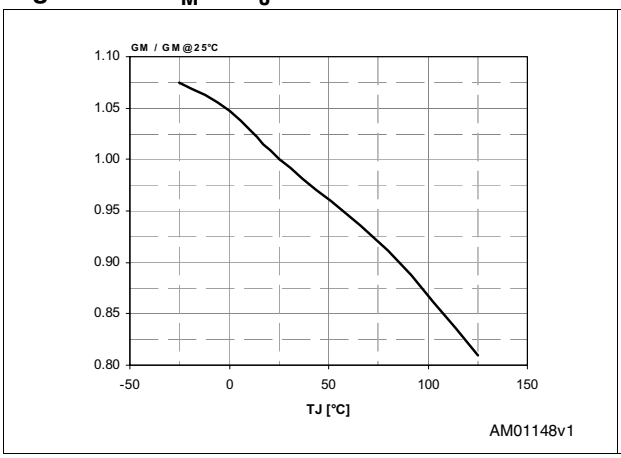


Figure 9. V_{REF_FB} vs T_J

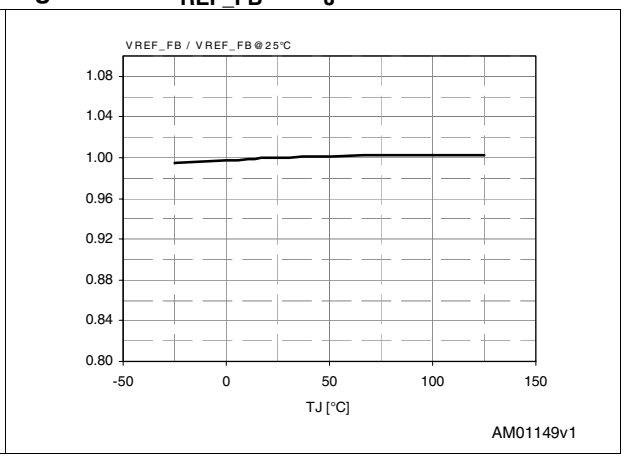


Figure 10. I_{COMP} vs T_J

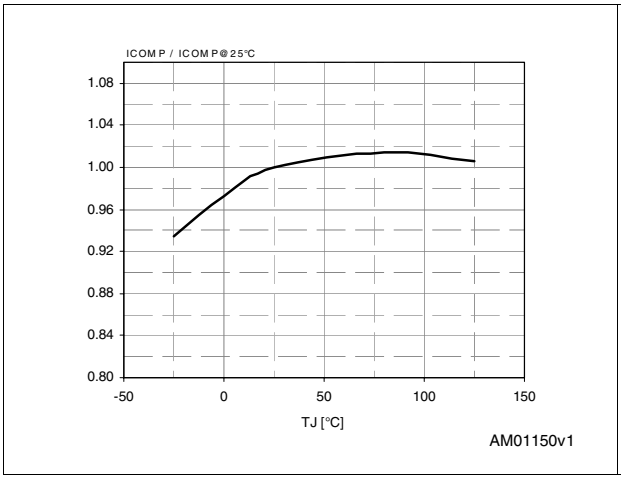


Figure 11. Operating supply current (no switching) vs T_J

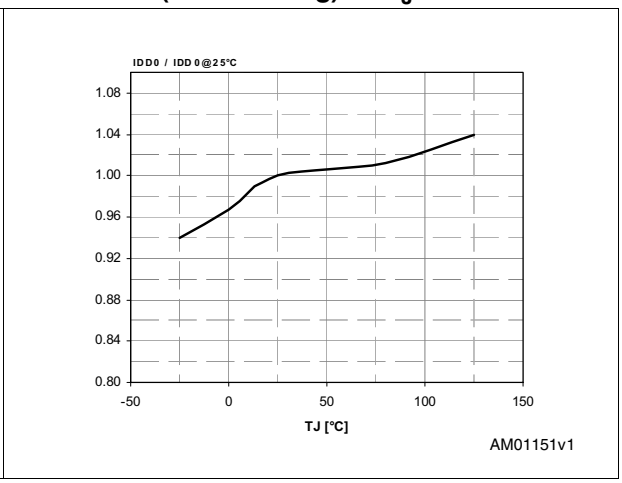


Figure 12. Operating supply current (switching) vs T_J

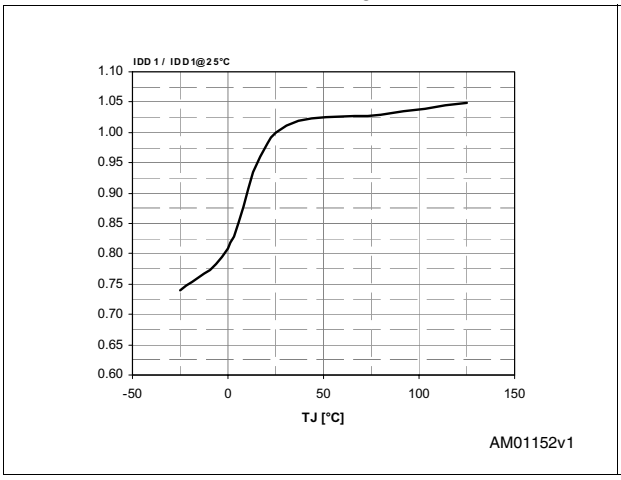


Figure 13. IDlim vs R_{LIM}

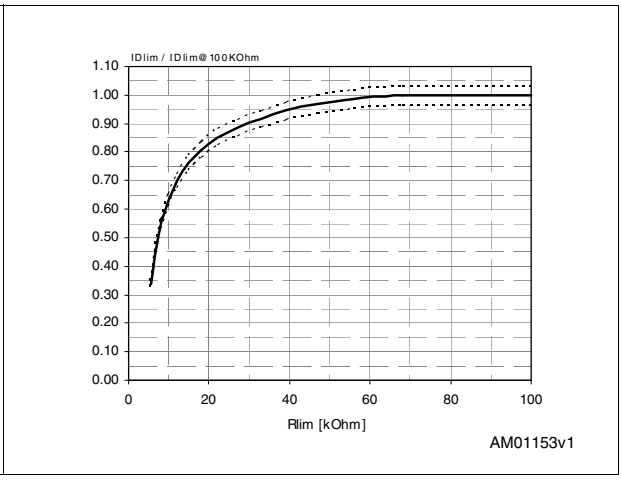


Figure 14. Power MOSFET on-resistance vs T_J

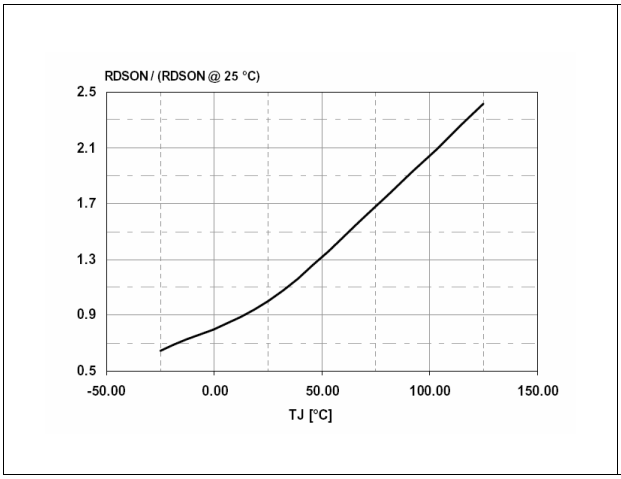


Figure 15. Power MOSFET break down voltage vs T_J

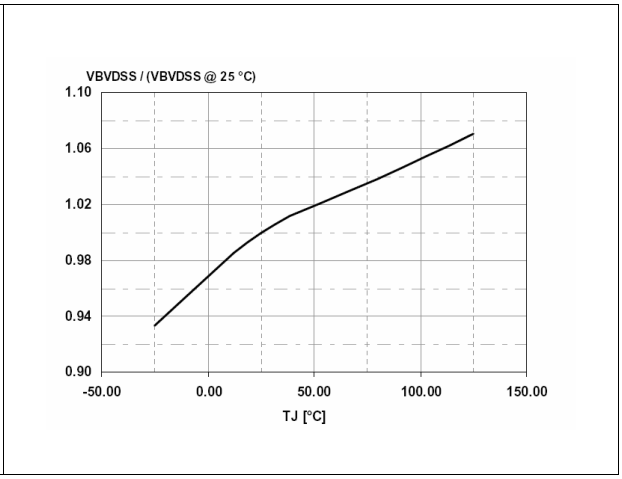
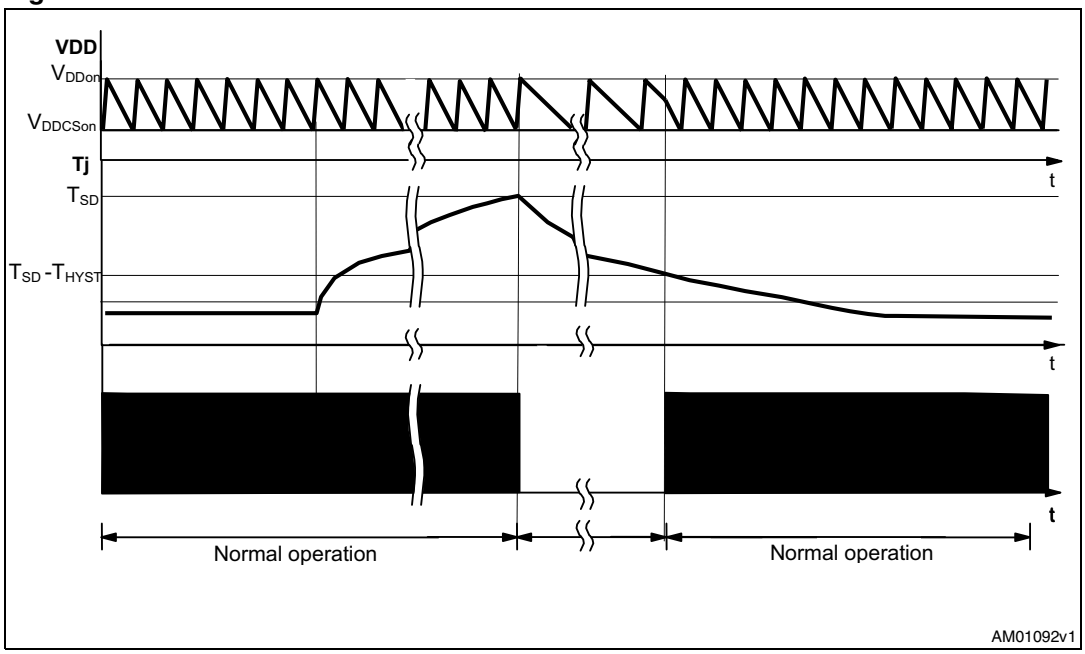


Figure 16. Thermal shutdown



6 Typical circuit

Figure 17. Buck converter

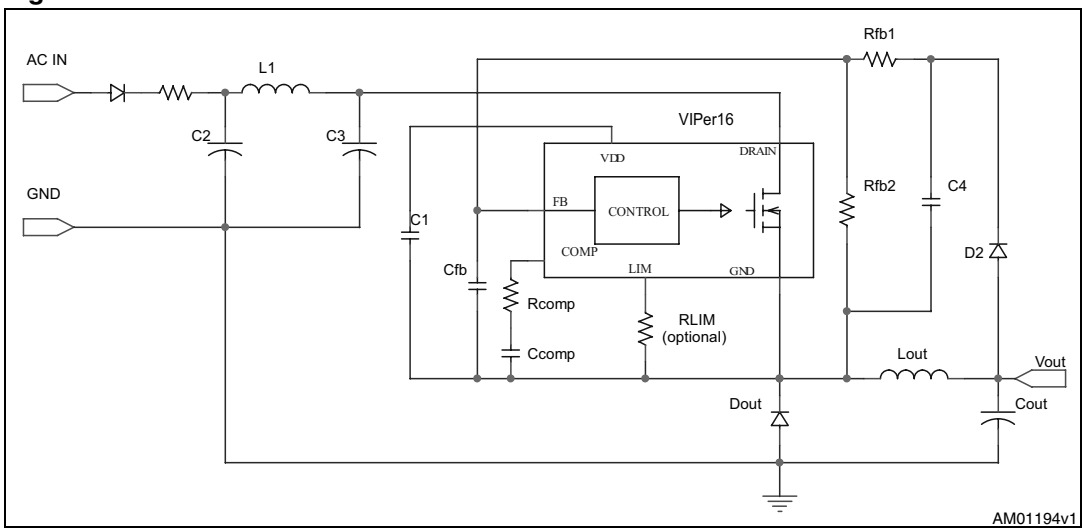


Figure 18. Buck boost converter

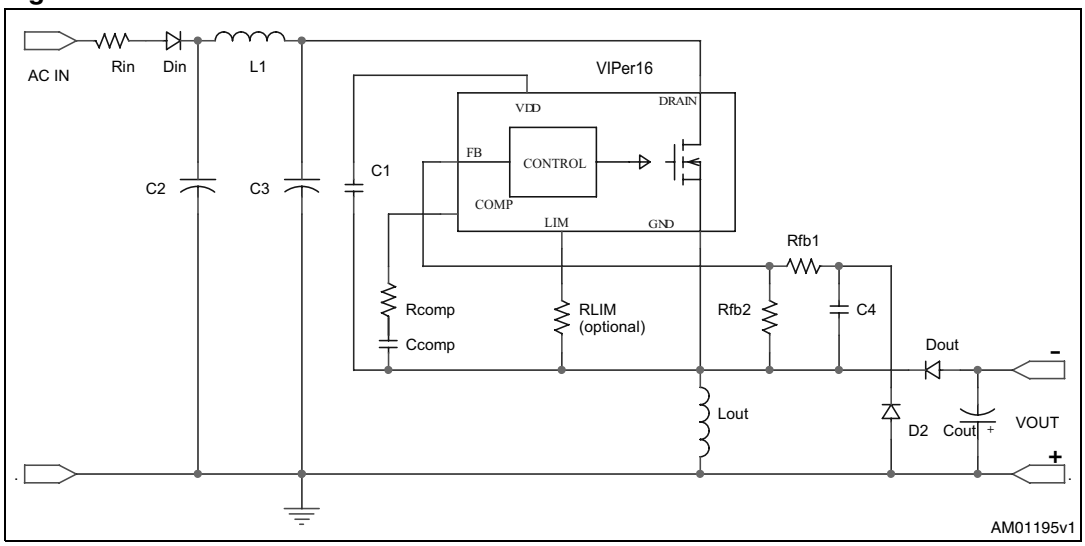


Figure 19. Flyback converter (primary regulation)

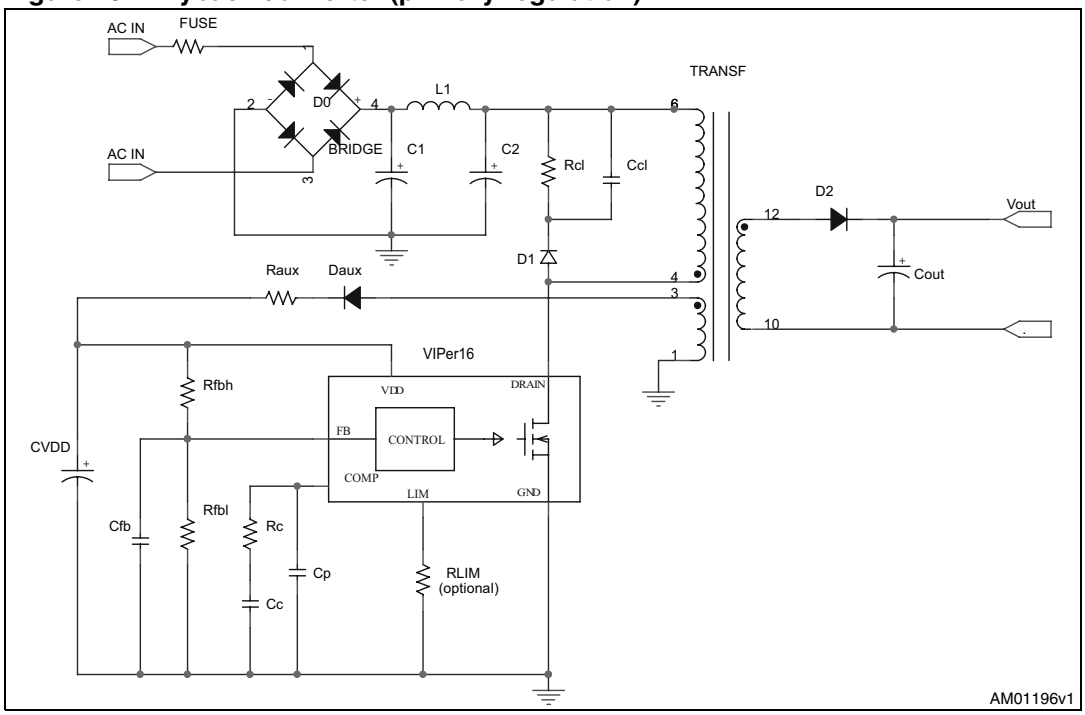
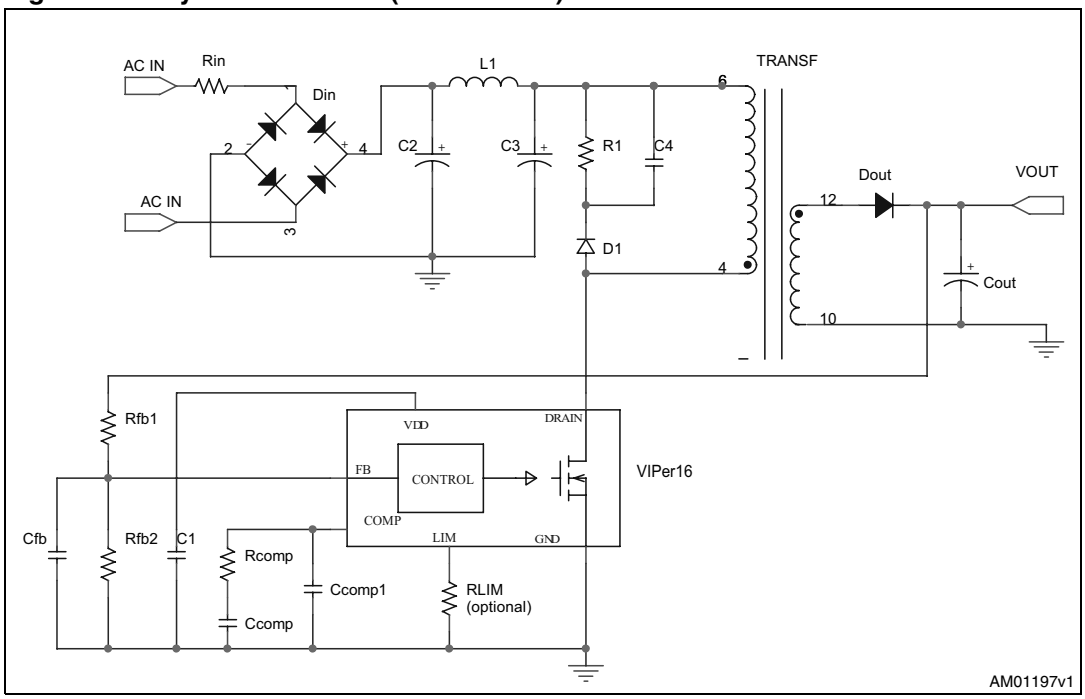


Figure 20. Flyback converter (non isolated)



7 Power section

The power section is implemented with an n-channel power MOSFET with a breakdown voltage of 800 V min. and a typical $R_{DS(on)}$ of 20 Ω. It includes a SenseFET structure to allow a virtually lossless current sensing and the thermal sensor.

The gate driver of the power MOSFET is designed to supply a controlled gate current during both turn-ON and turn-OFF in order to minimize common mode EMI. During UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the power MOSFET cannot be turned ON accidentally.

8 High voltage current generator

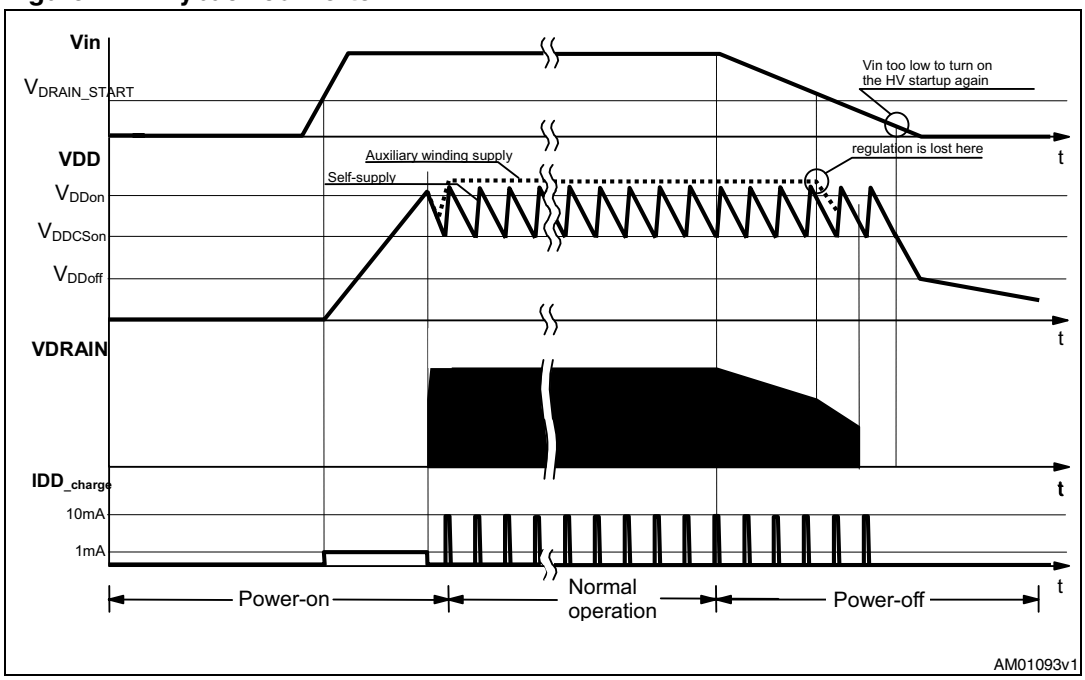
The high voltage current generator is supplied by the DRAIN pin. At the first start up of the converter, it is enabled when the voltage across the input bulk capacitor reaches the V_{DRAIN_START} threshold (50 V_{DC} typically), sourcing a 1 mA current (typical value); as the V_{DD} voltage reaches the V_{DDon} start-up threshold, the power section starts switching and the high voltage current generator is turned OFF. The VIPer16 is powered by the energy stored in the V_{DD} capacitor.

In steady state condition, if the self biasing function is used, the high voltage current generator is activated between V_{DDCSon} and V_{DDon} (see *Table 7*), delivering 10 mA to the V_{DD} capacitor during the MOSFET off time (see *Figure 21*).

The device can also be supplied through the auxiliary winding; in this case the high voltage current source is disabled during steady-state operation, provided that VDD is above V_{DDon}.

At converter power-down, the V_{DD} voltage drops and the converter activity stops as it falls below V_{DDoff} threshold (see *Table 7*).

Figure 21. Flyback converter



9 Oscillator

The switching frequency is internally fixed at 60 kHz (part number VIPER16LN) or 115 kHz (part number VIPER16HN).

In both cases the switching frequency is modulated by approximately ±4 kHz (60 kHz version) or ±8 kHz (115 kHz version) at 230 Hz (typical) rate, so that the resulting spread-spectrum action distributes the energy of each harmonic of the switching frequency over a number of sideband harmonics having the same energy on the whole but smaller amplitudes.

10 Soft start-up

During the converter start-up phase, the internal soft-start function progressively increases the cycle-by-cycle current limitation up to the I_{Dlim} value. In this way the drain current is further limited and the output voltage is progressively increased reducing the stress on the secondary diode. In combination with the control of the max duty cycle, this function helps to prevent transformer saturation during the start-up.

The soft-start time is internally fixed to 8.5 ms (see t_{SS} on *Table 7*)and the function is activated for any attempt of converter start-up and after a fault event.

11 Adjustable current limit set point

The device is a current mode PWM: cycle-by-cycle the drain current is sensed and converted in a voltage that is applied to the non inverting pin of the PWM comparator and compared with the one present on the COMP pin (see *Figure 2*). When the two voltages values are equal, the power section is switched off.

Connecting a resistor R_{LIM} between LIM and GND pins fixes the current sunk from the LIM pin and allows the designer to set the drain current limitation: it will be fixed to its default value, I_{DLIM} on *Table 7*, if the LIM pin is left open or if the R_{LIM} value is high enough (> 80 kΩ); it will be decreased, as reported in *Figure 13 on page 10*, if lower values of R_{LIM} are chosen.

12 FB pin and COMP pin

The device can be used both in non-isolated and in isolated topologies. In case of non-isolated topology, the feedback signal from the output voltage is applied to the FB pin and is compared with the error amplifier internal reference, V_{REF_FB} (see *Table 7*). The error amplifier output sources and sinks the I_{COMP} current respectively to and from the compensation network connected on the COMP pin. The value of this voltage is then internally compared with the one coming from the SenseFET and the power section is switched off when the two values are equal on cycle by cycle basis.

As the regulation point on FB pin is 3.3 V, see V_{REF_FB} on *Table 7*, a single resistor has to be connected to this pin if the output voltage is 3.3 V. While for higher output voltages an external resistor divider is needed. The FB pin is also provided with an internal pull up, in order to protect the IC when it is accidentally left floating.

The COMP pin, which is the output of the error amplifier, is used for the loop compensation: usually, an RC network, which stabilizes the overall control loop, is connected between this pin and GND.

In isolated topology, the FB pin is connected to GND, disabling the error amplifier. In this case a 15 kΩ internal resistor is connected between an internal 3.3 V generator and the COMP pin, which is also connected to an opto-transistor in parallel with the compensation network (see *Figure 21*).

The COMP pin voltage dynamics ranges is between V_{COMPL} and V_{COMPH} as reported in *Figure 23* and *Table 7*.

At very low load or no load condition, when the voltage across the COMP pin drops below the voltage level V_{COMPL} - $V_{COMPL\ HYS}$, (where $V_{COMPL\ HYS}$ is 50 mV typical), the converter enters burst mode (see *Section 13 on page 17*). When the COMP voltage rises above the V_{COMPH} threshold, the peak drain current will reach its limit, as well as the deliverable output power.

Figure 22. Feedback circuit

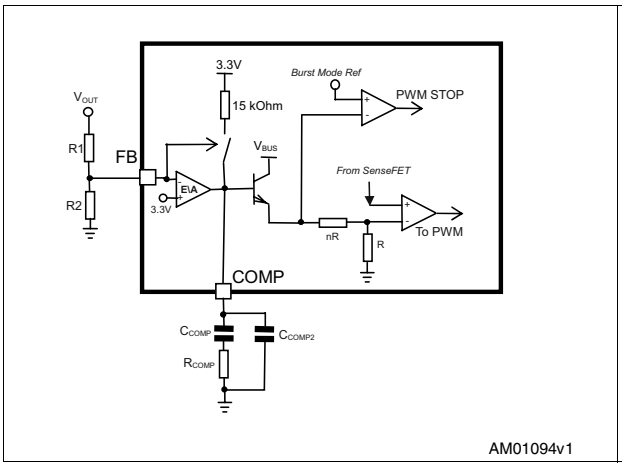
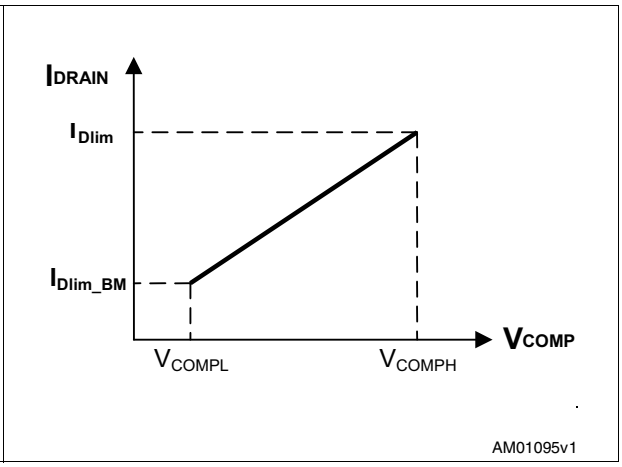


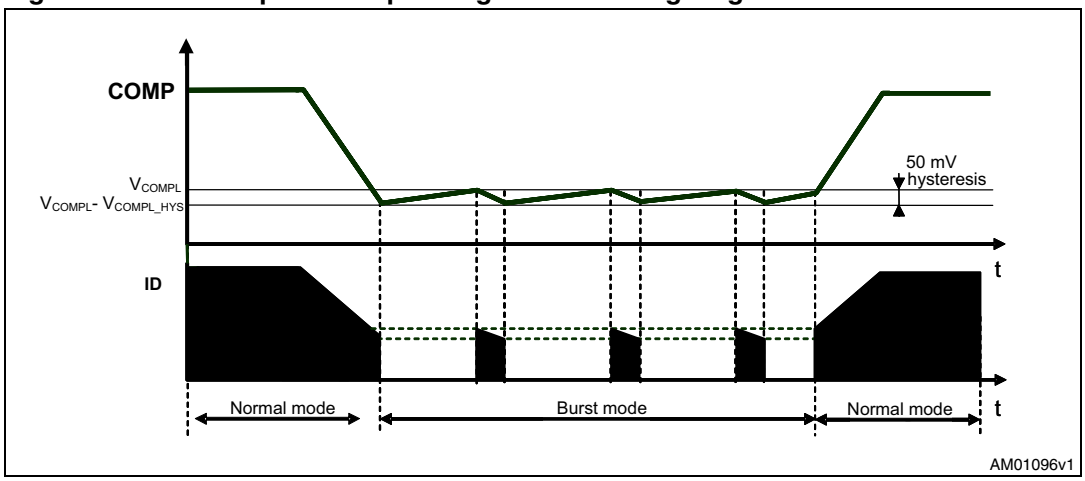
Figure 23. COMP pin voltage versus I_{DLIM}



13 Burst mode

When the voltage at the COMP pin is 50 mV below an internally fixed threshold, V_{COMPL}, the power MOSFET is kept in OFF state and the consumption reduced at the lowest value. At this point, the voltage on the COMP pin increases as a result of the feedback reaction to the energy delivery stop. When the V_{COMPL} threshold is exceeded, the converter will start switching again. This controlled on-off operation, referred to as “burst mode”, causes an average frequency reduction, which can go down even to a few hundreds hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. This mode of operation, shown in the timing diagram of *Figure 24*, is noise-free since the peak current is very low.

Figure 24. Load-dependent operating modes: timing diagrams



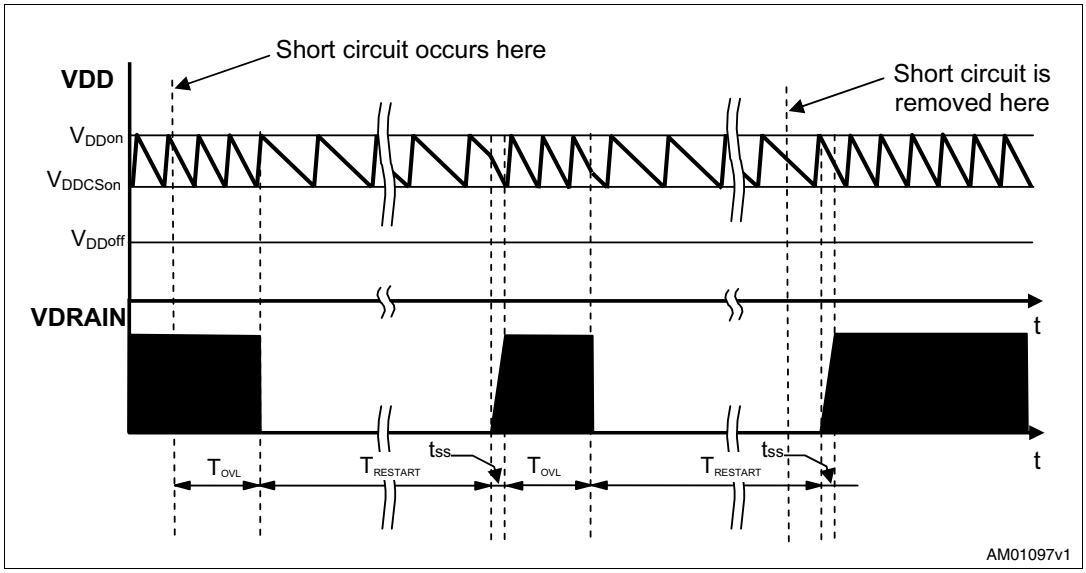
14 Autorestart after fault

In case of over load or short circuit, a counter increments every cycle the current-step logic detects a current limit condition; i.e. when the drain current reaches the I_{DLIM} value (or the one set by the user through the R_{lim} resistor). If this condition is maintained continuously for a fixed-time, t_{OVL}, the overload protection is tripped, the power section is turned off and the converter is disabled for a $t_{RESTART}$ time, whose typical value is 1 s (see *Table 7*). After the start-up sequence, the protection will occur in the same way until the overload condition is removed.

This protection ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low power throughput and avoiding the IC overheating in case of repeated overload events.

If the overload is removed before the protection tripping, the counter will be decremented cycle-by-cycle down to zero.

Figure 25. Timing diagram: OLP sequence



15 Open loop failure protection

When the VIPER16 is supplied by an auxiliary winding, the converter is protected against feedback loop failure or accidentally disconnections.

With reference to *Figure 22*, if resistance R_1 is opened, the VIPER16 works at its drain current limitation.

The output voltage will increase and so the auxiliary voltage, which is coupled with the output through the secondary/auxiliary turns ratio.

As the auxiliary voltage increases up to the internal V_{DD} active clamp, $V_{DDclamp}$ (see *Table 7*) and the clamp current injected on VDD pin exceeds the latch threshold, I_{DDol} (see *Table 7*), a fault signal is internally generated.

Both the conditions: drain current equal to the drain current limitation and I_{DDol} through V_{DD} clamp, have to be verified to let the fault be revealed. This helps to distinguish an actual malfunction from a bad auxiliary winding design.

With reference to *Figure 22*, if the resistor R_2 is opened, the FB pin is pulled up via R_1, and the output voltage is clamped to V_{REF_FB} (3.3 V, typ).

In case of accidental disconnection of the track on FB, the voltage on this pin goes up due to an internal pull-up, thus avoiding the power section switching.

In case of isolated flyback topology with auxiliary winding, the open loop failure protection will be triggered in the same way as described before, when the upper resistor of the output voltage divider, R_{UP}, is opened or the lower resistor, R_{DOWN} is shorted. If, on the contrary, R_{UP} is shorted or R_{DOWN} is opened, the output voltage will be limited to the voltage reference.

16 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 8. DIP-7 mechanical data

Dim.	mm		
	Typ	Min	Max
A			5,33
A1		0,38	
A2	3,30	2,92	4,95
b	0,46	0,36	0,56
b2	1,52	1,14	1,78
c	0,25	0,20	0,36
D	9,27	9,02	10,16
E	7,87	7,62	8,26
E1	6,35	6,10	7,11
e	2,54		
eA	7,62		
eB			10,92
L	3,30	2,92	3,81
M (6)(8)	2,508		
N	0,50	0,40	0,60
N1			0,60
O (7)(8)	0,548		

1- The leads size is comprehensive of the thickness of the leads finishing material.

2- Dimensions do not include mold protrusion, not to exceed 0,25 mm in total (both side).

3- Package outline exclusive of metal burrs dimensions.

4- Datum plane “H” coincident with the bottom of lead, where lead exits body.

5- Ref. POA MOTHER doc. 0037880

6- Creepage distance > 800 V

7- Creepage distance 250 V

8- Creepage distance as shown in the 664-1 CEI / IEC standard.

Figure 26. Package dimensions

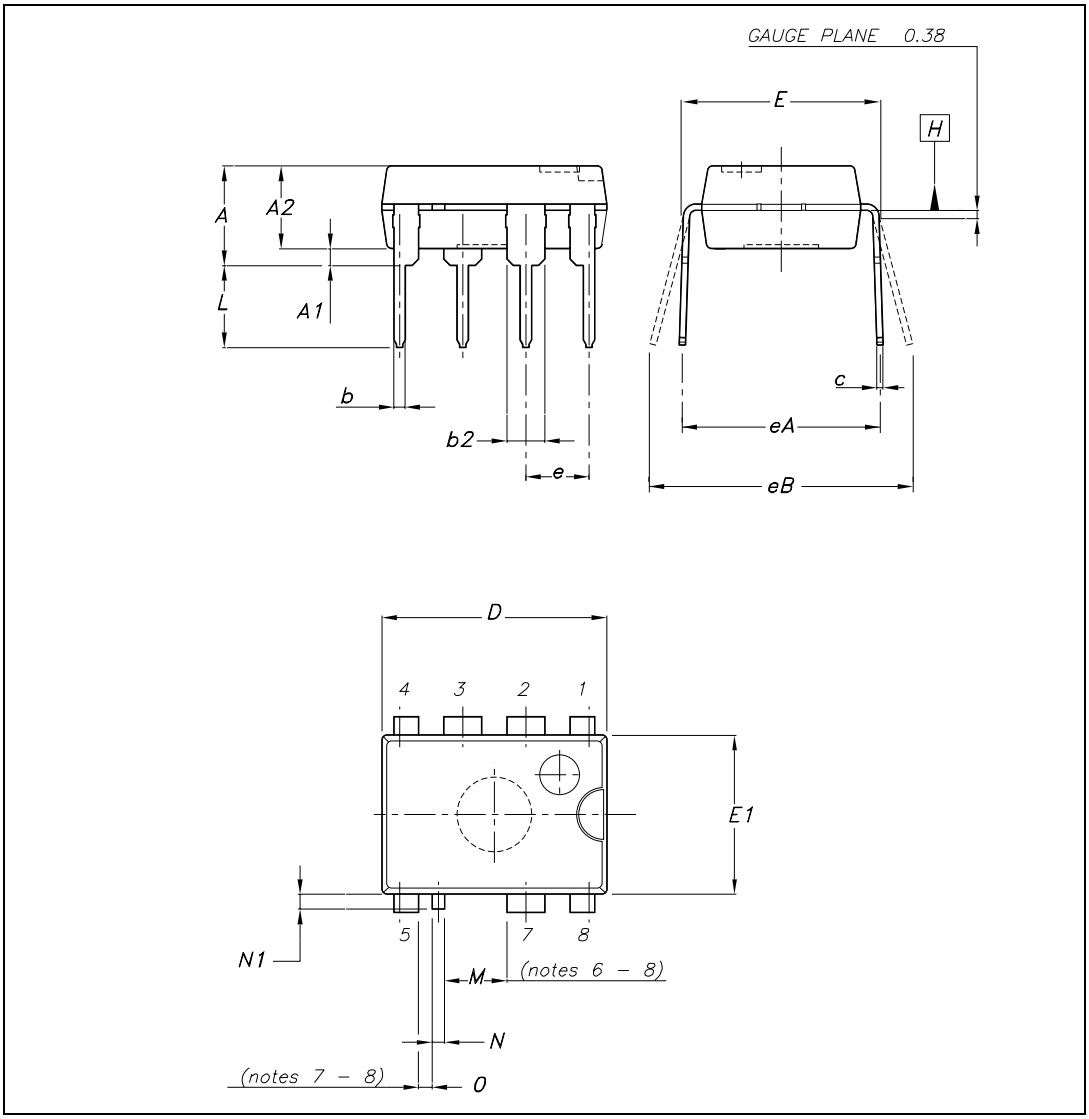
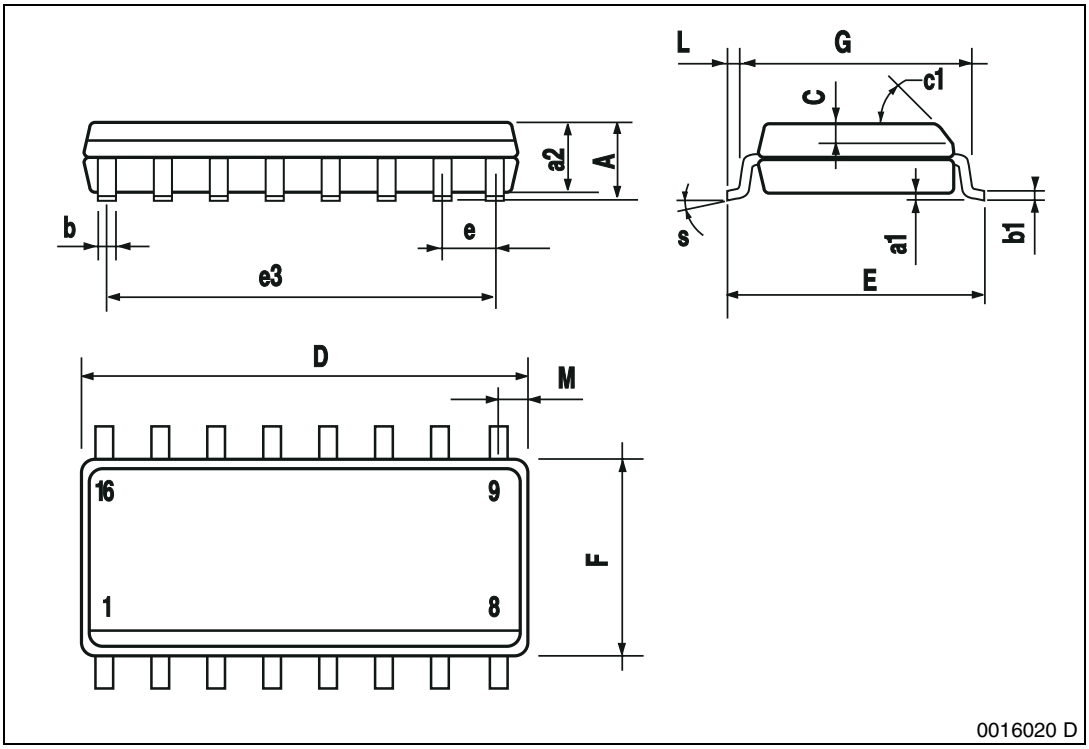


Table 9. SO16 narrow mechanical data

Dim.	mm		
	Min	Typ	Max
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

Figure 27. Package dimensions



17 Revision history

Table 10. Document revision history

Date	Revision	Changes
21-Jan-2009	1	Initial release
07-Dec-2009	2	Updated *Figure 7 on page 9*

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