

December 2007

74VHC02 Quad 2-Input NOR Gate

Features

- High Speed: t_{PD} = 3.6ns (Typ.) at V_{CC} = 5V
- Low power dissipation: $I_{CC} = 2\mu A$ (Max.) at $T_A = 25$ °C
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- Power down protection is provided on all inputs
- Low noise: $V_{OLP} = 0.8V$ (Max.)
- Pin and function compatible with 74HC02

General Description

The VHC02 is an advanced high-speed CMOS 2-Input NOR Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages, including buffer output, which provide high noise immunity and stable output. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Ordering Information

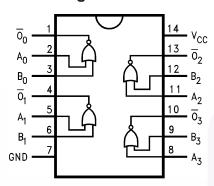
Order Number	Package Number	Package Description
74VHC02M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC02SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC02MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

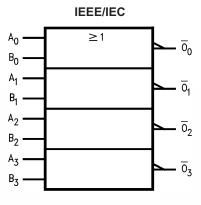
Connection Diagram



Pin Description

Pin Names	Description
A _n , B _n	Inputs
\overline{O}_n	Outputs

Logic Symbol



Truth Table

Α	В	ō
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	-0.5V to +7.0V
V _{IN}	DC Input Voltage	-0.5V to +7.0V
V _{OUT}	DC Output Voltage	-0.5V to V _{CC} + 0.5V
I _{IK}	Input Diode Current	–20mA
I _{OK}	Output Diode Current	±20mA
I _{OUT}	DC Output Current	±25mA
I _{CC}	DC V _{CC} / GND Current	±50mA
T _{STG}	Storage Temperature	−65°C to +150°C
T _L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions⁽¹⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	2.0V to +5.5V
V _{IN}	Input Voltage	0V to +5.5V
V _{OUT}	Output Voltage	0V to V _{CC}
T _{OPR}	Operating Temperature	-40°C to +85°C
t _r , t _f	Input Rise and Fall Time,	
	$V_{CC} = 3.3V \pm 0.3V$	0ns/V ~ 100ns/V
	$V_{CC} = 5.0V \pm 0.5V$	0ns/V ~ 20ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

					Т	- A = 25°	С		40°C to 5°C	
Symbol	Parameter	V _{CC} (V)	Con	Conditions		Тур.	Max.	Min.	Max.	Units
V _{IH}	HIGH Level Input	2.0			1.50			1.50		V
	Voltage	3.0-5.5			0.7 x V _{CC}			0.7 x V _{CC}		
V _{IL}	LOW Level Input	2.0					0.50		0.50	V
	Voltage	3.0-5.5					0.3 x V _{CC}		0.3 x V _{CC}	
V _{OH}	HIGH Level	2.0	$V_{IN} = V_{IH}$	$I_{OH} = -50\mu A$	1.9	2.0		1.9		V
	Output Voltage	3.0	or V _{IL}		2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		$I_{OH} = -4mA$	2.58			2.48		
		4.5		$I_{OH} = -8mA$	3.94			3.80		
V _{OL}	LOW Level	2.0	$V_{IN} = V_{IH}$	$I_{OL} = 50\mu A$		0.0	0.1		0.1	V
	Output Voltage	3.0	or V _{IL}			0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		I _{OL} = 4mA			0.36		0.44	
		4.5		$I_{OL} = 8mA$			0.36		0.44	
I _{IN}	Input Leakage Current	0–5.5	V _{IN} = 5.5V or GND				±0.1		±1.0	μA
Icc	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$	V _{IN} = V _{CC} or GND			2.0		20.0	μA

Noise Characteristics

				T _A =	25°C	
Symbol	Parameter	V _{CC} (V)	Conditions	Тур.	Limits	Units
V _{OLP} ⁽²⁾ Quiet Output Maximum Dynamic V _{OL}		5.0	C _L = 50pF	0.3	0.8	V
V _{OLV} ⁽²⁾	V _{OLV} ⁽²⁾ Quiet Output Minimum Dynamic V _{OL}		C _L = 50pF	-0.3	-0.8	V
V _{IHD} ⁽²⁾	V _{IHD} ⁽²⁾ Minimum HIGH Level Dynamic Input Voltage		C _L = 50pF		3.5	V
V _{ILD} ⁽²⁾			C _L = 50pF		1.5	V

Note:

2. Parameter guaranteed by design.

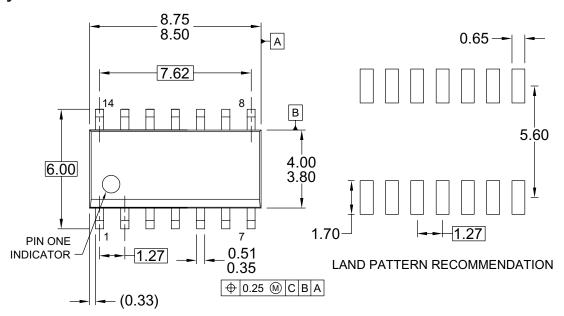
AC Electrical Characteristics

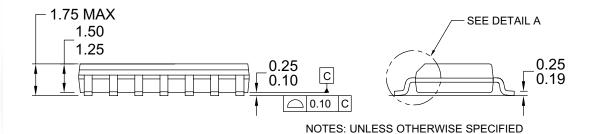
				т	' _A = 25°	С		-40°C 85°C	
Symbol	Parameter	V _{CC} (V)	Conditions	Min.	Тур.	Max.	Min.	Max.	Units
t _{PHL} , t _{PLH}	Propagation Delay	3.3 ± 0.3	C _L = 15pF		5.6	7.9	1.0	9.5	ns
			$C_L = 50pF$		8.1	11.4	1.0	13.0	
		5.0 ± 0.5	$C_L = 15pF$		3.6	5.5	1.0	6.5	ns
			$C_L = 50pF$		5.1	7.5	1.0	8.5	
C _{IN}	Input Capacitance		V _{CC} = Open		4	10		10	pF
C _{PD}	Power Dissipation Capacitance		(3)		15				pF

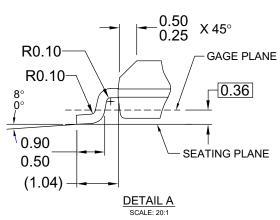
Note:

3. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4$ (per gate).

Physical Dimensions







- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

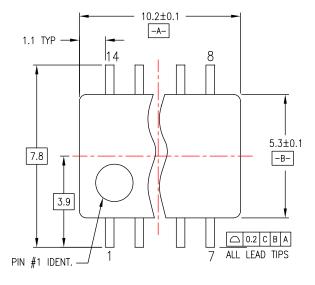
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

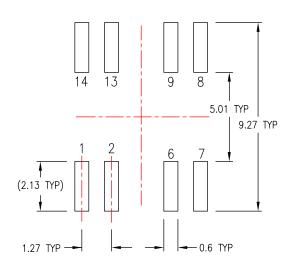
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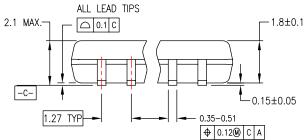
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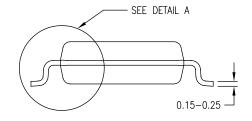
Physical Dimensions (Continued)





LAND PATTERN RECOMMENDATION





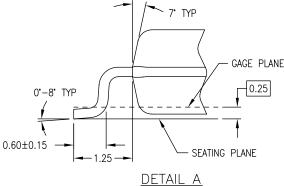
DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD

- FLASH, AND TIE BAR EXTRUSIONS.



M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued) 5.0±0.1 -A-0.65 0.43 TYP 6.4 4.4±0.1 -B-1.65 3.2 □ 0.2 C B A PIN #1 IDENT. 6.10 0.45 -LAND PATTERN RECOMMENDATION SEE DETAIL A ALL LEAD TIPS 0.90+0.15 1.2 MAX □ 0.1 C 0.09-0.20 -C-0.10±0.05 0.65 0.19 - 0.30⊕ 0.13M ABS CS 12.00°TOP & BOTTOM R0.09 min GAGE PLANE 0.25 0°-8° NOTES: 0.6±0.1 A. CONFORMS TO JEDEC REGISTRATION MO-153, SEATING PLANE R0.09min VARIATION AB, REF NOTE 6 -1 00 **B. DIMENSIONS ARE IN MILLIMETERS DETAIL A** C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,

- AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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