

74LVC1G07

Buffer with open-drain output

Rev. 14 — 8 June 2018

Product data sheet

1 General description

The 74LVC1G07 provides the non-inverting buffer.

The output of this device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2 Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2000 V
 - MM: JESD22-A115-A exceeds 200 V
- -24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G07GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G07GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G07GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm	SOT886
74LVC1G07GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm	SOT891
74LVC1G07GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 x 1.0 x 0.35 mm	SOT1115
74LVC1G07GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm	SOT1202
74LVC1G07GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.35 mm	SOT1226
74LVC1G07GX4	-40 °C to +125 °C	X2SON4	plastic thermal enhanced extremely thin small outline package; no leads; 4 terminals; body 0.6 x 0.6 x 0.32 mm	SOT1269-2

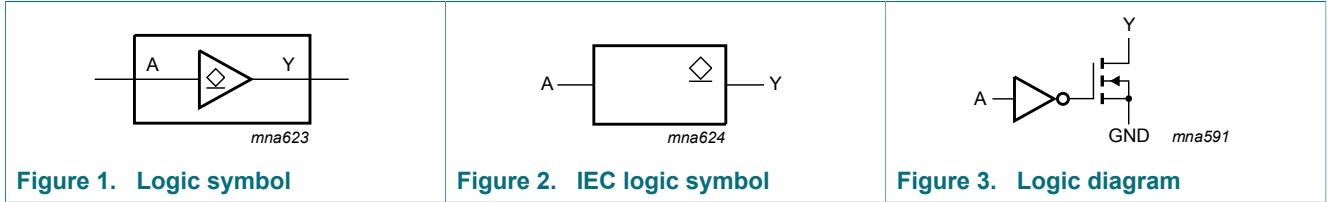
4 Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G07GW	VS
74LVC1G07GV	V07
74LVC1G07GM	VS
74LVC1G07GF	VS
74LVC1G07GN	VS
74LVC1G07GS	VS
74LVC1G07GX	VS
74LVC1G07GX4	VS

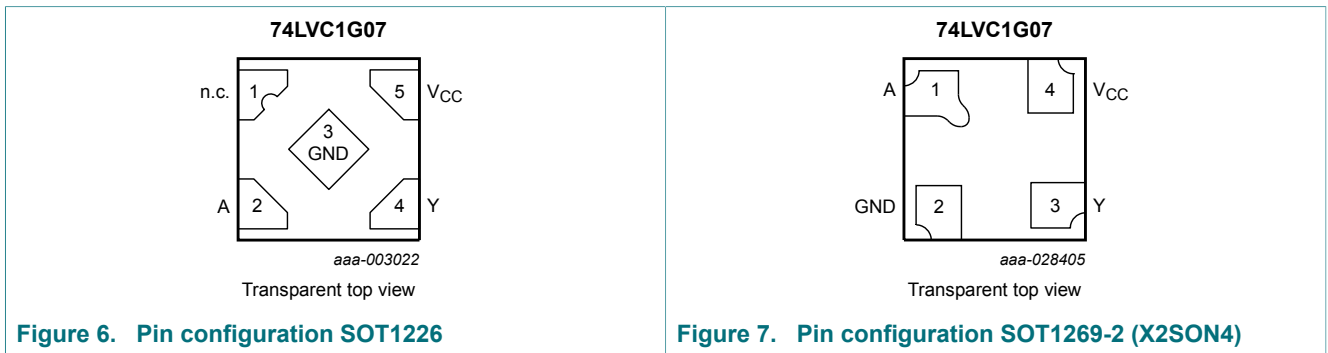
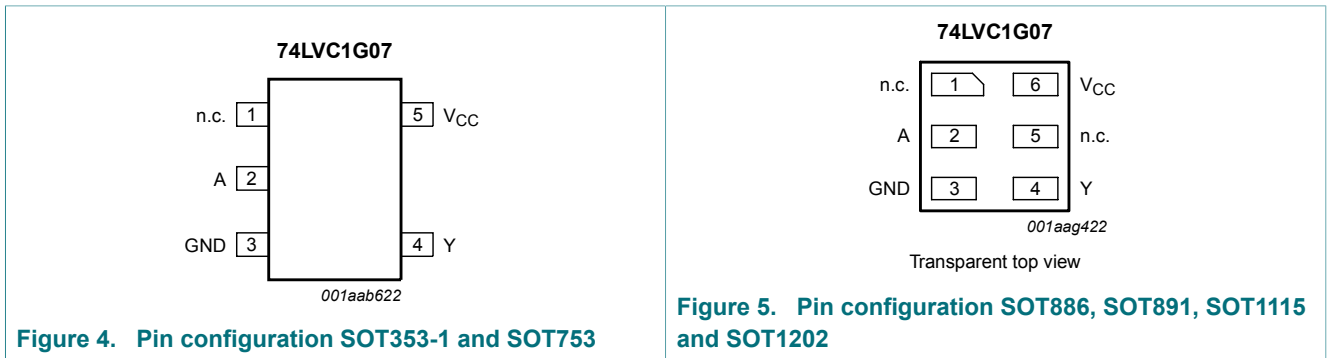
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5 Functional diagram



6 Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin			Description
	TSSOP5, SC-74A and X2SON5	XSON6	X2SON4	
n.c.	1	1, 5	-	not connected
A	2	2	1	data input
GND	3	3	2	ground (0 V)
Y	4	4	3	data output
V _{CC}	5	6	4	supply voltage

7 Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input A	Output Y
L	L
H	Z

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode [1]	-0.5	+6.5	V
		Power-down mode; $V_{CC} = 0$ V [1]	-0.5	+6.5	V
I_O	output current	$V_O = 0$ V to 6.5 V	-	50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		TSSOP5, SC-74A, XSON6 and X2SON5 package [2]	-	250	mW
		X2SON4 package [3]	-	150	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

For XSON6 and X2SON5 package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

[3] For X2SON4 packages: above 57 °C the value of P_{tot} derates linearly with 1.7 mW/K.

9 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	5.5	V
		Power-down mode; $V_{CC} = 0\text{ V}$	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	-	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	-	-	10	ns/V

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit								
			Min	Typ ^[1]	Max	Min	Max									
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V								
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V								
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V								
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V								
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V								
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V								
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V								
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V								
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}														
		I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.10	-	0.10	V								
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.70	V								
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.30	-	0.45	V								
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.40	-	0.60	V								
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.80	V								
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	μA								
		I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	±0.1	±2	-	±2	μA						
				I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	±0.1	±2	-	±2	μA				
						I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	0.1	4	-	4	μA		
								ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	5	500	-	500	μA
										C _I	input capacitance	V _{CC} = 3.3 V; V _I = GND to V _{CC}	-	5.0	-	-

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

11 Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	A to Y; see Figure 8 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	2.6	6.7	1.0	8.4	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	1.7	5.5	0.5	7.0	ns
		V _{CC} = 2.7 V	0.5	2.3	4.7	0.5	6.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.2	4.2	0.5	5.5	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.6	3.5	0.5	4.5	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3 V ^[3]	-	7.0	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLZ} and t_{PZL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1 Waveforms and test circuit

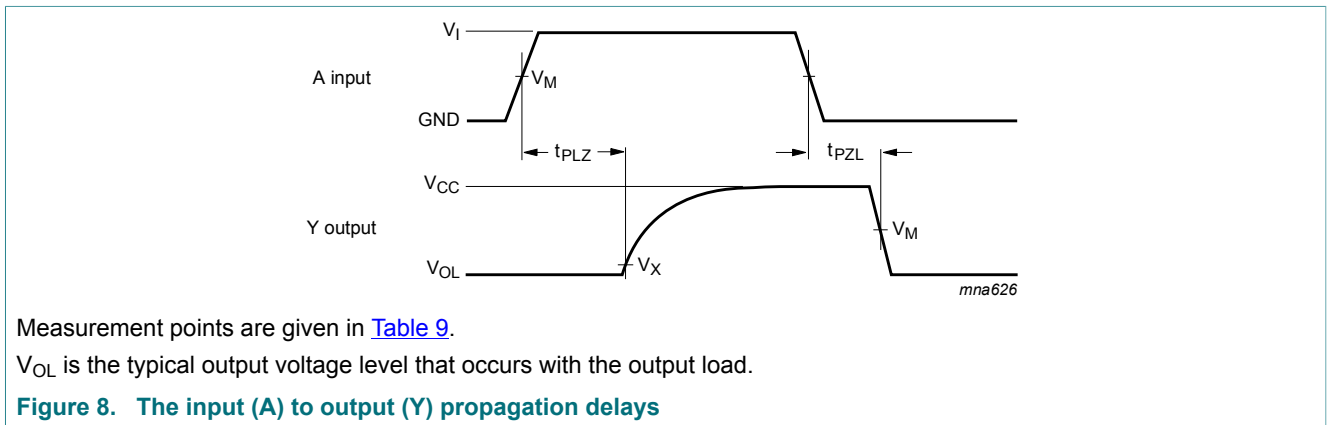
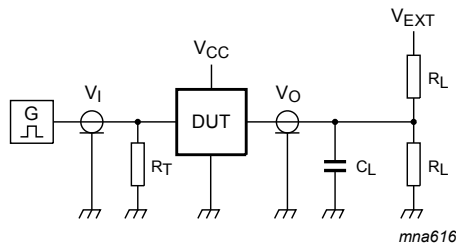


Table 9. Measurement points

Supply voltage	Input	Output	
V_{CC}	V_M	V_M	V_X
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 V$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 V$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Figure 9. Test circuit for measuring switching times

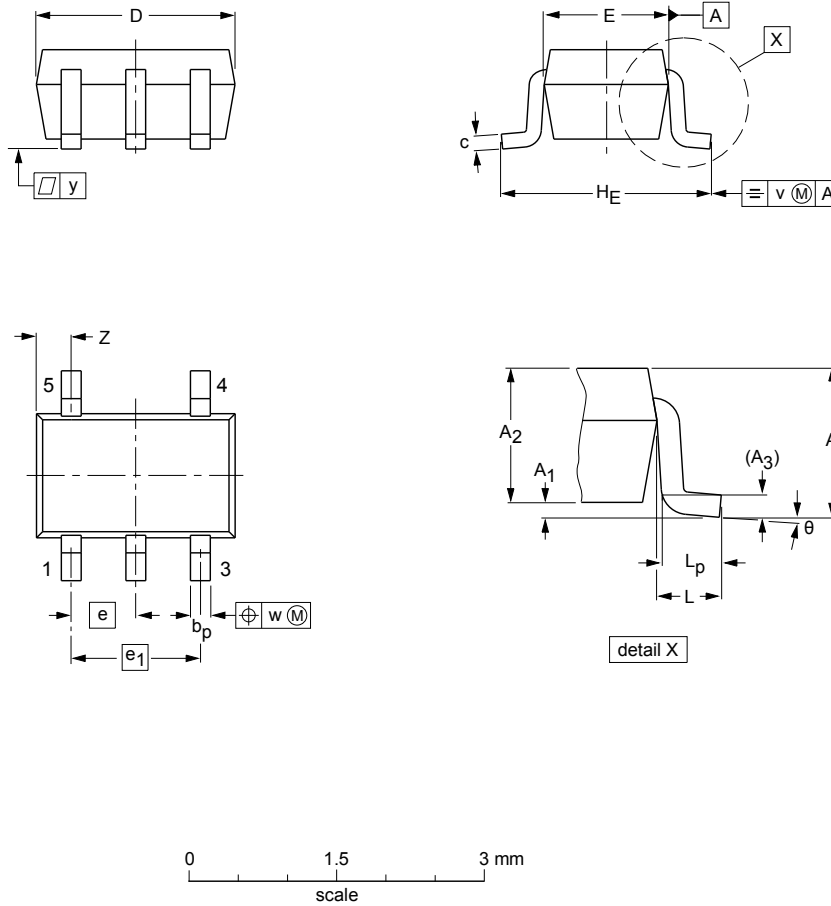
Table 10. Test data

Supply voltage	Input	Load			V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	$\leq 2.0 \text{ ns}$	30 pF	1 k Ω	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	$\leq 2.0 \text{ ns}$	30 pF	500 Ω	$2V_{CC}$
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	6 V
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	6 V
4.5 V to 5.5 V	V_{CC}	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	$2V_{CC}$

12 Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

Note

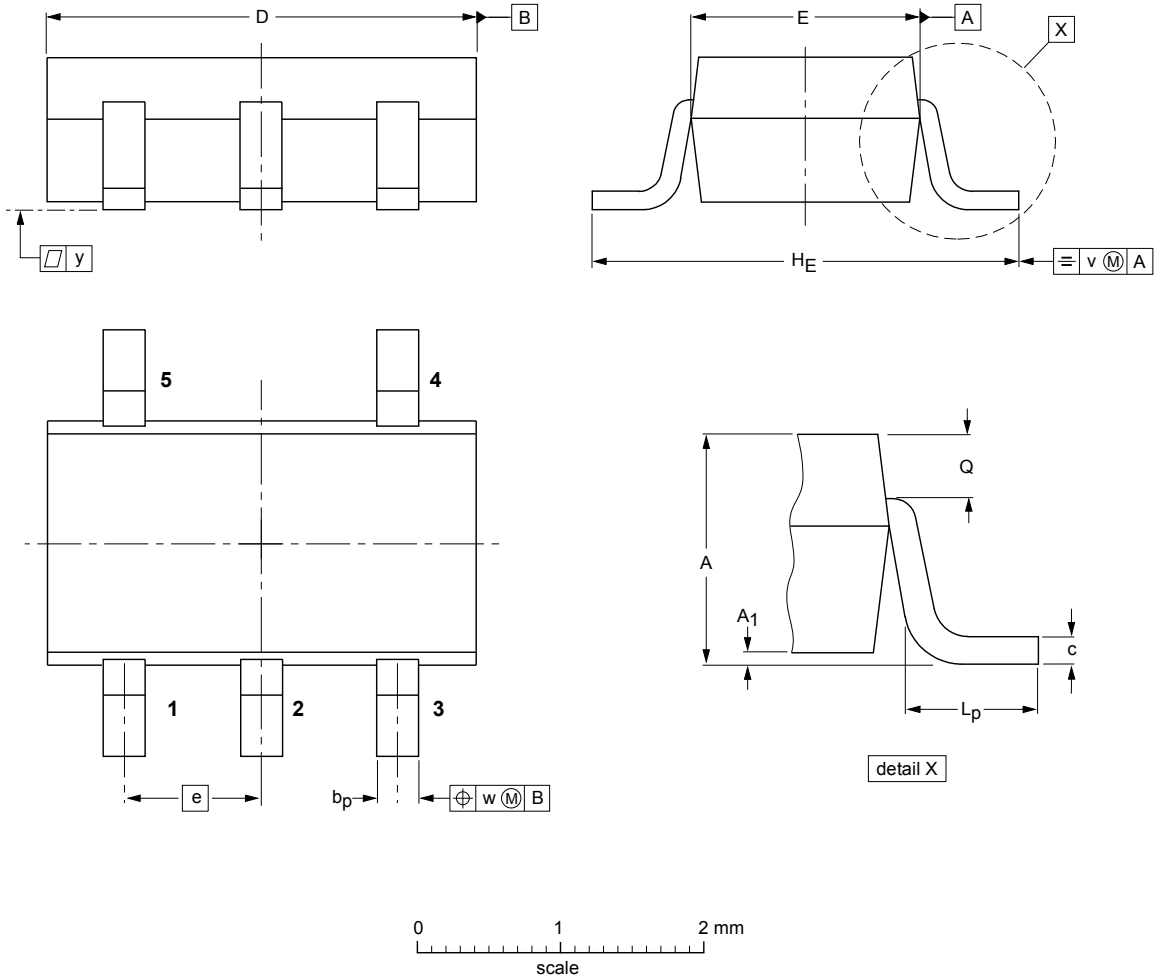
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT353-1		MO-203	SC-88A		00-09-01 03-02-19

Figure 10. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	c	D	E	e	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT753			SC-74A		-02-04-16 06-03-16

Figure 11. Package outline SOT753 (SC-74A)

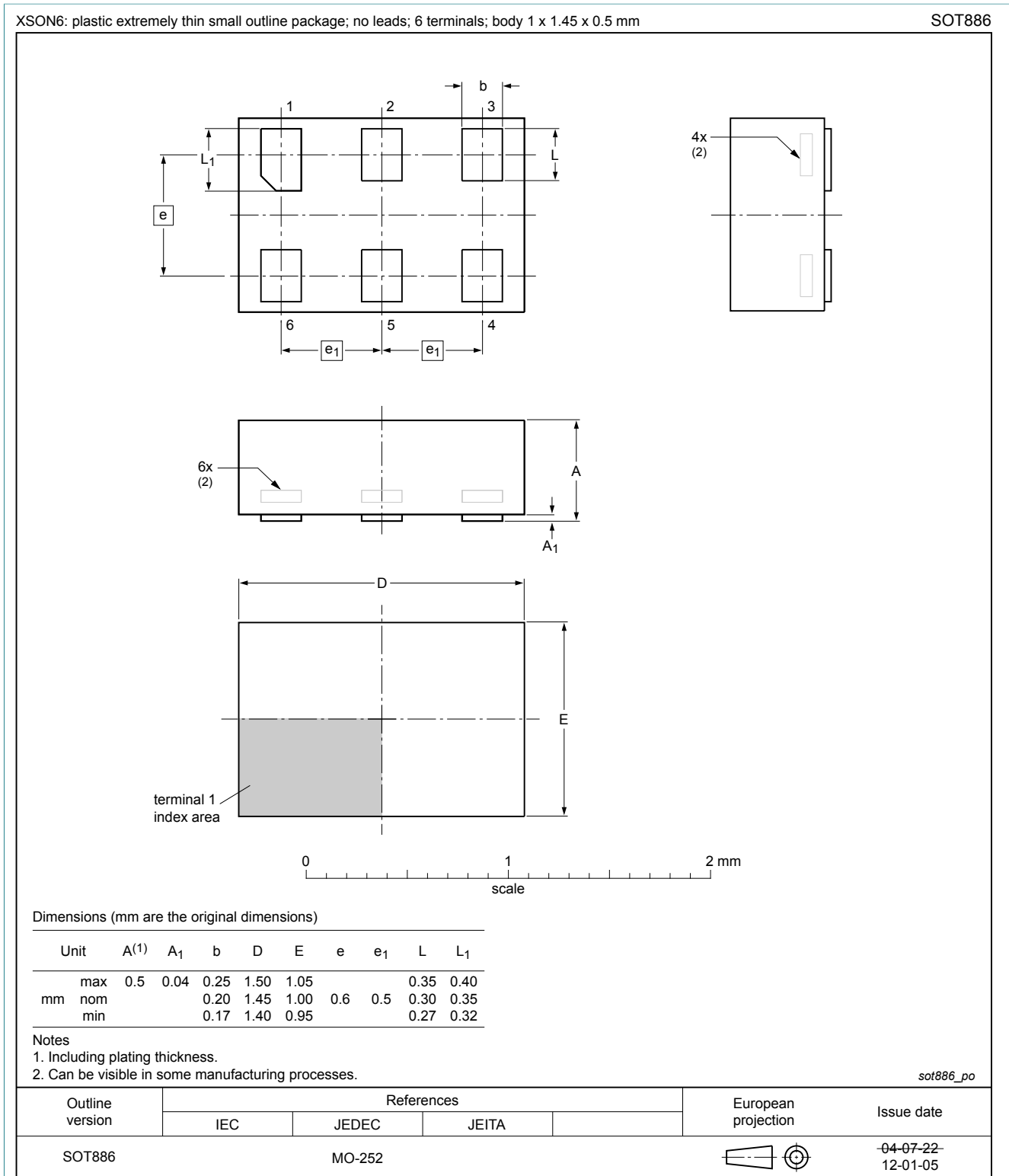
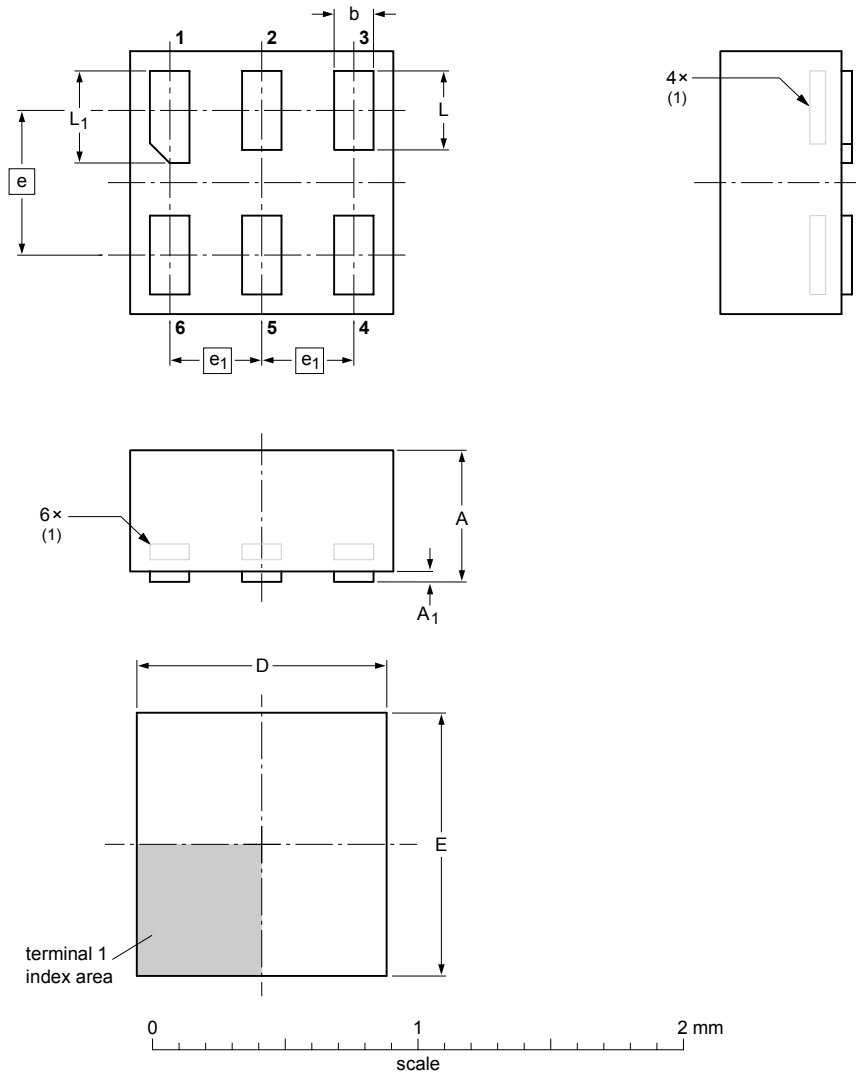


Figure 12. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.20 0.12	1.05 0.95	1.05 0.95	0.55	0.35	0.35 0.27	0.40 0.32

Note

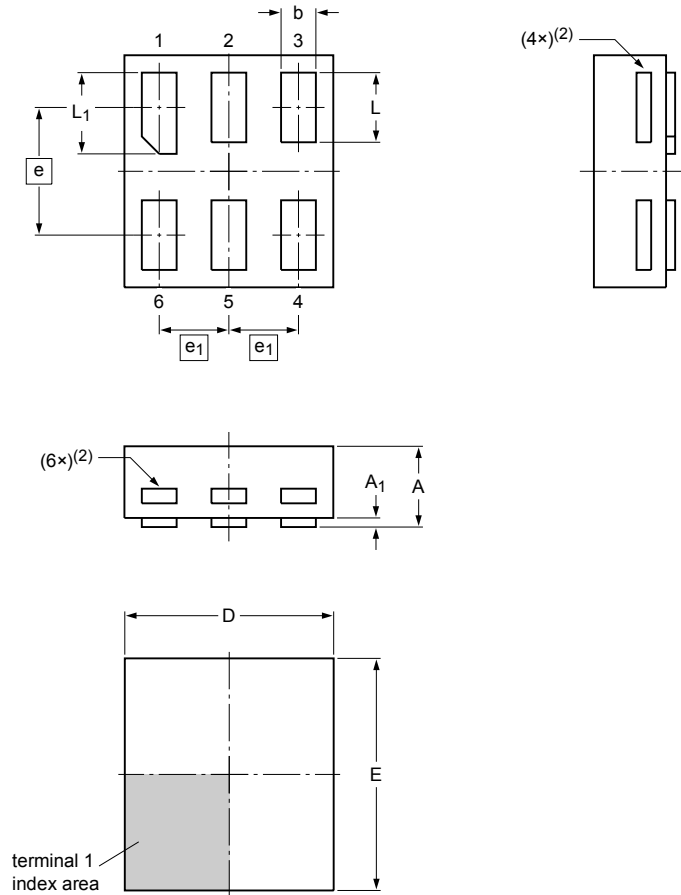
1. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT891					-05-04-06 07-05-15

Figure 13. Package outline SOT891 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm

SOT1115



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
max	0.35	0.04	0.20	0.95	1.05			0.35	0.40
nom			0.15	0.90	1.00	0.55	0.3	0.30	0.35
min			0.12	0.85	0.95			0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

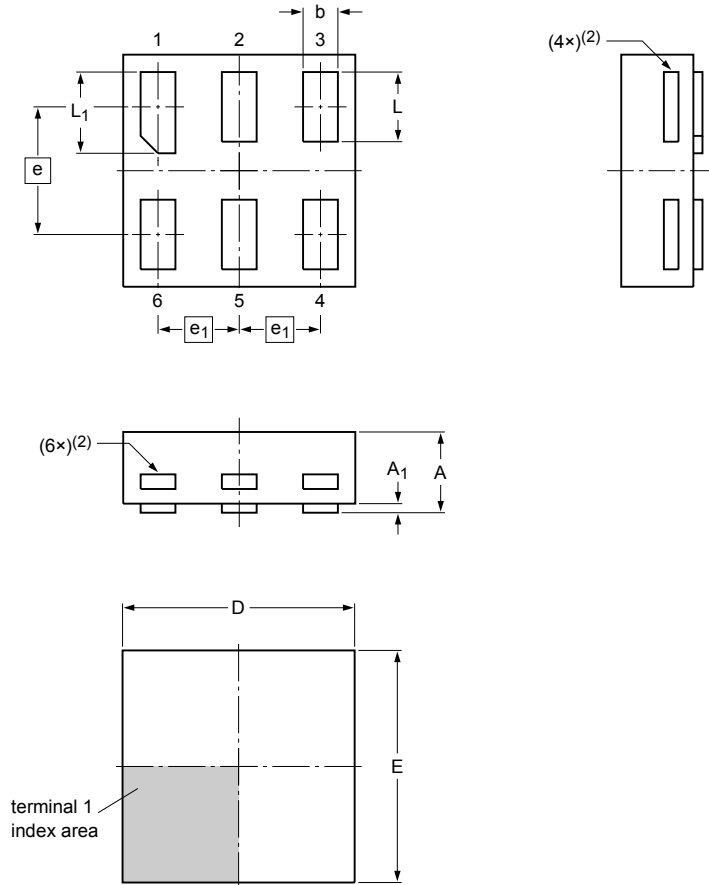
sot1115_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1115						-10-04-02- 10-04-07

Figure 14. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
min			0.12	0.95	0.95			0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

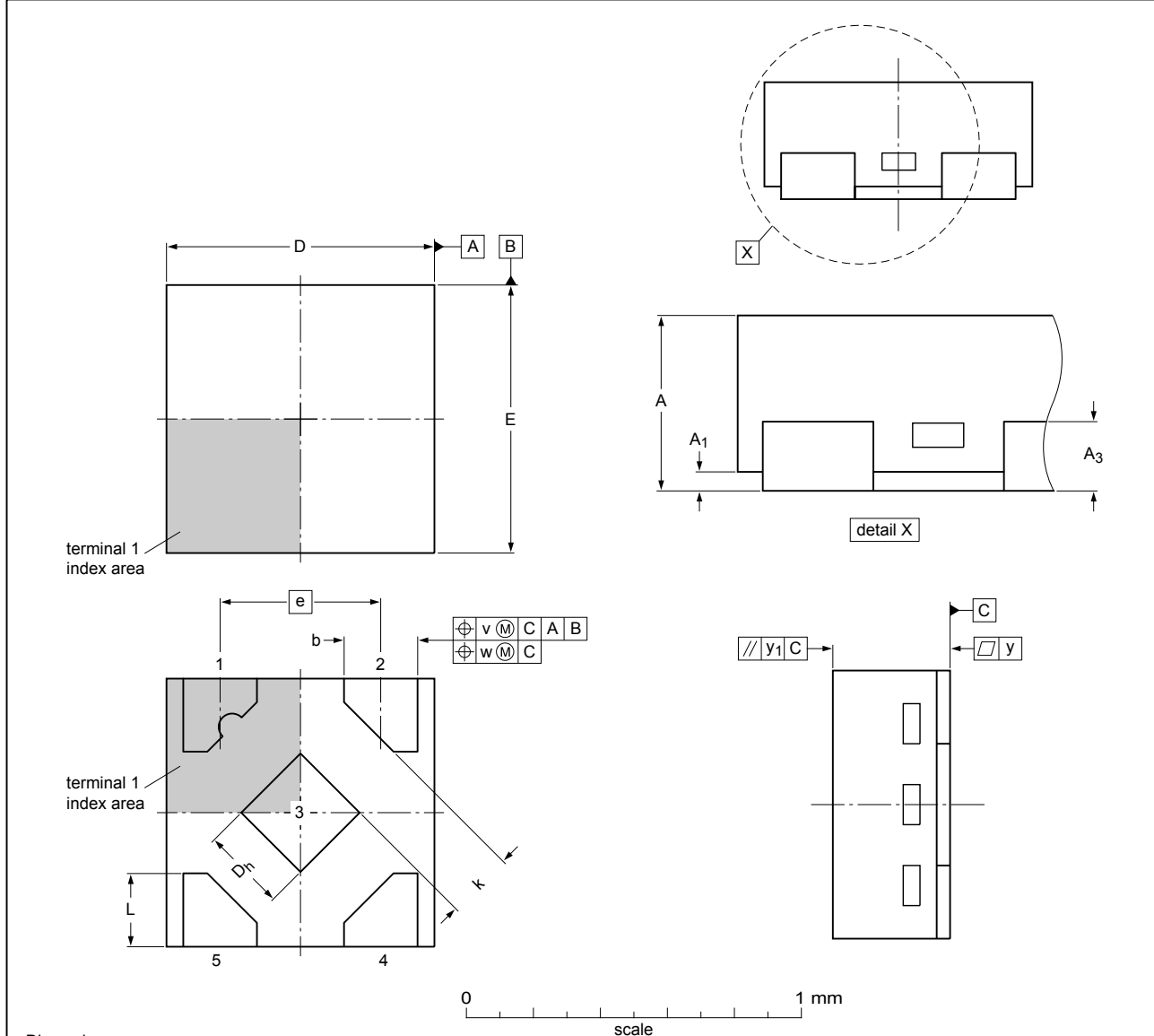
sot1202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						-10-04-02- 10-04-06

Figure 15. Package outline SOT1202 (XSON6)

X2SON5: plastic thermal enhanced extremely thin small outline package; no leads;
5 terminals; body 0.8 x 0.8 x 0.35 mm

SOT1226



Dimensions

Unit	A ⁽¹⁾	A ₁	A ₃	D	D _h	E	b	e	k	L	v	w	y	y ₁
max	0.35	0.04	0.128	0.85	0.30	0.85	0.27			0.27				
mm nom				0.80	0.25	0.80	0.22	0.48		0.22	0.1	0.05	0.05	0.05
min			0.040	0.75	0.20	0.75	0.17		0.20	0.17				

Note

1. Dimension A is including plating thickness.
2. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1226_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT1226						12-04-10 12-04-25

Figure 16. Package outline SOT1226 (X2SON5)

X2SON4: plastic thermal enhanced extremely thin small outline package; no leads;
4 terminals; body 0.6 x 0.6 x 0.32 mm

SOT1269-2

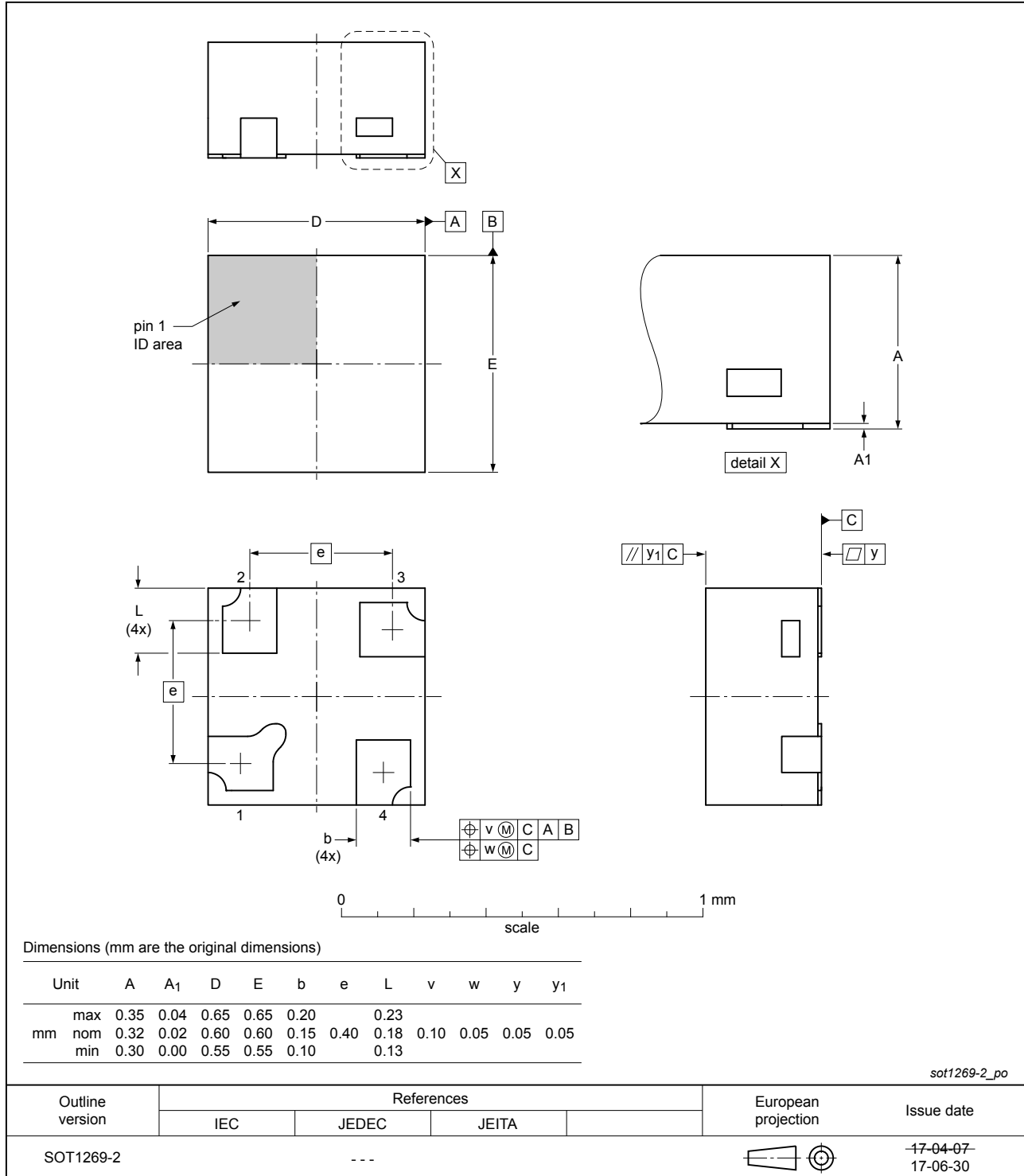


Figure 17. Package outline SOT1269-2 (X2SON4)

13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G07 v.14	20180608	Product data sheet	-	74LVC1G07 v.13
Modifications:	<ul style="list-style-type: none"> Added type number 74LVC1G07GX4 (SOT1269-2) 			
74LVC1G07 v.13	20170511	Product data sheet	-	74LVC1G07 v.12
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVC1G07 v.12	20161128	Product data sheet	-	74LVC1G07 v.11
Modifications:	<ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. 			
74LVC1G07 v.11	20120629	Product data sheet	-	74LVC1G07 v.10
Modifications:	<ul style="list-style-type: none"> Added type number 74LVC1G07GX (SOT1226) Package outline drawing of SOT886 (Figure 12) modified. 			
74LVC1G07 v.10	20111207	Product data sheet	-	74LVC1G07 v.9
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74LVC1G07 v.9	20100824	Product data sheet	-	74LVC1G07 v.8
74LVC1G07 v.8	20070717	Product data sheet	-	74LVC1G07 v.7
74LVC1G07 v.7	20070515	Product data sheet	-	74LVC1G07 v.6
74LVC1G07 v.6	20040907	Product specification	-	74LVC1G07 v.5
74LVC1G07 v.5	20030307	Product specification	-	74LVC1G07 v.4
74LVC1G07 v.4	20021002	Product specification	-	74LVC1G07 v.3
74LVC1G07 v.3	20020528	Product specification	-	74LVC1G07 v.2
74LVC1G07 v.2	20010406	Product specification	-	74LVC1G07 v.1
74LVC1G07 v.1	20001122	Product specification	-	-

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com

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