74LCX245 Low Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

Features

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- 5V tolerant inputs and outputs
- 2.3V to 3.6V V_{CC} specifications provided
- 7.0ns t_{PD} max. (V_{CC} = 3.3V), 10µA I_{CC} max.
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal⁽¹⁾
- ±24mA output drive (V_{CC} = 3.0V)
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 500mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
- Leadless DQFN package

Note:

 To ensure the high-impedance state during power up or down, OE should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

General Description

The LCX245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V and 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The T/R input determines the direction of data flow through the device. The \overline{OE} input disables both the A and B ports by placing them in a high impedance state.

The LCX245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Ordering Information

Order Number	Package Number	Package Description
74LCX245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX245BQX ⁽²⁾	MLP20B	20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74LCX245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LCX245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Note:

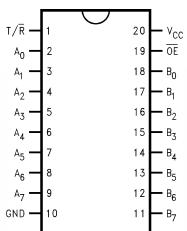
2. DQFN package available in Tape and Reel only.

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

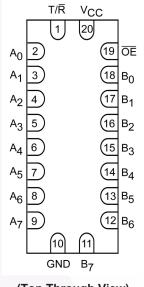
All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagrams

Pin Assignments for SOIC, SOP, SSOP, and TSSOP



Pin Assignment for DQFN

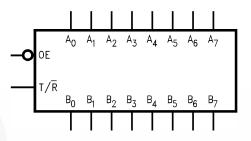


(Top Through View)

Pin Description

Pin Names	Description		
ŌĒ	Output Enable Input		
T/R	Transmit/Receive Input		
A ₀ -A ₇	Side A Inputs or 3-STATE Outputs		
B ₀ –B ₇	Side B Inputs or 3-STATE Outputs		

Logic Symbol



Truth Table

Inputs			
OE	T/R	Outputs	
L	L	Bus $B_0 - B_7$ Data to Bus $A_0 - A_7$	
L	Н	Bus $A_0 - A_7$ Data to Bus $B_0 - B_7$	
Н	Х	HIGH Z State on $A_0 - A_7$, $B_0 - B_7^{(3)}$	

H = HIGH Voltage Level

L = LOW Voltage Level

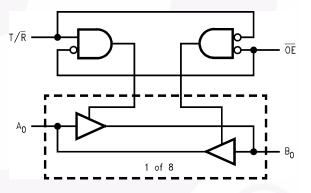
X = Immaterial

Z = High Impedance

Note:

3. Unused bus terminals during HIGH Z State must be held HIGH or LOW.

Logic Diagram



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	-0.5V to +7.0V
VI	DC Input Voltage	-0.5V to +7.0V
Vo	DC Output Voltage	
	Output in 3-STATE	-0.5V to +7.0V
	Output in HIGH or LOW State ⁽⁴⁾	–0.5V to V _{CC} + 0.5V
I _{IK}	DC Input Diode Current, V _I < GND	–50mA
I _{OK}	DC Output Diode Current	
	V _O < GND	–50mA
	V _O > V _{CC}	+50mA
Ι _Ο	DC Output Source/Sink Current	±50mA
I _{CC}	DC Supply Current per Supply Pin	±100mA
I _{GND}	DC Ground Current per Ground Pin	±100mA
T _{STG}	Storage Temperature	–65°C to +150°C

Note:

4. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions⁽⁵⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Supply Voltage			
	Operating	2.0	3.6	V
	Data Retention	1.5	3.6	
VI	Input Voltage	0	5.5	V
Vo	Output Voltage			
	3-STATE	0	5.5	V
	HIGH or LOW State	0	V _{CC}	
I _{OH} / I _{OL}	Output Current			
	$V_{CC} = 3.0V - 3.6V$		±24	mA
	$V_{CC} = 2.7V - 3.0V$		±12	
	V _{CC} = 2.3V–2.7V		±8	
T _A	Free-Air Operating Temperature	-40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$	0	10	ns/V

Note:

5. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

				$T_A = -40^{\circ}C$	to +85°C	
Symbol	Parameter	V _{CC} (V)	Conditions	Min.	Max.	Units
V _{IH}	HIGH Level Input Voltage	2.3–2.7		1.7		V
		2.7–3.6	-	2.0		
V _{IL}	LOW Level Input Voltage	2.3–2.7			0.7	V
		2.7-3.6			0.8	
V _{OH}	HIGH Level Output Voltage	2.3–3.6	I _{OH} = -100μA	V _{CC} – 0.2		V
		2.3	$I_{OH} = -8mA$	1.8]
		2.7	$I_{OH} = -12mA$	2.2]
		3.0	$I_{OH} = -18mA$	2.4]
			$I_{OH} = -24mA$	2.2]
V _{OL}	LOW Level Output Voltage	2.3–3.6	I _{OL} = 100μA		0.2	V
		2.3	$I_{OL} = 8mA$		0.6	
		2.7	$I_{OL} = 12mA$		0.4	
		3.0	$I_{OL} = 16 \text{mA}$		0.4	
			$I_{OL} = 24 \text{mA}$		0.55	
l _l	Input Leakage Current	2.3–3.6	$0 \le V_I \le 5.5V$		±5.0	μA
I _{OZ}	3-STATE Output Leakage	2.3–3.6	$0 \le V_O \le 5.5V,$ V _I = V _{IH} or V _{IL}		±5.0	μA
I _{OFF}	Power-Off Leakage Current	0	$V_{\rm I}$ or $V_{\rm O} = 5.5 V$		10	μA
I _{CC}	Quiescent Supply Current	2.3–3.6	$V_{I} = V_{CC}$ or GND		10	μA
			$3.6V \le V_I, V_O \le 5.5V^{(6)}$		±10	
ΔI_{CC}	Increase in I _{CC} per Input	2.3–3.6	$V_{IH} = V_{CC} - 0.6V$		500	μA

Note:

6. Outputs disabled or 3-STATE only.

AC Electrical Characteristics

		$T_A = -40^{\circ}C$ to +85°C, $R_L = 500\Omega$						
			3V ± 0.3V, 50pF		2.7V, 50pF	$V_{CC} = 2.5$ $C_L =$	V ± 0.2V, 30pF	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{PHL} , t _{PLH}	Propagation Delay, A _n to B _n or B _n to A _n	1.5	7.0	1.5	8.0	1.5	8.4	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	1.5	7.5	1.5	8.5	1.5	9.0	ns
t _{OSHL} , t _{OSLH}	Output to Output Skew ⁽⁷⁾		1.0					ns

Note:

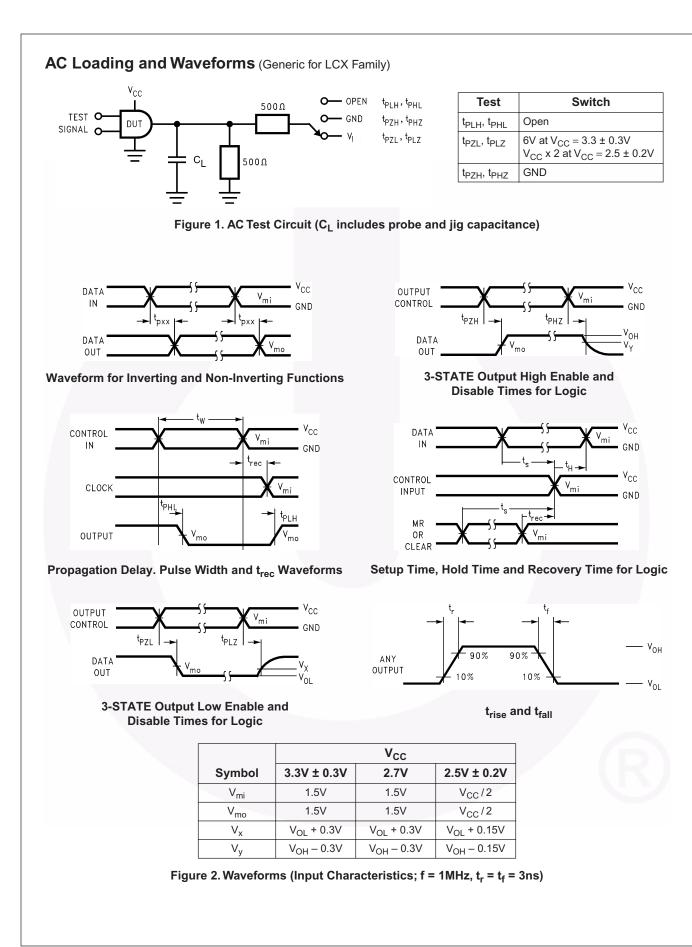
 Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

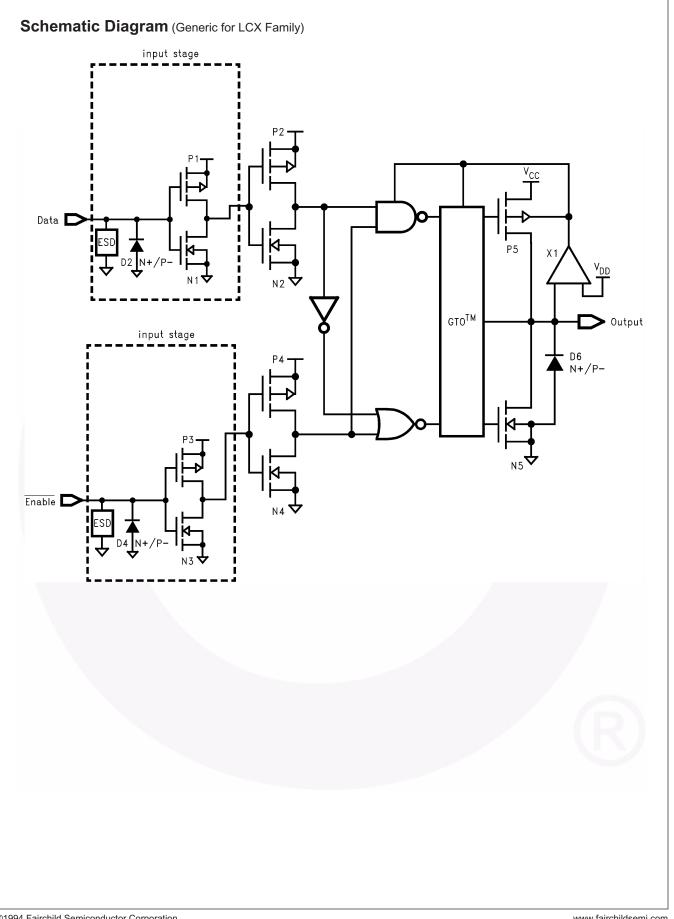
Dynamic Switching Characteristics

				$T_A = 25^{\circ}C$	
Symbol	Parameter	V _{CC} (V)	Conditions	Typical	Unit
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	3.3	$C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V$	0.8	V
		2.5	$C_L = 30 pF$, $V_{IH} = 2.5 V$, $V_{IL} = 0 V$	0.6	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	3.3	$C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V$	-0.8	V
		2.5	$C_{L} = 30 pF, V_{IH} = 2.5V, V_{IL} = 0V$	-0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	$V_{CC} = Open, V_I = 0V \text{ or } V_{CC}$	7.0	pF
C _{OUT}	Output Capacitance	$V_{CC} = 3.3$ V, $V_I = 0$ V or V_{CC}	8.0	pF
C _{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_{I} = 0V or V_{CC} , f = 10MHz	25.0	pF



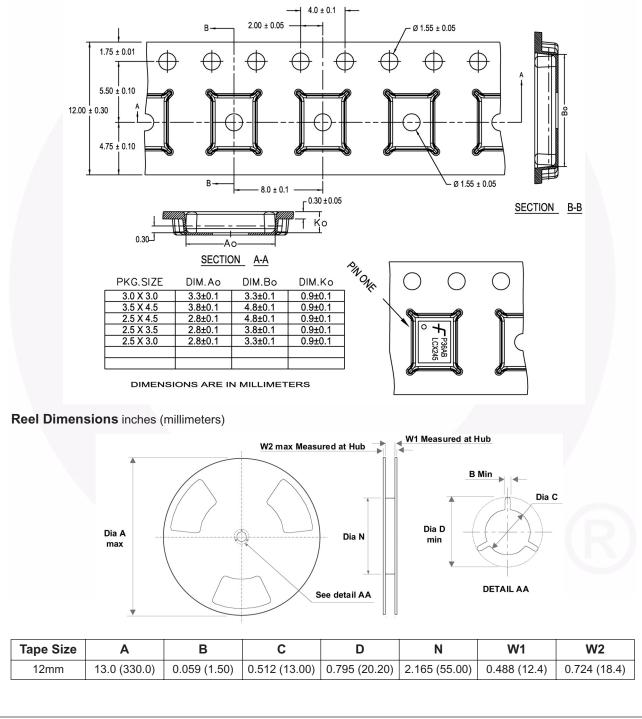


Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

Tape Dimension inches (millimeters)



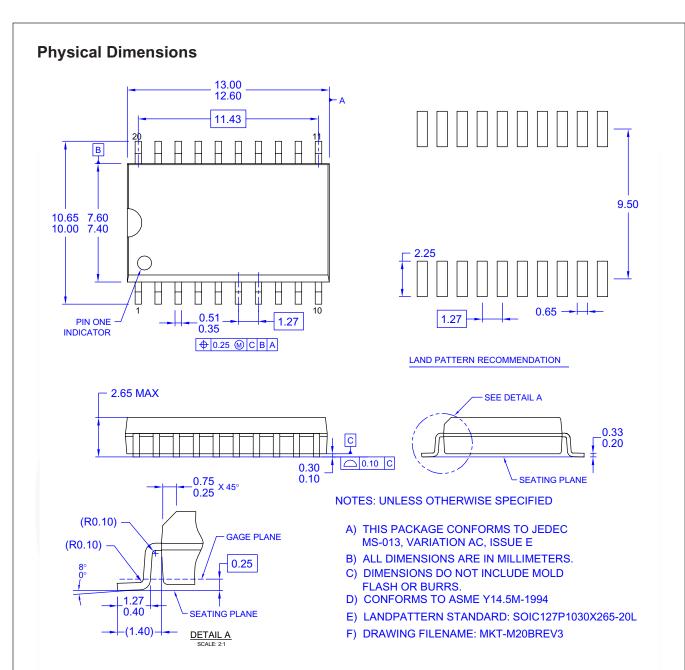
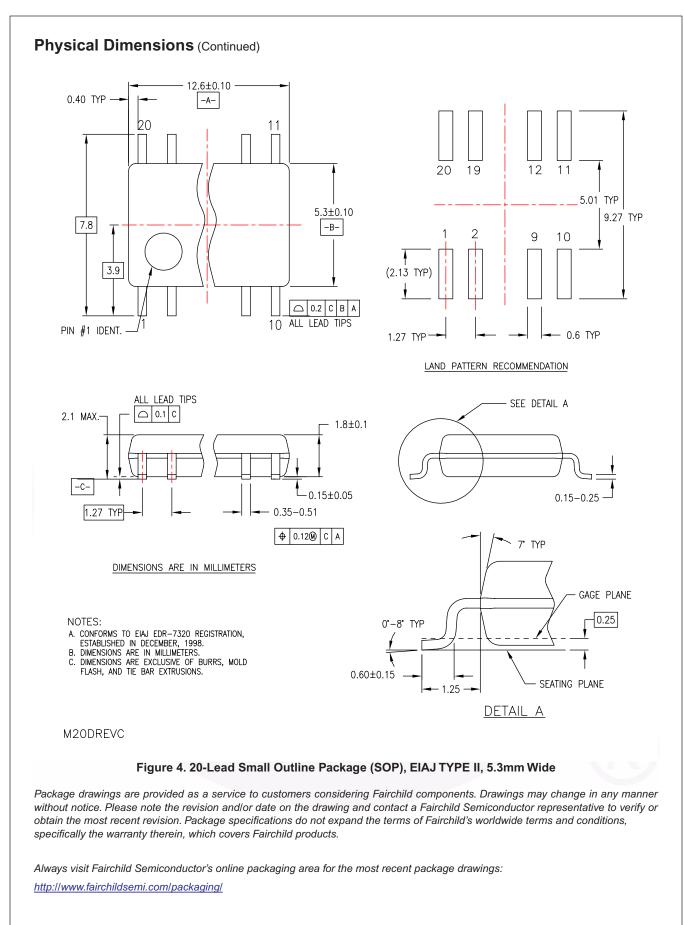
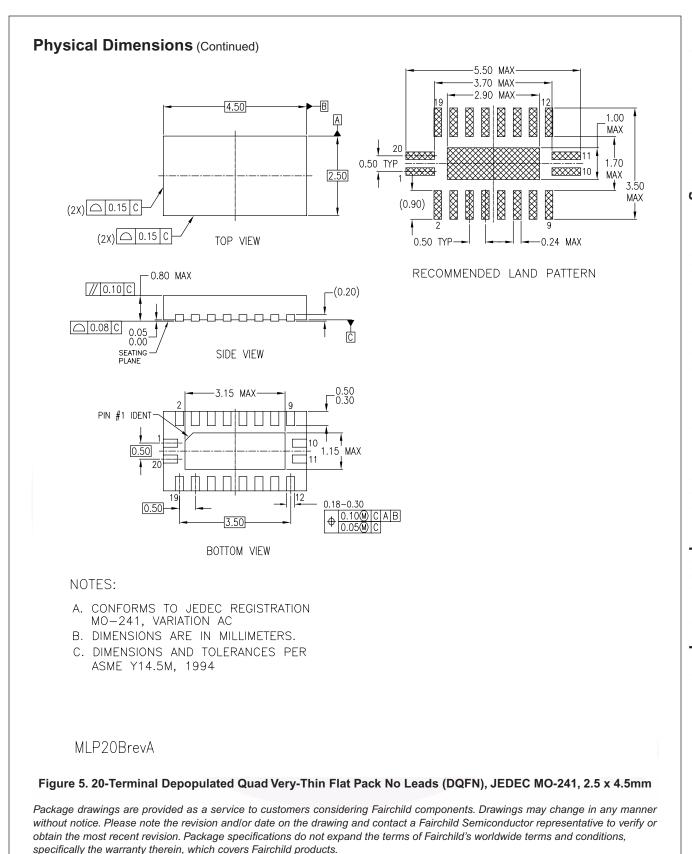


Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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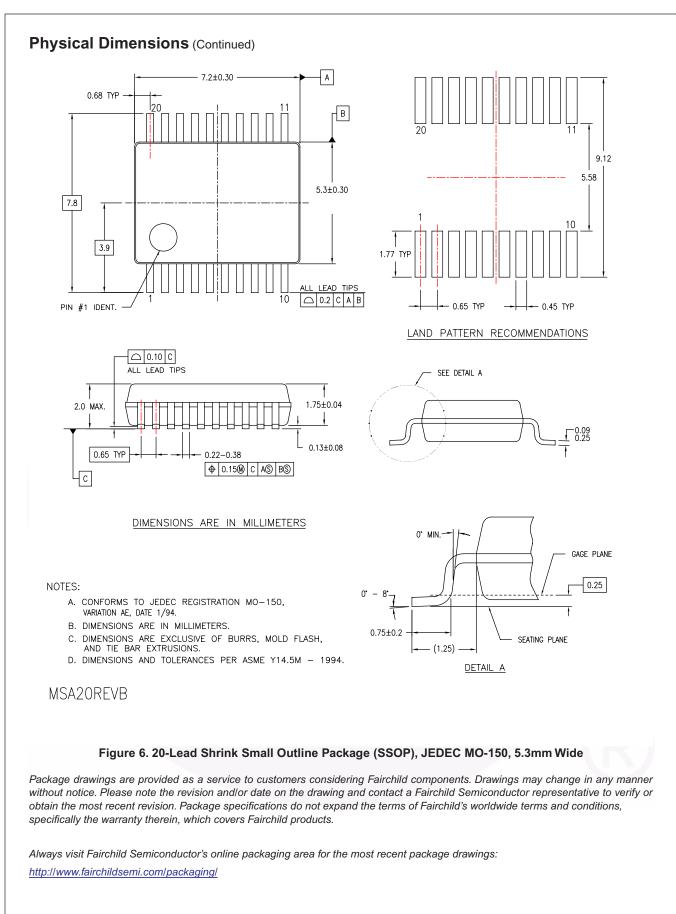


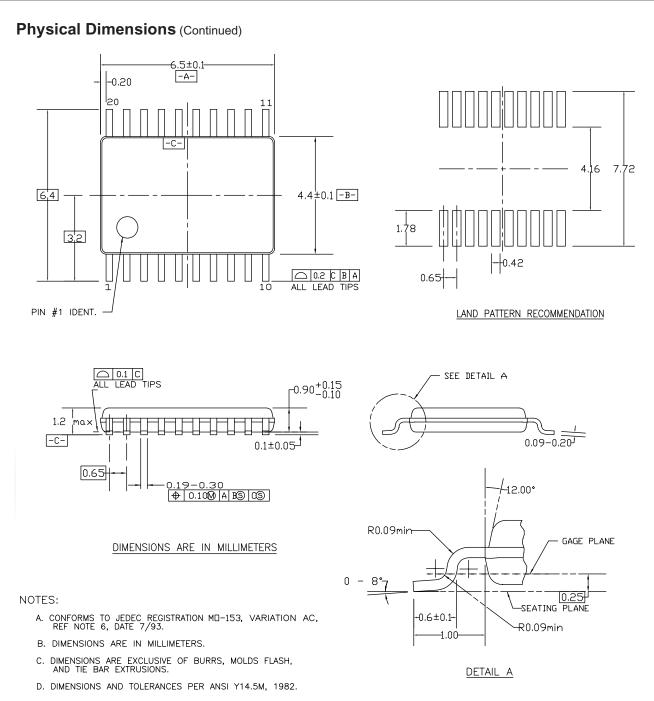


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MTC20REVD1

Figure 8. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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