

February 2010

74LVX3245 8-Bit Dual Supply Translating Transceiver with 3-STATE Outputs

General Description

The LVX3245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 3V bus and a 5V bus in a mixed 3V/5V supply environment. The Transmit/ Receive (T/ \overline{R}) input determines the direction of data flow. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B Ports by placing them in a high impedance condition. The A Port interfaces with the 3V bus; the B Port interfaces with the 5V bus.

The LVX3245 is suitable for mixed voltage applications such as notebook computers using 3.3V CPU and 5V peripheral components.

Features

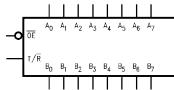
- Bidirectional interface between 3V and 5V buses
- Inputs compatible with TTL level
- 3V data flow at A Port and 5V data flow at B Port
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Implements proprietary EMI reduction circuitry
- Functionally compatible with the 74 series 245

Ordering Code:

Order Number	Package Number	Package Description
74LVX3245WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVX3245QSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
74LVX3245MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

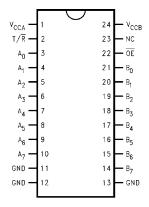
Logic Symbol/s



Pin Descriptions

Pin Names	Description
OE	Output Enable Input
T/R	Transmit/Receive Input
A ₀ –A ₇	Side A Inputs or 3-STATE Outputs
B ₀ –B ₇	Side B Inputs or 3-STATE Outputs

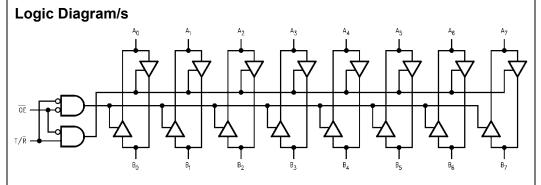
Connection Diagram/s



Truth Table/s

Inp	uts	Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	Н	Bus A Data to Bus B
Н	х	HIGH-Z State

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial



Absolute Maximum Ratings(Note 1)

Supply Voltage (V _{CCA} , V _{CCB})	-0.5V to +7.0V
DC Input Voltage (VI) @ OE, T/R	-0.5V to V _{CCA} + 0.5V
DC Input/Output Voltage (VI/O)	
@A _n	–0.5V to $V_{\mbox{\scriptsize CCA}}$ + 0.5V
@ B _n	–0.5V to $V_{CCB}{+}0.5V$
DC Input Diode Current (IIN)	
@ OE, T/R	±20 mA
DC Output Diode Current (I _{OK})	±50 mA
DC Output Source or	
Sink Current (I _O)	±50 mA
DC V _{CC} or Ground Current	
per Output Pin (I _{CC} or I _{GND})	±50 mA
and Max Current @ I _{CCA}	±100 mA
@ I _{CCB}	±200 mA
Storage Temperature Range (T _{STG})	−65°C to +150°C
DC Latch-Up Source or	
Sink Current	±300 mA
Maximum Junction Temperature	
Under Bias (T _J)	+150°C

Recommended Operating Conditions (Note 2)

Supply Voltage	
V _{CCA}	2.7V to 3.6V
V _{CCB}	4.5V to 5.5V
Input Voltage (V _I) @ OE, T/R	0V to V_{CCA}
Input/Output Voltage (V _{I/O})	
@ A _n	0V to V_{CCA}
@ B _n	0V to V _{CCB}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	8 ns/V
V_{IN} from 30% to 70% of V_{CC}	
V _{CC} @ 3.0V, 4.5V, 5.5V	

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused Pins (inputs and I/Os) must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	I Parameter		V _{CCA}	V _{CCB}	TA = -	+25°C	$\textbf{T}_{\textbf{A}} = -40^{\circ}\textbf{C} \text{ to } +85^{\circ}\textbf{C}$	Units	Conditions
Symbol	Falameter		(V)	(V)	Тур	Gu	aranteed Limits	Units	Conditions
V _{IHA}	Minimum HIGH Level	A _n , T/R,	3.6	5.0		2.0	2.0		
	Input Voltage	OE	2.7	5.0		2.0	2.0	v	$V_{OUT} \le 0.1V$ or
V _{IHB}		B _n	3.3	4.5		2.0	2.0	v	$\geq V_{CC} - 0.1V$
			3.3	5.5		2.0	2.0		
V _{ILA}	Maximum LOW Level	A _n , T/R,	3.6	5.0		0.8	0.8		
	Input Voltage	OE	2.7	5.0		0.8	0.8	v	$V_{OUT} \le 0.1V$ or
V _{ILB}		B _n	3.3	4.5		0.8	0.8	v	$\geq V_{CC} - 0.1V$
			3.3	5.5		0.8	0.8		
V _{OHA}	Minimum HIGH Level		3.0	4.5	2.99	2.9	2.9		$I_{OUT} = -100 \ \mu A$
	Output Voltage		3.0	4.5	2.65	2.35	2.25	v	$I_{OH} = -24 \text{ mA}$
			2.7	4.5	2.5	2.3	2.2	v	$I_{OH} = -12 \text{ mA}$
			2.7	4.5	2.3	2.1	2.0		$I_{OH} = -24 \text{ mA}$
V _{OHB}	НВ		3.0	4.5	4.5	4.4	4.4	v	$I_{OUT} = -100 \ \mu A$
			3.0	4.5	4.25	3.86	3.76	v	$I_{OH} = -24 \text{ mA}$
V _{OLA}	Maximum LOW Level		3.0	4.5	0.002	0.1	0.1		I _{OUT} =100 μA
	Output Voltage		3.0	4.5	0.21	0.36	0.44	v	I _{OL} = 24 mA
			2.7	4.5	0.11	0.36	0.44	v	$I_{OL} = 12 \text{ mA}$
			2.7	4.5	0.22	0.42	0.5		I _{OL} = 24 mA
V _{OLB}			3.0	4.5	0.002	0.1	0.1	v	$I_{OUT} = 100 \ \mu A$
			3.0	4.5	0.18	0.36	0.44	v	I _{OL} = 24 mA
I _{IN}	Maximum Input								
	Leakage Current		3.6	5.5		±0.1	±1.0	μA	$V_I = V_{CCB}, GNE$
	@ OE, T/R								
I _{OZA}	Maximum 3-STATE								$V_I = V_{IL}, V_{IH}$
	Output Leakage		3.6	5.5		±0.5	±5.0		$\overline{OE} = V_{CCA}$
	@ A _n								$V_O = V_{CCA}, GND$
I _{OZB}	Maximum 3-STATE								$V_I = V_{IL}, V_{IH}$
	Output Leakage		3.6	5.5		±0.5	±5.0	μA	$\overline{OE} = V_{CCA}$
	@ B _n								$V_O = V_{CCB}$, GND

Symbol	Paramet	Parameter		V _{CCB}	$T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions
Cymbol	i alameter		(V)	(V)	Тур	Gu	aranteed Limits	0	Contaitions
ΔI_{CC}	Maximum	B _n	3.6	5.5	1.0	1.35	1.5	mA	$V_I = V_{CCB} - 2.1V$
	I _{CCT} /Input @	A _n , T/R, OE	3.6	5.5		0.35	0.5	mA	$V_I = V_{CCA} - 0.6V$
I _{CCA}	Quiescent V _{CCA} Supply Current		3.6	5.5		5	50	μΑ	
I _{CCB}	Quiescent V _{CCB} Supply Current		3.6	5.5		8	80	μΑ	$\begin{split} A_n &= V_{CCA} \text{ or GND} \\ B_n &= V_{CCB} \text{ or GND}, \\ \overline{OE} &= GND, \ T/\overline{R} &= V_{CCA} \end{split}$
V _{OLPA} V _{OLPB}	Quiet Output Maximu Dynamic V _{OL}	m	3.3 3.3	5.0 5.0		0.8 1.5		V	(Note 3) (Note 4)
V _{OLVA} V _{OLVB}	Quiet Output Minimun Dynamic V _{OL}	n	3.3 3.3	5.0 5.0		-0.8 -1.2		V	(Note 3) (Note 4)
V _{IHDA} V _{IHDB}	Minimum HIGH Level Dynamic Input Voltage		3.3 3.3	5.0 5.0		2.0 2.0		v	(Note 3) (Note 5)
V _{ILDA} V _{ILDB}	Maximum LOW Level Dynamic Input Voltage		3.3 3.3	5.0 5.0		0.8 0.8		V	(Note 3) (Note 5)

Note 3: Worst case package.

Note 4: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 5: Max number of Data Inputs (n) switching. (n–1) inputs switching 0V to V_{CC} level. Input-under-test switching:

 V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1 \mbox{ MHz}.

AC Electrical Characteristics

			T _A = +25°C	;	$T_A = -40^\circ$	C to +85°C	T _A = -40°	C to +85°C	
			C _L = 50 pF		C _L =	50 pF			Units
Symbol	Parameters	V _{CC}	_ = 3.3V (N	ote 6)	V _{CCA} = 3.3	BV (Note 6)			
		V _{CCE}	V _{CCB} = 5.0V (Note 7)			V _{CCB} = 5.0V (Note 7)		V _{CCB} = 5.0V (Note 7)	
		Min	Тур	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.0	5.4	8.0	1.0	8.5	1.0	9.0	ns
t _{PLH}	A to B	1.0	5.6	7.5	1.0	8.0	1.0	8.5	115
t _{PHL}	Propagation Delay	1.0	5.1	7.5	1.0	8.0	1.0	8.5	ns
t _{PLH}	B to A	1.0	5.7	7.5	1.0	8.0	1.0	8.5	115
t _{PZL}	Output Enable	1.0	4.8	8.0	1.0	8.5	1.0	9.0	20
t _{PZH}	Time OE to B	1.0	6.3	8.5	1.0	9.0	1.0	9.5	ns
t _{PZL}	Output Enable	1.0	6.3	8.5	1.0	9.0	1.0	9.5	
t _{PZH}	Time OE to A	1.0	6.8	9.0	1.0	9.5	1.0	10.0	ns
t _{PHZ}	Output Disable	1.0	5.3	7.5	1.0	8.0	1.0	8.5	
t _{PLZ}	Time OE to B	1.0	4.2	7.0	1.0	7.5	1.0	8.0	ns
t _{PHZ}	Output Disable	1.0	5.3	8.0	1.0	8.5	1.0	9.0	ns
t _{PLZ}	Time OE to A	1.0	3.7	6.5	1.0	7.0	1.0	7.5	115
t _{OSHL}	Output to Output								
t _{OSLH}	Skew (Note 8)		1.0	1.5		1.5		1.5	ns
	Data to Output								

Note 6: Voltage Range 3.3V is 3.3V \pm 0.3V.

Note 7: Voltage Range 5.0V is 5.0V \pm 0.5V.

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter		Тур	Units	Conditions
C _{IN}	Input Capacitance		4.5	pF	V _{CC} = Open
C _{I/O}	Input/Output		15	pF	$V_{CCA} = 3.3V$ $V_{CCB} = 5.0V$
	Capacitance			pi	$V_{CCB} = 5.0V$
C _{PD}	Power Dissipation $A \rightarrow B$		55	pF	$V_{CCB} = 5.0V$
	Capacitance (Note 9)	$B\toA$	40	pi	$V_{CCA} = 3.3V$

Note 9: C_{PD} is measured at 10 MHz

8-Bit Dual Supply Translating Transceiver

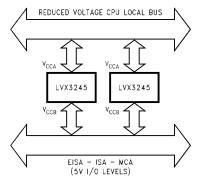
The LVX3245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX3245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.

Power Up Considerations

To insure that the system does not experience unnecessary I_{CC} current draw, bus contention, or oscillations during power up, the following guidelines should be adhered to (refer to Table 1):

- Power up the control side of the device first. This is the $V_{\mbox{\scriptsize CCA}}.$
- OE should ramp with or ahead of V_{CCA}. This will help guard against bus contention.
- The Transmit/Receive control pin (T/ $\!\overline{\!R}\!$) should ramp with V_{CCA} , this will ensure that the A Port data pins are con-



figured as inputs. With V_{CCA} receiving power first, the A I/O Port should be configured as inputs to help guard against bus contention and oscillations.

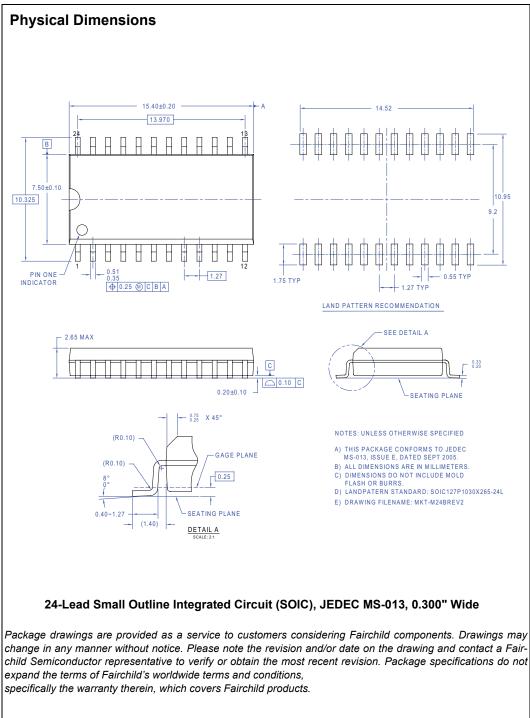
• A side data inputs should be driven to a valid logic level. This will prevent excessive current draw.

The above steps will ensure that no bus contention or oscillations, and therefore no excessive current draw occurs during the power up cycling of these devices. These steps will help prevent possible damage to the translator devices and potential damage to other system components.

TABLE 1. Low Voltage	Translator Power	Up Sequencing Table
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Device Type	V _{CCA}	V _{CCB}	T/R	OE	A Side I/O	B Side I/O	Floatable Pin Allowed
74LVX3245	3V	5V	ramp	ramp	logic	outputs	No
1 1207102 10	(power up 1st)	configurable	with V _{CCA}	with V _{CCA}	0V or V _{CCA}	ouputo	

Please reference Application Note AN-5001 for more detailed information on using Fairchild's LVX Low Voltage Dual Supply CMOS Translating Transceivers.



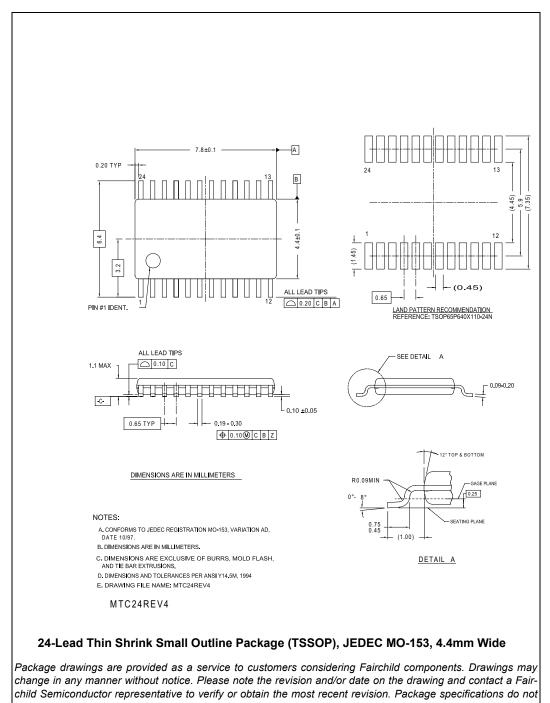
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-1.75 8.74 13 0.10 M A-B А D П Π П Π 5.60 3.99 3.84 6 0 0.10 A-B Н Н Н ННН Н Н Н .635 2X 12 TIPS 0.635 В 24X 0.3 LAND PATTERN RECOMMENDATION TOP VIEW ⊕ 0.178 M C A-B D (0.695) 1.49 1.39 DETAIL A 0.71 45 0.203 0.161 1.73 MAX С 0.61 END VIEW SIDE VIEW 0°M IN R0.008 Min GAGE PLANE NOTES : R0.008 0.013 A. THIS PACKAGE CONFORMS TO JEDEC M0-137 VARIATION AE **B. ALL DIMENSIONS ARE IN MILLIMETERS** C. DRAWING CONFORMS TO С SEATING PLANE 0.254 ASME Y14.5M-1994 D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS DETAIL A E. LAND PATTERN STANDARD: SOP63P600X175-24M F. DRAWING FILE NAME: MKT-MQA24REV2

24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide

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